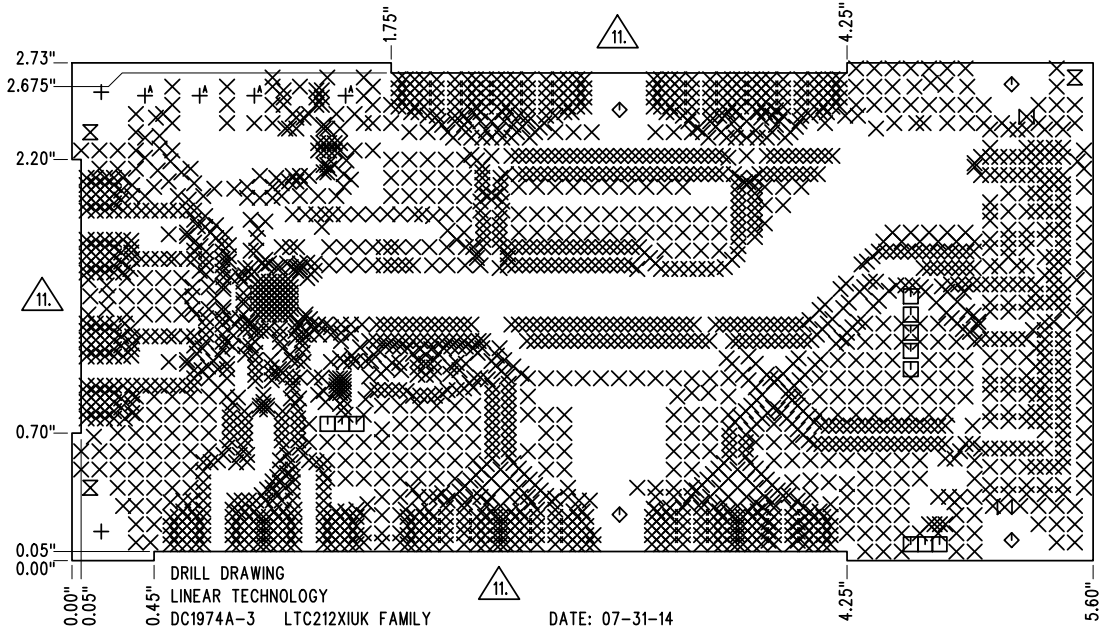
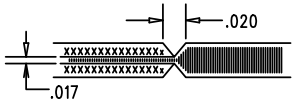
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
–	3	PRODUCTION	CLARENCE M.	07–31–14

SHOWN FROM TOP SIDE



NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC–A–600.
2. MATERIAL: –LEAD FREE ASSEMBLY COMPLIANT, NELCO 4000–13EP.
   –FINISHED THICKNESS TO BE 0.062" +/– .005"
   –TOTAL OF 6 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
   –FLAMMABILITY RATING: 94 V–O MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN. 0.00" ARE PRIMARY DATUMS.
4. DRILLING: –DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
   –ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
   –HOLE LOCATION TOLERANCES ARE +/–0.003" IN RELATION TO CENTER
5. FINISH: –SMOBC USING LPI BOTH SIDES, COLOR GREEN.
   –GOLD IMMERSION BOTH SIDES.
   –FOR SILKSCREENS: USE WHITE NON–CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
7. PCBS ARE TO BE RoHS COMPLIANT.
8. SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):

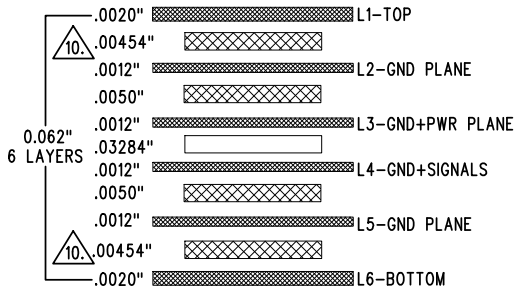


9. A. CONTROLLED 50 OHM +/–10% IMPEDANCE FOR LAYERS 1–3, USING 0.020" TRACE AT 2GHz FREQ.
   B. CONTROLLED 50 OHM +/–10% IMPEDANCE FOR SINGLE ENDED STRIP LINE FOR LAYER 1–2 AND LAYER 6–5, USING 0.006" TRACE AT 2GHz FREQ.
   C. CONTROLLED 100 OHM +/–10% IMPEDANCE FOR DIFFERENTIAL PAIR FOR LAYER 1–2 AND 6–5 USING 7 MIL TRACES, 13 MIL GAP.

10. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

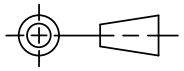
11. INNER AND OUTER LAYER COPPER SHALL BE EXPOSED ALONG BOARD EDGES. DO NOT MODIFY INNER LAYER COPPER BACKOFF OUTLINE (SMA CONNECTOR).

LAYER STRUCTURE



SIZE	QTY	SYM	PLATED	TOL
0.125	2	+	NO	+/–0.003"
0.008	2364	×	YES	+/–0.003"
0.035	11	□	YES	+/–0.003"
0.19	4	◇	NO	+/–0.003"
0.07	3	⧖	NO	+/–0.003"
0.05	2	⋈	NO	+/–0.003"
0.094	4	+A	YES	+/–0.003"

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
0.XX" = ±0.01"
0.XXX" = ±0.005"
INTERPRET DIM AND TOL PER ASME Y14.5M–1994
THIRD ANGLE PROJECTION



APPROVALS	
PCB DES.	KIM T.
APP ENG.	CLARENCE M.
SCALE = NONE	

LINEAR TECHNOLOGY
1630 MCCARTHY BLVD
MILPITAS, CA 95035
PH: (408)432–1900
www.linear.com

TITLE: FABRICATION DRAWING

DUAL 14–BIT HIGH SPEED ADC WITH JESD204B SERIAL OUTPUTS

SIZE	IC NO.	REV
N/A	LTC212XIUK FAMILY DEMO CIRCUIT 1974A	3

FILENAME: DC1974A–3.PCB SHT 1 OF 1