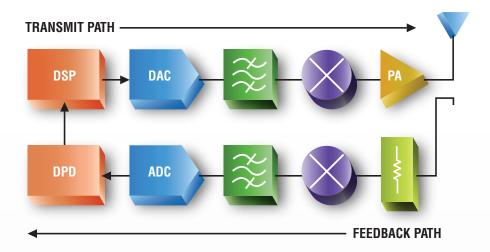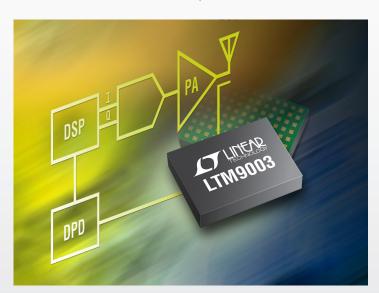# Digital Predistortion Solutions

The power amplifier (PA) consumes more electrical power than any other block in a cellular basestation and is a significant factor in the operating expense for the service provider. Since complex digital modulation requires extremely high linearity from the PA, it must be driven well below saturation where it is most efficient. To improve PA efficiency, designers use digital techniques to reduce the crest factor and improve PA linearity, allowing it to run closer to saturation. Digital predistortion (DPD) has emerged as the preferred method of PA linearization. The complete solution consists of the DPD algorithm in the FPGA and the RF feedback receiver, also called the observation path receiver.
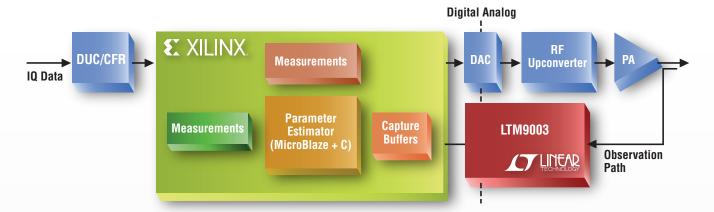

The LTM®9003 is a wideband RF-to-digital receiver subsystem that includes a high performance 12-bit, 250Msps analog-to-digital converter (ADC), a bandpass filter, intermediate frequency (IF) amplifier and a high linearity RF downconverting mixer. The integrated µModule® receiver offers a significant reduction in board space and development time for wireless basestations implementing PA linearization with DPD. The LTM9003 harnesses years of signal chain design experience in an easy-to-use 11.25mm × 15mm µModule package.

Product	ADC	Bandpass Filter	Passband Flatness	Digital I/O	SNR	SFDR	Power	Supply Voltage Range	Packages
LTM9003-AA	12-Bit, 250Msps	184MHz Center, 125MHz BW	0.5dB	LVDS, Parallel	143.9dB/Hz	58.8dB	1472mW	2.5V (ADC), 3.3V (Amp), 3.3V (Mixer)	15mm × 11.25mm × 2.32mm LGA
LTM9003-AB	12-Bit, 250Msps	184MHz Center, 125MHz BW	0.5dB	LVDS, Parallel	143.9dB/Hz	62.4dB	1591mW	2.5V (ADC), 3.3V (Amp), 5V (Mixer)	15mm × 11.25mm × 2.32mm LGA

Xilinx Digital Predistortion LogiCORE IP Core

The Xilinx digital predistortion LogiCORE IP uses a combination of high speed data path processing and software running on a MicroBlaze processor. The processor subsystem is used to calculate sets of values that represent the behavior of the amplifier under certain signal conditions. These values are used to precondition the signal before it enters the PA. Tests have shown 40% efficiency for a typical class AB power amplifier module, a significant improvement over the 10% range without digital predistortion. This enhancement leads to millions of dollars saved per annum in operational expenditure in a typical network deployment.

DPD V3.0 Features

- Support for Xilinx Virtex-5, Virtex-6 and Spartan-6 Devices
- 1-4 Transmit Antennas
- 1-4 Clocks per Output Sample to Optimize Correction Performance vs Area
- Multiple Memory Correction Models to Optimize Correction Performance vs Area
- Up to 60MHz of Transmit Bandwidth Support (20MHz with Spartan-6 FPGA)
- Overdrive Detection and Adaptive Quadrature Modulation Correction
- High Performance – Spectral Correction Ranging from 15dB to 30dB Depending on Amplifier and Air Interface
- Algorithm Support for Memory and Reactive Effects

- Real IF or Complex IF Sampling Receiver Selection
- Advanced Debugging – Signal Status, Debug and Diagnostics Interface Capabilities
- Tested with 30+ Power Amplifiers Ranging from Class AB to Symmetric/Asymmetric Doherty Architectures from NXP, Freescale and Other Manufacturers
- Low FPGA Utilization:
  - 1Tx and 3 Clocks per Sample Shown for Comparison
  - Architecture A, B and C Represent Different Memory Polynomial Models, with Architecture C Typically Providing Up to 6dB of Additional Correction Performance at the Expense of More DSP48s

Family	Arch	Tx Path	Clocks/Sample	Has QMC	Slices	BRAM_36k	BRAM_18k	BRAMS_9k	DSP48
Virtex-5	A	1	3	✔	1374	37	0	0	17
Virtex-5	B	1	3	✔	1447	39	0	0	23
Virtex-5	C	1	3	✔	1423	41	0	0	29
Virtex-6	A	1	3	✔	1123	37	0	0	17
Virtex-6	B	1	3	✔	1157	39	0	0	23
Virtex-6	C	1	3	✔	1236	41	0	0	29
Spartan-6	A	1	3	✔	1204	0	69	2	18
Spartan-6	B	1	3	✔	1297	0	72	2	24
Spartan-6	C	1	3	✔	1324	0	75	2	30

Availability

The Xilinx V3.0 LogiCORE IP design is available now. To request your copy of the DPD V3.0 LogiCORE IP, please contact your local Xilinx sales representative.

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