

# DESIGN NOTES

## Maximize the Performance of 16-Bit, 105MSPS ADC with Careful IF Signal Chain Design

Design Note 468

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### Introduction

Modern communication systems require an ADC to receive an analog signal and then convert it into a digital signal that can be processed with an FPGA. The job of a mixed signal engineer is to optimize the signal at the input of the ADC to maximize overall system performance. This usually requires a signal chain comprised of multiple gain and filtering sections. An ADC is only as good as the signal it is measuring.

For instance, the LTC<sup>®</sup>2274 provides excellent AC performance with an appropriate IF signal chain. The LTC2274 is a 16-bit, 105MSPS ADC that serially transmits 8B/10B encoded output data compliant with the JESD204 specification. It uses a single differential transmission line pair to reduce the number of IO lines required to transmit output data. The LTC2274 has 77dB of SNR, and 100dB of spurious free dynamic range.

### Signal Chain Topology

Figure 2 details a signal chain optimized for a 70MHz center frequency and a 20MHz bandwidth driving the LTC2274. The final filter and circuitry around the ADC are shown in detail. The earlier stages of the chain can be changed to suit a target application.

The first stage of amplification in the chain uses an AH31 from TriQuint Semiconductor. This GaAs FET amplifier offers a low noise figure and high IP3 point, which minimizes distortion caused by the amplifier stage. It provides 14dB of gain over a wide frequency region. The high IP3 prevents intermodulation distortion between frequencies outside the passband of the surface acoustic wave (SAW) filter.

A SAW filter follows the amplification stage for band selection. The SAW filter offers excellent selectivity and a flat passband if matched correctly. Gain before the SAW must not be higher than the maximum input power rating

of the SAW; otherwise it leads to distortion. A digitally controlled step attenuator may be required in the signal path to control the power going into the SAW filter.

The second stage of amplification is used to recover the loss in the SAW filter. The insertion loss of the SAW filter is about -15dB, so the final amplifier should have at least this much gain, plus enough gain to accommodate the final filter. By splitting the gain between two amplifiers, the noise and distortion can be optimized without overdriving the SAW filter. It also allows for a final filter with better suppression of noise from the final amplifier, improving SNR and selectivity.

The output stage of the final filter needs to be absorptive to accommodate the ADC front end. This suppresses glitches reflected back from the direct sampling process.

This signal chain will not degrade the performance of the LTC2274. When receiving a 4-channel WCDMA signal with a 20MHz bandwidth, centered at 70MHz, the ACPR is 71.5dB (see Figure 1).

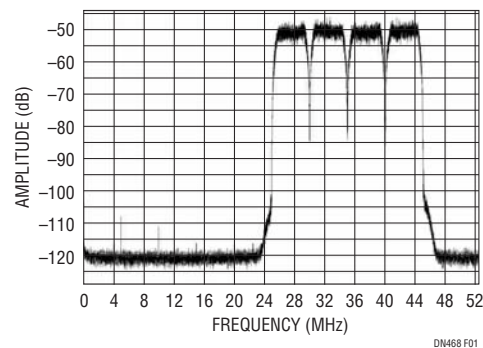


Figure 1. Typical Spread Spectrum Performance

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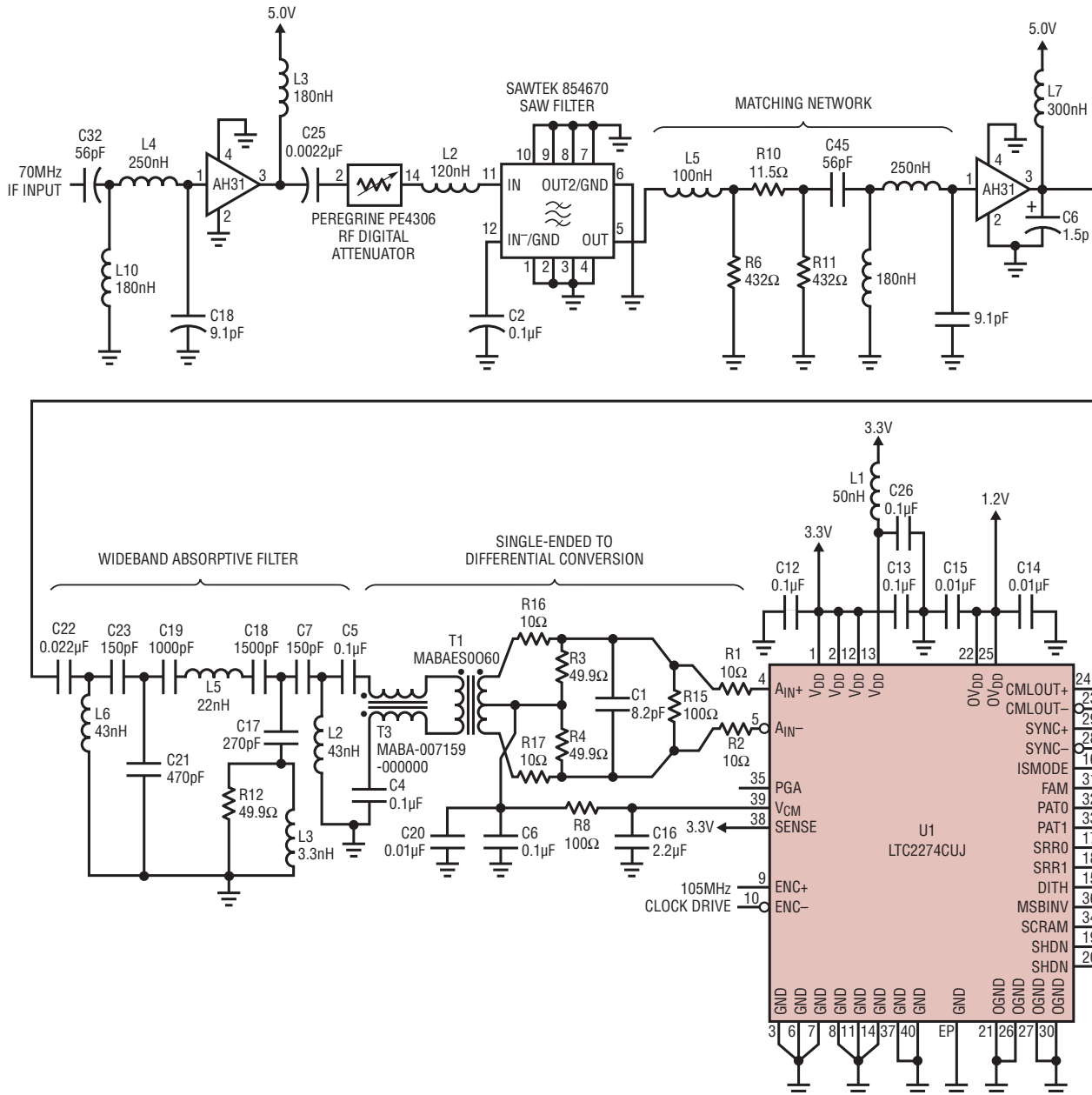


Figure 2. IF Receiver Chain

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## Conclusion

The LTC2274 can be used to receive high IF frequencies, but getting the most out of this high performance ADC requires a carefully designed analog front end. The performance of the LTC2274 is such that it is possible to dispense with the automatic gain control and build a

receiver with a low fixed gain. The LTC2274 is a part of a family of 16-bit converters that range in sample rate from 65Msps to 105Msps. For complete schematics of this receiver network, visit [www.linear.com](http://www.linear.com)

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