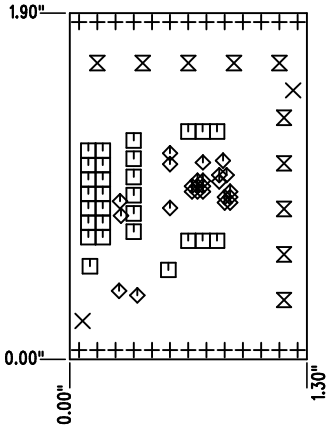
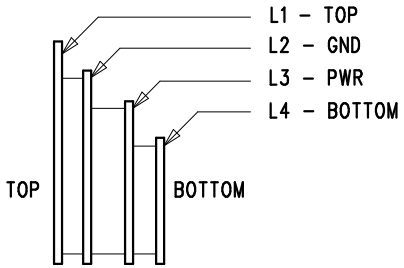
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
–	2	PRODUCTION	LEO C.	08-06-10

SHOWN FROM TOP SIDE



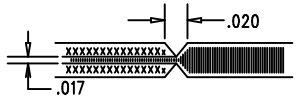
LAYER STRUCTURE



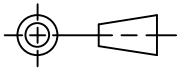
SIZE	QTY	SYM	PLATED	TOL
0.02	26	+	YES	+/–0.003"
0.07	2	X	NO	+/–0.003"
0.035	28	□	YES	+/–0.003"
0.012	25	◇	YES	+/–0.003"
0.064	10	⧖	YES	+/–0.003"

NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC-A-600.
2. MATERIAL: –EPOXY FIBERGLASS, NEMA GRADE FR-4
   –FINISHED THICKNESS TO BE 0.062" +/– .005"
   –TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
   –FLAMMABILITY RATING: 94 V–0 MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN. 0.00" ARE PRIMARY DATUMS.
4. DRILLING: –DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
   –ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
   –HOLE LOCATION TOLERANCES ARE +/–0.003" IN RELATION TO CENTER
5. FINISH: –SMOBC USING LPI BOTH SIDES, COLOR GREEN.
   –GOLD IMMERSION BOTH SIDES.
   –FOR SILKSCREEN: TOP SIDE USE WHITE NON–CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
7. PCBS ARE TO BE RoHS COMPLIANT.
8. SCORING FOR PANELIZED PCB:



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
0.XX" = ±0.01"
0.XXX" = ±0.005"
INTERPRET DIM AND TOL PER ASME Y14.5M–1994
THIRD ANGLE PROJECTION



APPROVALS	
PCB DES.	KT
APP ENG.	LEO C.

SCALE = NONE

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TITLE: FABRICATION DRAWING
QUAD 12/16-BIT RAIL-TO-RAIL SPI DAC WITH 10ppm/°C MAX REFERENCE

SIZE	IC NO.	REV
N/A	LTC2654CUF FAMILY DEMO CIRCUIT 1678A	2

FILENAME: DC1678A-2.PCB
SHT 1 OF 1