Five-Channel, Low Dropout, 300 mA, Current Source Output, 16-Bit SoftSpan DAC

Data Sheet

LTC2672-16DICE

FEATURES

- Per channel programmable output current ranges: 300 mA, 200 mA, 100 mA, 50 mA, 25 mA, 12.5 mA, 6.25 mA, and 3.125 mA
- Flexible 2.1 V to V_{CC} output supply voltages
- Flexible single- or dual-supply operation
- 0.6 V maximum dropout voltage guaranteed
- Separate voltage supply per output channel
- Internal switches to optional negative supply
- Full 16-bit resolution at all ranges
- Precision internal reference (10 ppm/°C typical V_{REF} temperature coefficient) or external reference
- Analog multiplexer monitors voltages and currents
- A/B toggle via SPI or dedicated pin
- 1.71 V to V_{CC} digital I/O supply voltage
- 32-pad bare die

APPLICATIONS

- Tunable lasers
- Semiconductor optical amplifier biasing
- Resistive heaters
- Current mode biasing

FUNCTIONAL BLOCK DIAGRAM

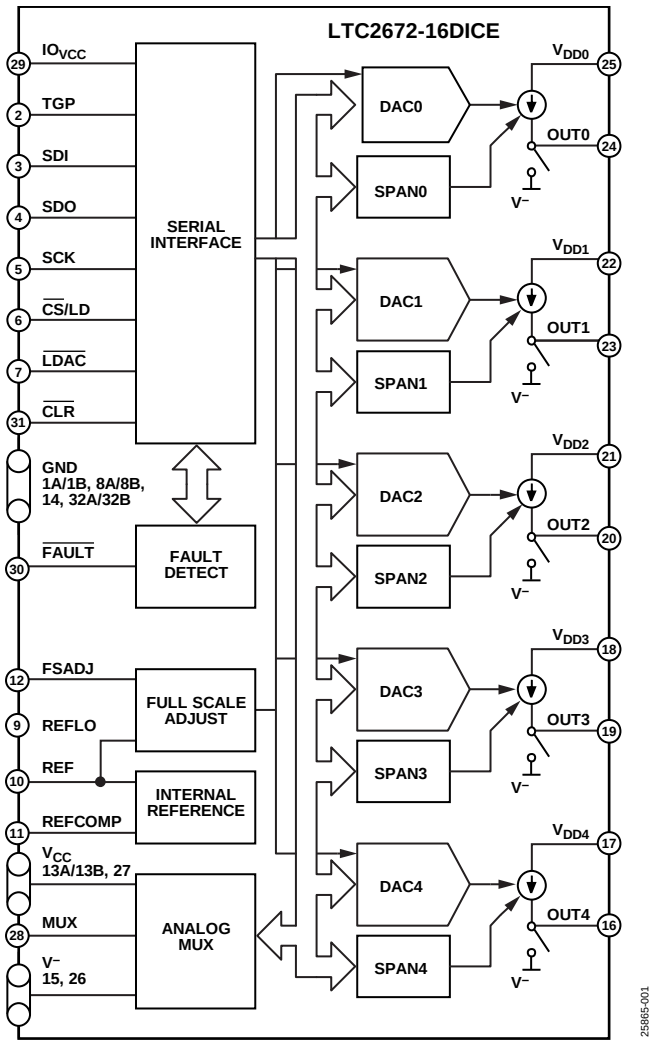

Figure 1.

GENERAL DESCRIPTION

The LTC2672-16DICE is a five-channel, 16-bit current source, digital-to-analog converter (DAC) that provides five high compliance current source outputs with guaranteed 0.6 V dropout at 200 mA. There are eight current ranges that are programmable per channel with full-scale outputs of up to 300 mA. The channels can be paralleled to allow either ultrafine adjustments of large currents or combined outputs of up to 1.5 A. A dedicated supply pin is provided for each output channel. Each channel can be operated from 2.1 V to V_{CC}, and internal switches allow any output to be pulled to the optional negative supply. The LTC2672-16DICE includes a precision integrated 1.25 V reference (10 ppm/°C typical), with the option to use an external reference. The serial peripheral interface (SPI) compatible, 3-wire serial interface operates on logic levels as low as 1.71 V.

Note than throughout this data sheet, multifunction pins, such as $\overline{CS}$/LD, are referred to by the entire pin name or by a single function of the pin.

The LTC2672-16DICE is available in a 32-pad bare die and is specified at room temperature. Additional application and technical information can be found in the LTC2672 data sheet.

Rev. 0 Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

4/2021—Revision 0: Initial Version

SPECIFICATIONS

Wafer level probe specification, ambient temperature only.

All specifications apply at 25°C, unless otherwise noted. Typical values are at T_J = 25°C, V_{CC} = IO_{VCC} = 5 V, V^- = −3.3 V, V_{DDx} = 5 V, FSADJ = V_{CC}, and reference output voltage (V_{REF}) = 1.25 V external, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE						
Resolution			16			Bits
Monotonicity		All ranges[1]	16			Bits
Differential Nonlinearity	DNL	All ranges[1]	−1	+0.45	+1	LSB
Integral Nonlinearity	INL	All ranges[1]	−64	+12	+64	LSB
Current Offset Error	I_{OS}	All current ranges[1]	−0.4	+0.1	+0.4	%FSR
I_{OS} Temperature Coefficient		All current ranges		10		ppm/°C
Gain Error	GE[2]	300 mA and 200 mA output current ranges	−0.9	+0.3	+0.9	%FSR
		100 mA, 50 mA, and 25 mA output current ranges	−1.2	+0.4	+1.2	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges	−1.5	+0.7	+1.5	%FSR
Gain Temperature Coefficient		FSADJ = V_{CC}		30		ppm/°C
Total Unadjusted Error	TUE[2]	300 mA and 200 mA output current ranges	−1.4	+0.4	+1.4	%FSR
		100 mA, 50 mA, and 25 mA output current ranges	−1.7	+0.5	+1.7	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges	−2	+0.8	+2	%FSR
Power Supply Rejection	PSR	Range = 100 mA, OUTx current (I_{OUTx}) = 50 mA				
		V_{CC} = 4.75 V to 5.25 V		0.5		LSB
		V_{DDx} = 2.85 V to 3.15 V		0.4		LSB
		V_{DDx} = 4.75 V to 5.25 V		0.7		LSB
		V^- = −3.25 V to −2.75 V		0.6		LSB
DC Crosstalk[3]		Result of a 200 mW change in dissipated power		0.1		%FSR
Dropout Voltage[4] (V_{DDx} − V_{OUTx}[5])	$V_{DROPOUT}$	200 mA range, (V_{DDx} − V^-) = 4.75 V		0.45	0.6	V
		200 mA range, (V_{DDx} − V^-) = 2.85 V		0.5	0.65	V
		300 mA range, (V_{DDx} − V^-) = 4.75 V		0.75		V
		300 mA range, (V_{DDx} − V^-) = 2.85 V		0.85	1.15	V
Off Mode Output Leakage Current[6]		800 Ω load to GND	−1	+0.1	+1	µA
OUTx Switch to V^- Resistance	$R_{PULLDOWN}$	Span code = 1000 binary, sinking 80 mA		8	12	Ω
AC PERFORMANCE		T_A = 25°C for all ac performance specifications				
Settling Time[7, 8]	t_{SET}					
Full-Scale Step 3.125 mA Range		±0.0015% (±1 LSB at 16 binary)		21.1		µs
		±0.024% (±1 LSB at 12 binary)		3.8		µs
145 mA to 155 mA Step 200 mA Range		±0.0015% (±1 LSB at 16 binary)		7.2		µs
		±0.024% (±1 LSB at 12 binary)		3.6		µs
Full-Scale Step 200 mA Range		±0.0015% (±1 LSB at 16 binary)		200		µs
		±0.024% (±1 LSB at 12 binary)		3.5		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Glitch Impulse		At midscale transition, 200 mA range, resistive load that connects the DAC output to GND (R_{LOAD}) = 4 Ω		1.0		nA × s
DAC to DAC Crosstalk[9]		100 mA to 200 mA step, R_{LOAD} = 15 Ω		230		pA × s
Noise Current	i_{NOISE}	Output current noise density internal reference, I_{OUTx} = 150 mA, R_{LOAD} = 4 Ω, load capacitance (C_{LOAD}) = 10 µF				
Frequency		1 kHz		12		nA/√Hz
		10 kHz		5		nA/√Hz
		100 kHz		0.5		nA/√Hz
		1 MHz		0.05		nA/√Hz
REFERENCE						
V_{REF}			1.248	1.250	1.252	V
V_{REF} Temperature Coefficient[10]				10		ppm/°C
V_{REF} Line Regulation		V_{CC} = 5 V ± 10%		50		µV/V
V_{REF} Short-Circuit Current		V_{CC} = 5.5 V, forcing output to GND		2.5		mA
REFCOMP Pin Short-Circuit Current		V_{CC} = 5.5 V, forcing output to GND		65		µA
V_{REF} Load Regulation		V_{CC} = 5 V, REF current (I_{REF}) = 100 µA sourcing		140		mV/mA
V_{REF} Output Voltage Noise Density		REFCOMP current ($C_{REFCOMP}$) = REFCOMP capacitance (C_{REF}) = 0.1 µF, f = 10 kHz		32		nV/√Hz
External Reference Input						
Current[11]				0.001	1	µA
Capacitance[11]				40		pF
Voltage[11]		REFCOMP pin is tied to GND	1.225		1.275	V
External Full-Scale Adjust Resistor[11]	R_{FSADJ}	R_{FSADJ} to GND	19	20	41	kΩ
POWER SUPPLY						
Analog Supply Voltage	V_{CC}		2.85		5.5	V
Digital Input and Output Supply Voltage	IO_{VCC}		1.71		V_{CC}	V
Negative Supply	V^-		−5.5		0	V
Output Supplies	V_{DDx}	200 mA range and below (relative to GND)	2.1		V_{CC}	V
		300 mA range and below (relative to GND)	2.4		V_{CC}	V
Output Supplies, Total Voltage[12]		Safe operating area (V_{DDx} relative to V^-)	2.85		9	V
V_{CC} Supply Current		All ranges (code = 0, all channels)		4	5.3	mA
IO_{VCC} Supply Current		All ranges (code = 0, all channels)		0.01	1	µA
V^- Supply Current		All ranges (code = 0, all channels)		7.5	11	mA
V_{DDx} Supply Current		All ranges (code = 0, per channel)		1.5	2.2	mA
		25 mA range (code = full-scale, per channel)[13]		28	32	mA
		200 mA range (code = full-scale, per channel)[13]		205	215	mA
V_{CC} Shutdown Current[14, 15]	I_{SLEEP}			50	500	µA
IO_{VCC} Shutdown Current[14, 15]				0.01	1	µA
V^- Shutdown Current[14, 15]				0.29	1.2	mA
V_{DDx} Shutdown Current[14, 15]				80	250	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MONITOR MULTIPLEXER						
MUX DC Output Impedance				15		kΩ
MUX Leakage Current		Monitor multiplexer disabled (high impedance)	−1	+0.1	+1	µA
MUX Output Voltage Range		Monitor multiplexer selected to OUT0 voltage to OUT4 voltage	V^-		V_{CC}	V
MUX Continuous Current[12]		T_A = 25°C (do not exceed)	−1		+1	mA

[1] Offset current is measured at Code 384 for the LTC2672-16DICE. Linearity is defined from Code 384 to Code 65,535 for the LTC2672-16DICE.
[2] For a full-scale current (I_{FS}) = 300 mA, load resistance (R_{LOAD}) = 10 Ω. For a I_{FS} = 200 mA, R_{LOAD} = 15 Ω. For a I_{FS} = 100 mA, R_{LOAD} = 30 Ω. For a I_{FS} = 50 mA, R_{LOAD} = 50 Ω. For a I_{FS} = 25 mA, R_{LOAD} = 100 Ω. For a I_{FS} = 12.5 mA, R_{LOAD} = 200 Ω. For a I_{FS} = 6.25 mA, R_{LOAD} = 400 Ω. For a I_{FS} = 3.125 mA, R_{LOAD} = 800 Ω.
[3] I_{FS} = 200 mA and R_{LOAD} = 15 Ω. DC crosstalk is measured with a 100 mA to 200 mA current step on all four aggressor channels. The total power dissipation change is 4 × 50 mW = 200 mW. The monitor channel is held at 3/4 × I_{FS} or 150 mA.
[4] Wafer probe testing is performed at output currents of up to 100 mA. Output currents above 100 mA are guaranteed by design and characterization.
[5] V_{OUTx} is the channel output (OUTx) voltage.
[6] The loads attached to the OUTx pins must be terminated to GND.
[7] V_{DDx} = 5 V (3.125 mA range), V_{DDx} = 3.6 V (200 mA range), and V^- = −3.3 V for all ranges. For large current output steps, internal thermal effects result in a final settling tail. In most cases, the tail is too small to affect settling to ±0.024%, but several milliseconds can be needed for full settling to the ±0.0015% level. For optimal results, set V_{DDx} as low as practicable for each channel to reduce power dissipation in the device. The listed results were obtained using the DC2903A evaluation board demonstration circuit with no additional heatsinks.
[8] Internal reference mode. The load is 15 Ω (200 mA range) or 800 Ω (3.125 mA range) terminated to GND.
[9] DAC to DAC crosstalk is the glitch that appears at the output of one DAC because of a 100 mA to 200 mA step change in an adjacent DAC channel. The measured DAC is at midscale (100 mA output current) in the 200 mA span range, with the internal reference, V_{DDx} = 5 V, V^- = −3.3 V.
[10] The temperature coefficient is calculated by first computing the ratio of the maximum change in the output voltage to the nominal output voltage, and then dividing the ratio by the specified temperature range.
[11] Guaranteed by design and not production tested.
[12] Stresses beyond those listed for extended periods can cause permanent damage to the device or affect device reliability and lifetime.
[13] Single channel at a specified output.
[14] V_{CC} = IO_{VCC} = 5 V, V_{DDx} = 5 V, and V^- = −3.3 V.
[15] Digital inputs are at 0 V or IO_{VCC}.

SPI COMMAND SEQUENCES

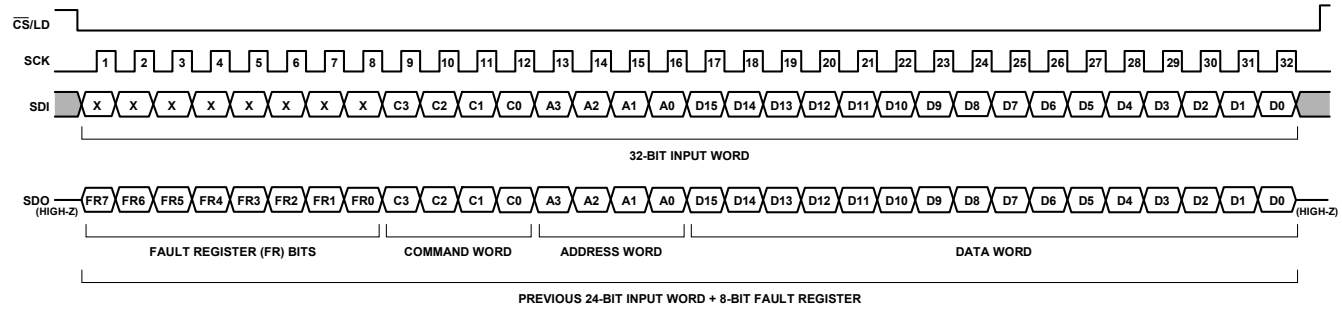

Figure 2. 32-Bit SPI Command Sequence

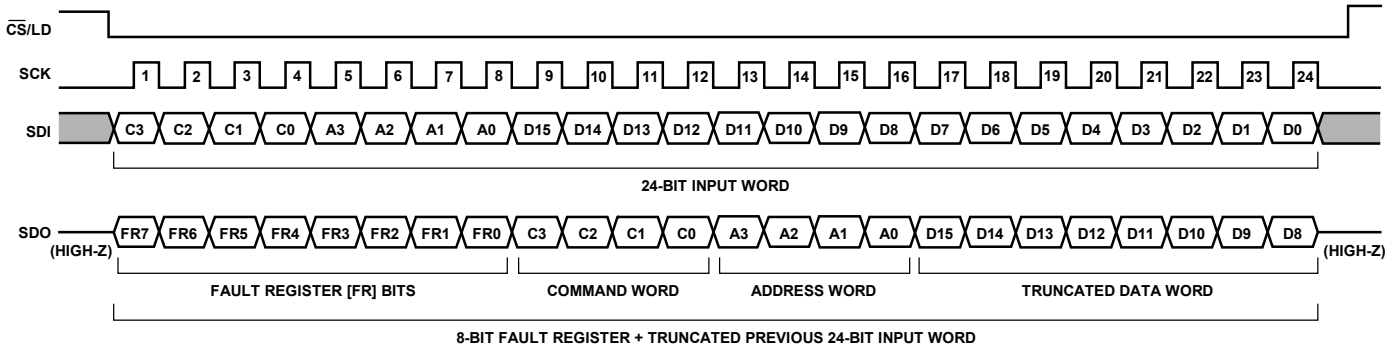

Figure 3. 24-Bit SPI Command Sequence

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC} to GND	−0.3 V to +6 V
IO_{VCC} to GND	−0.3 V to +6 V
V^- to GND	−6 V to +0.3 V
V_{DDx} to GND	−0.3 V to (V_{CC} + 0.3 V)
V_{DDx} to V^-	−0.3 V to +10 V
OUTx to GND	(V^- − 0.3 V) to (V_{DDx} + 0.3 V)
MUX	(V^- − 0.3 V) to (V_{CC} + 0.3 V)
REF, REFCOMP, FSADJ	−0.3 V to minimum (V_{CC} + 0.3 V or 6 V)
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$, TGP to GND	−0.3 V to +6 V
$\overline{FAULT}$ to GND	−0.3 V to +6 V
SDO	−0.3 V to minimum (V_{CC} + 0.3 V or 6 V)
Temperature	
Operational Range[1]	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction, T_{JMAX}	150°C

[1] Operating temperature range is valid for Analog Devices, Inc., packaged devices that are referenced on the LTC2672 data sheet. Die that are repackaged may operate to a different temperature range.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

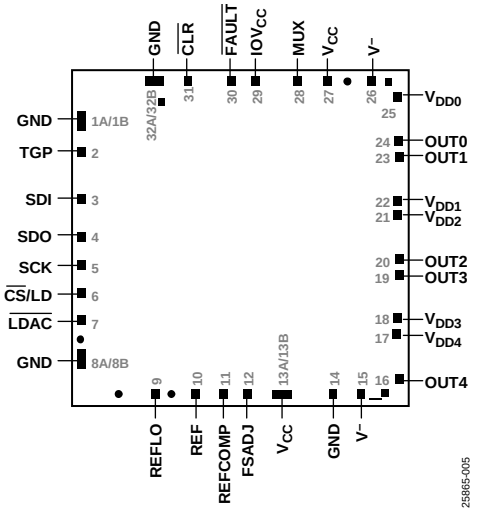

Figure 4. Pad Configuration

Table 3. Pad Function Descriptions

Pad No.	Mnemonic	X-Axis (µm)	Y-Axis (µm)	Pad Type[1]	Description
1A	GND	−1648.70	+1149.35	P (double)	Analog Ground
1B	GND	−1648.70	+1256.35	P (double)	Analog Ground
2	TGP	−1648.70	+882.50	DI (single)	Asynchronous Toggle Pin
3	SDI	−1648.70	+405.10	DI (single)	Serial Data Input
4	SDO	−1648.70	+16.45	DO (single)	Serial Data Output
5	SCK	−1648.70	−289.25	DI (single)	Serial Clock Input
6	$\overline{CS}$/LD	−1648.70	−573.05	DI (single)	Serial Interface Chip Select/Load Input
7	$\overline{LDAC}$	−1648.70	−852.85	DI (single)	Active Low Asynchronous DAC Update Pin
8A	GND	−1648.70	−1310.15	P (double)	Analog Ground
8B	GND	−1648.70	−1203.15	P (double)	Analog Ground
9	REFLO	−882.85	−1623.30	AI (single)	Reference Low
10	REF	−466.25	−1623.30	AI (single)	Reference Input/Output
11	REFCOMP	−181.05	−1623.30	AI (single)	Internal Reference Compensation Pin
12	FSADJ	+63.95	−1623.30	AI (single)	Full-Scale Current Adjust Pin
13A	V_{CC}	+381.30	−1623.30	P (double)	Analog Supply Voltage
13B	V_{CC}	+488.30	−1623.30	P (double)	Analog Supply Voltage
14	GND	+956.95	−1623.30	P (single)	Analog Ground
15	V^-	+1252.40	−1623.30	P (single)	Negative Supply Voltage
16	OUT4	+1648.70	−1468.00	AO (single)	DAC Analog Current Output 4
17	V_{DD4}	+1616.20	−997.10	P (single)	Output Supply 4
18	V_{DD3}	+1626.20	−838.30	P (single)	Output Supply 3
19	OUT3	+1648.70	−389.50	AO (single)	DAC Analog Current Output 3
20	OUT2	+1648.70	−226.30	AO (single)	DAC Analog Current Output 2
21	V_{DD2}	1626.20	222.50	P (single)	Output Supply 2
22	V_{DD1}	1626.20	381.30	P (single)	Output Supply 1
23	OUT1	1648.70	830.10	AO (single)	DAC Analog Current Output 1
24	OUT0	1637.85	993.30	AO (single)	DAC Analog Current Output 0
25	V_{DD0}	1626.20	1452.10	P (single)	Output Supply 0
26	V^-	1364.85	1623.30	P (single)	Negative Supply Voltage
27	V_{CC}	897.95	1623.30	P (single)	Analog Supply Voltage
28	MUX	593.70	1623.30	AO (single)	Analog Multiplexer Output
29	IO_{VCC}	158.10	1623.30	P (single)	Digital Input/Output Supply Voltage
30	$\overline{FAULT}$	−100.10	+1623.30	DO (single)	Active Low Fault Detection Pin

Pad No.	Mnemonic	X-Axis (µm)	Y-Axis (µm)	Pad Type[1]	Description
31	$\overline{CLR}$	−549.05	+1623.30	DI (single)	Active Low Asynchronous Clear Input
32A	GND	−943.80	+1623.30	P (double)	Ground
32B	GND	−836.80	+1623.30	P (double)	Ground

[1] P is power, DI is digital input, DO is digital output, AI is analog input, and AO is analog output.

OUTLINE DIMENSIONS

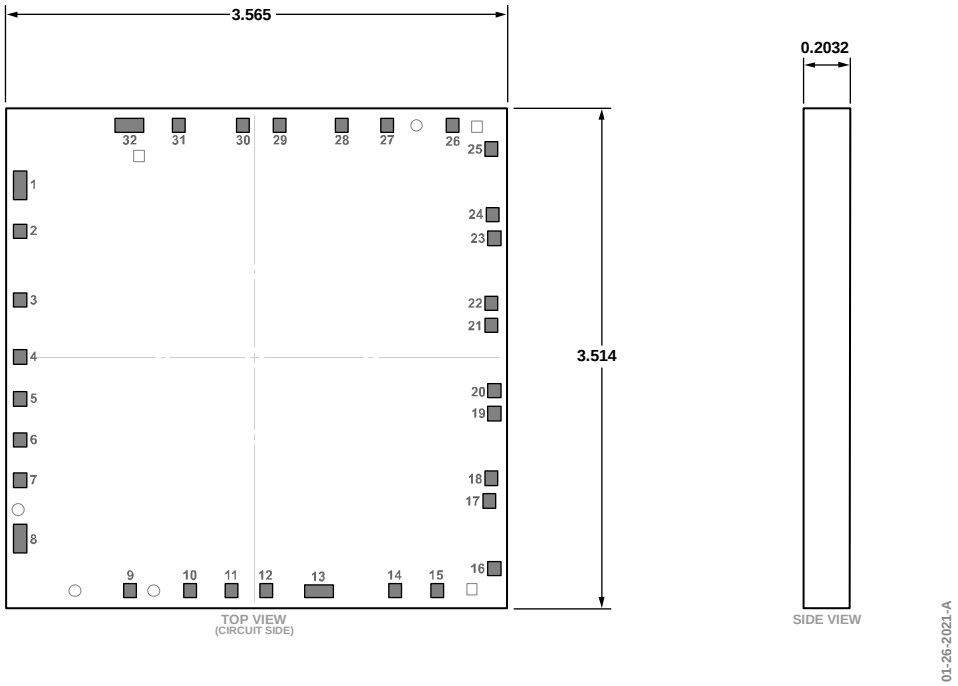

Figure 5. 32-Pad Bare Die [CHIP]
(C-32-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSESMBLY RECOMMENDATIONS

Table 4. Die Specifications

Parameter	Value	Unit
Scribe Line Width	70	µm
Die Size (Maximum)	3.565 (x) × 3.514 (y)	mm
Thickness	0.2032	mm
Bond Pads (Minimum Size)	82 × 82	µm
Bond Pad Composition	Aluminum (Al) 0.5% Copper (Cu) alloy	Not applicable
Backside	Bare Silicon (Si)	Not applicable
Passivation	Borophosphosilicate glass (BPSG) + Si Nitride (N)	Not applicable
Chip Size	3.495 (x) × 3.444 (y)	mm

Table 5. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Silver-filled epoxy
Bonding Method	Gold ball
Bonding Sequence	No special recommendations

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option
LTC2672-16DICE#6AM	0°C to 70°C	32-Pad Bare Die [CHIP]	C-32-1

[1] Operating temperature range is valid for Analog Devices, Inc., packaged devices that are referenced on the LTC2672 data sheet. Die that are repackaged may operate to a different temperature range.

NOTES

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