# 16-Channel, 16-Bit Voltage Output SoftSpan DAC

## FEATURES

- 16 independent SoftSpan DAC channels
- Independently programmable output ranges: 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V, ±15 V
- Full 16-bit resolution at all ranges
- Flexible single- or dual-supply operation
- Maximum INL error: ±3 LSB
- Precision 4.096 V reference, ±5 ppm/°C maximum
- A/B toggle or sinusoidal dither using up to 3 toggle pins
- Multiplexer for output voltage and load current sense
- Outputs drive ±20 mA guaranteed
- 6 mm × 6 mm, 40-lead LFCSP and 3.5 mm × 3.5 mm, 64-ball WLCSP

## APPLICATIONS

- Optical networking
- Instrumentation
- Data acquisition
- Automatic test equipment
- Process control and industrial automation

## FUNCTIONAL BLOCK DIAGRAM

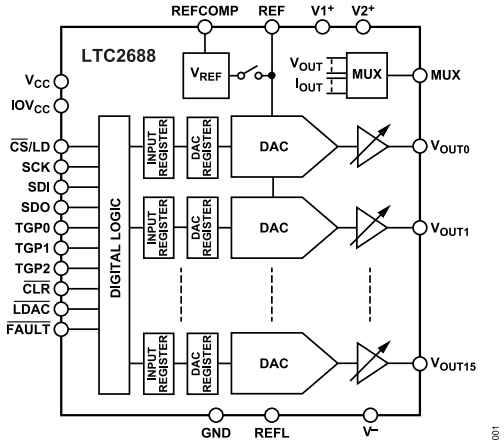


*Figure 1.*

## GENERAL DESCRIPTION

The LTC2688 is a 16-channel,16-bit, ±15 V digital-to-analog converter (DAC) with an integrated precision reference. The LTC2688 is guaranteed monotonic and has built in rail-to-rail output buffers that can source or sink up to 20 mA. This SoftSpan™ DAC offers five output ranges up to ±15 V. The range of each channel is independently programmable.

The internal 4.096 V precision reference sets the accuracy of the output voltage. An external reference can be used for additional range options. Three toggle pins support Input Register A and Input Register B toggle or sinusoidal dither at multiple frequencies. An analog multiplexer simplifies measurement of pin voltages, load currents, and junction temperature.

Programmable offset and gain registers improve the accuracy of the DAC outputs.

The serial peripheral interface (SPI) and MICROWIRE™-compatible, 3-wire serial interface operates on logic levels as low as 1.71 V and clock rates up to 50 MHz.

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**6/2021—Revision 0: Initial Version**

## SPECIFICATIONS

All specifications apply over the full operating temperature range, unless otherwise noted. Typical values are at $T_A$ = 25°C. $V_{CC}$ = 5 V, $IOV_{CC}$ = 5 V, $V1^+ = V2^+$ = 15 V, $V^-$ = −15 V, $V_{REF}$ = 4.096 V, $V_{OUT}$ unloaded, unless otherwise specified. For ±15 V range, $V1^+ = V2^+$ = 18 V, $V^-$ = −18 V.

***Table 1.***

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DC PERFORMANCE | | | | | | |
| Resolution | | | 16 | | | Bits |
| Monotonicity | | All ranges[1] | 16 | | | Bits |
| Differential Nonlinearity | DNL | All ranges[1] | | | ±1 | LSB |
| Integral Nonlinearity | INL | All ranges[1] | | | ±3 | LSB |
| Unipolar Offset Error | $V_{OS}$ | 0 V to 5 V range | | ±0.5 | ±2 | mV |
| | | 0 V to 10 V range | | ±1 | ±4 | mV |
| $V_{OS}$ Temperature Coefficient | | All unipolar ranges | | 1 | | ppm/°C |
| Single-Supply Zero-Scale Error | ZSE | All unipolar ranges, $V^-$ = GND | | 2 | 4 | mV |
| Bipolar Zero Error | BZE | All bipolar ranges | | | ±0.04 | % FSR[2] |
| BZE Temperature Coefficient | | All bipolar ranges | | 2 | | ppm/°C |
| Gain Error | GE | All ranges, external reference | | | ±0.08 | % FSR[2] |
| Gain Temperature Coefficient | | | | 2 | | ppm/°C |
| Output Voltage Swing | $V_{OUT}$ | To $V^-$ (unloaded) | | $V^-$ + 0.004 | | V |
| | | To $Vx^+$ (unloaded) | | $Vx^+$ − 0.004 | | V |
| | | To $V^-$ (−20 mA ≤ output current ($I_{OUT}$) ≤ +20 mA), ±15 V range | | | $V^-$ + 2.2 | V |
| | | To $Vx^+$ (−20 mA ≤ $I_{OUT}$ ≤ +20 mA), ±15 V range | $Vx^+$ − 2.2 | | | V |
| Power Supply Rejection | PSR | $V_{CC}$ = 5 V ± 5% | | −80 | | dB |
| | | $Vx^+/V^-$ = 15 V ± 5% | | −80 | | dB |
| Load Regulation | | −20 mA ≤ $I_{OUT}$ ≤ +20 mA, $Vx^+$ = +17.2 V, $V^-$ = −17.2 V, ±15 V range | | 70 | 150 | µV/mA |
| DC Crosstalk[3], 0 V to 5 V Range | | Due to full-scale output change | | ±2 | | µV |
| | | Due to load current change | | ±1 | | µV/mA |
| | | Due to powering down (per channel) | | ±4 | | µV |
| $Vx^+/V^-$ Short-Circuit Output Current[4], ±15 V Output Range | $I_{SC}$ | Negative full scale, forcing output to GND | −41 | | | mA |
| | | Positive full scale, forcing output to GND | | | 41 | mA |
| REFERENCE | | | | | | |
| Reference Output Voltage[5] | | | 4.094 | 4.096 | 4.098 | V |
| | | $T_A = T_{MIN}$ to $T_{MAX}$ | 4.092 | 4.096 | 4.100 | V |
| Reference Temperature Coefficient[6] | | | | | | |
| LFCSP Package | | | | ±2 | ±5 | ppm/°C |
| WLCSP Package | | | | ±5 | | ppm/°C |
| Line Regulation | | $V_{CC}$ ± 5% | | −80 | | dB |
| Short-Circuit Current | | Forcing output to GND | | 0.1 | | mA |
| REFCOMP Pin Short-Circuit Current | | Forcing output to GND | | 10 | | µA |
| Load Regulation | | $I_{OUT}$ = 1 µA | | 320 | | mV/mA |
| Output Voltage Noise Density | | REFCOMP, capacitor ($C_{REFCOMP}$) = REF capacitor ($C_{REF}$) = 0.1 µF, at f = 10 kHz | | 32 | | nV/√Hz |
| REFERENCE INPUT | | | | | | |
| Range | | External reference mode[7] | 2.0 | | $V_{CC}$ − 0.6 | V |
| Current | | | | 10 | 15 | µA |
| Capacitance | | | | 8 | | pF |
| POWER SUPPLY | | | | | | |

## SPECIFICATIONS

*Table 1.*

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Analog Supply Voltage | $V_{CC}$ | | 4.75 | | 5.25 | V |
| Analog Positive Supply | $V1^+$ | | $V_{CC}$ – 0.3 | | $V^-$ + 42 | V |
| | $V2^+$ | | $V_{CC}$ – 0.3 | | $V1^+$ + 0.3 | V |
| Analog Negative Supply | $V^-$ | | –21 | | 0 | V |
| Digital Input/Output (I/O) Supply Voltage | $IOV_{CC}$ | | 1.71 | | $V_{CC}$ + 0.3 | V |
| Supply Current | | | | | | |
| $V_{CC}$[8] | $IV_{CC}$ | $V_{CC}$ = 5 V; 0 V to 5 V range | | 21.9 | | mA |
| | | $V_{CC}$ = 5 V; 0 V to 10 V range | | 22.3 | | mA |
| | | $V_{CC}$ = 5 V; ±5 V range | | 25.6 | | mA |
| | | $V_{CC}$ = 5 V; ±10 V range | | 29.6 | | mA |
| | | $V_{CC}$ = 5 V; ±15 V range | | 33.6 | 37.0 | mA |
| $Vx^+/V^-$[9] | $I_S$ | $Vx^+/V^-$ = ±15 V; 0 V to 5 V range | | 6.4 | | mA |
| | | $Vx^+/V^-$ = ±15 V; 0 V to 10 V range | | 6.4 | | mA |
| | | $Vx^+/V^-$ = ±15 V; ±5 V range | | 8.3 | | mA |
| | | $Vx^+/V^-$ = ±15 V; ±10 V range | | 10.8 | | mA |
| | | $Vx^+/V^-$ = ±15 V; ±15 V range | | 13 | 15 | mA |
| $IOV_{CC}$ | $I_{IOVCC}$ | $IOV_{CC}$ = 5 V, digital inputs at $IOV_{CC}$ or GND | | 0.05 | 1 | µA |
| Shutdown Supply Current | | | | | | |
| $V_{CC}$ | | $V_{CC}$ = 5 V | | 20 | | µA |
| $V^+$ | | $V^+/V^-$ = ±15 V | | 30 | | µA |
| $V^-$ | | $V^+/V^-$ = ±15 V | | −30 | | µA |
| ANALOG MUX | | | | | | |
| MUX DC Output Impedance | | | | 3.5 | | kΩ |
| MUX Leakage Current | | | | | 1 | µA |
| MUX Output Voltage Range | | | $V^-$ | | $V1^+$ – 1.4 | V |
| MUX Continuous Current[10] | | | | | 0.2 | mA |
| Junction Temperature Sense Slope | | | | 7.95 | | mV/°C |
| Junction Temperature Accuracy | | | | ±5 | | °C |
| AC PERFORMANCE | | | | | | |
| Settling Time | $t_{SETTLE}$ | ±0.0015% (±1 LSB at 16 bits) | | | | |
| 0 V to 5 V Range, ±5 V Step | | | | <10 | | µs |
| 0 V to 10 V Range or ±5 V Range, ±10 V Step | | | | <11 | | µs |
| ±10 V Range, ±20 V Step | | | | <20 | | µs |
| ±15 V Range, ±30 V Step | | | | <28 | | µs |
| Voltage Output Slew Rate | SR | | | >3.5 | | V/µs |
| Capacitive Load Driving | | | | 1000 | | pF |
| Glitch Impulse[11] | | At midscale transition, 0 V to 5 V range | | 7 | | nV-sec |
| DAC to DAC Crosstalk[12] | | Due to full-scale output change, 0 V to 5 V range | | 1 | | nV-sec |
| Output Noise Spectral Density | $e_n$ | 0 V to 5 V output range, internal reference | | | | |
| | | At f = 1 kHz | | 60 | | nV/√Hz |
| | | At f = 10 kHz | | 45 | | nV/√Hz |
| | | 0.1 Hz to 10 Hz | | 1.7 | | µV rms |
| | | 0.1 Hz to 200 kHz | | 30 | | µV rms |
| DIGITAL INPUT/OUTPUT (I/O) | | | | | | |
| Digital Output High Voltage | $V_{OH}$ | SDO pin, load current = −100 µA | $IOV_{CC}$ − 0.2 | | | V |
| Digital Output Low Voltage | $V_{OL}$ | SDO pin, load current = 100 µA | | | 0.2 | V |
| | | $\overline{FAULT}$ pin, load current = 100 µA | | | 0.2 | V |

## SPECIFICATIONS

*Table 1.*

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital High-Z Output Leakage | $I_{OZ}$ | SDO pin leakage current ($\overline{CS}$/LD high) | | | ±1 | µA |
| | | $\overline{FAULT}$ pin leakage current (not asserted) | | | 1 | µA |
| Digital Input Leakage | $I_{LK}$ | $V_{IN}$ = GND to $IOV_{CC}$ | | | ±1 | µA |
| Digital Input Capacitance[10] | $C_{IN}$ | | | | 8 | pF |
| $IOV_{CC}$ = 2.7 V to $V_{CC}$ | | | | | | |
| Digital Input High Voltage | $V_{IH}$ | | 0.8 × $IOV_{CC}$ | | | V |
| Digital Input Low Voltage | $V_{IL}$ | | | | 0.5 | V |
| $IOV_{CC}$ = 1.71 V to 2.7 V | | | | | | |
| Digital Input High Voltage | $V_{IH}$ | | 0.8 × $IOV_{CC}$ | | | V |
| Digital Input Low Voltage | $V_{IL}$ | | | | 0.3 | V |

[1] Output ranges include 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V, and ±15 V.

[2] FSR is full-scale range.

[3] DC crosstalk is measured using the internal reference. The conditions of one DAC channel are changed as specified, and the output of an adjacent channel (at midscale) is measured before and after the change.

[4] This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

[5] Reference voltage output is production tested using a socket. Mechanical stress caused by soldering parts to a printed circuit board may cause the output voltage to shift and temperature coefficient to change. See the Printed Circuit Board Layout section.

[6] Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

[7] GE, BZE, and $V_{OS}$ specifications can degrade for reference input voltages less than 3 V. See Figure 5, Figure 6, and Figure 12 in the Typical Performance Characteristics section.

[8] Internal reference on. $IV_{CC}$ measured with all channels at zero scale for unipolar ranges and negative full scale for bipolar ranges.

[9] $Vx^+$ current ($I_{V^+}$) is measured with all channels at full scale. $V^-$ current ($I_{V^-}$) is measured with all channels at zero scale for unipolar ranges and negative full scale for bipolar ranges.

[10] Guaranteed by design; not production tested.

[11] 0 V to 5 V range, internal reference mode. DAC is stepped ±1 LSB between half scale and half scale – 1 LSB. Load is 2 kΩ in parallel with 200 pF to GND.

[12] DAC to DAC crosstalk is the glitch that appears at the output of one DAC due to full-scale change at the output of another DAC. 0 V to 5 V range with internal reference. The measured DAC is at midscale.

## TIMING CHARACTERISTICS

All specifications apply over the full operating temperature range, unless otherwise noted. Typical values are at $T_A$ = 25°C. $V_{CC}$ = 4.75 V to 5.25 V, $IOV_{CC}$ = 1.71 V to $V_{CC}$. $C_{LOAD}$ is load capacitance. $IOV_{CC}$ = 2.7 V to $V_{CC}$, unless otherwise noted. See Figure 2.

*Table 2.*

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_1$ | SDI valid to SCK setup | 3 | | | ns |
| $t_2$ | SDI valid to SCK hold | 3 | | | ns |
| $t_3$ | SCK high time | 6 | | | ns |
| $t_4$ | SCK low time | 6 | | | ns |
| $t_5$ | $\overline{CS}$/LD pulse width | 8 | | | ns |
| $t_6$ | LSB SCK high to $\overline{CS}$/LD high | 5 | | | ns |
| $t_7$ | $\overline{CS}$/LD low to SCK high | 5 | | | ns |
| $t_8$ | SDO propagation delay from SCK falling edge, $C_{LOAD}$ = 10 pF, $IOV_{CC}$ = 2.7 V to 5.25 V | | | 25 | ns |
| | SDO propagation delay from SCK falling edge, $C_{LOAD}$ = 10 pF, $IOV_{CC}$ = 1.7 1 V to 2.7 V | | | 60 | ns |
| $t_9$ | $\overline{CLR}$ pulse width | 8 | | | ns |
| $t_{10}$ | $\overline{CS}$/LD high to SCK positive edge | 4 | | | ns |

## SPECIFICATIONS

*Table 2.*

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{11}$ | $\overline{LDAC}$ pulse width | 8 | | | ns |
| $t_{12}$ | $\overline{CS}$/LD high to $\overline{LDAC}$ high or low transition[1] | 8 | | | ns |
| $f_{SCK}$ | SCK frequency | | | 50 | MHz |
| $t_{13}$ | TGPx high time | | 0.25 | | µs |
| $t_{14}$ | TGPx low time[2] | | 0.25 | | µs |

[1] Value of $t_{12}$ is not valid for write code to all DAC channels. For write code to all DAC channels, the typical value of $t_{12}$ is 320 ns.

[2] Guaranteed by design but not production tested.

### Timing Diagram

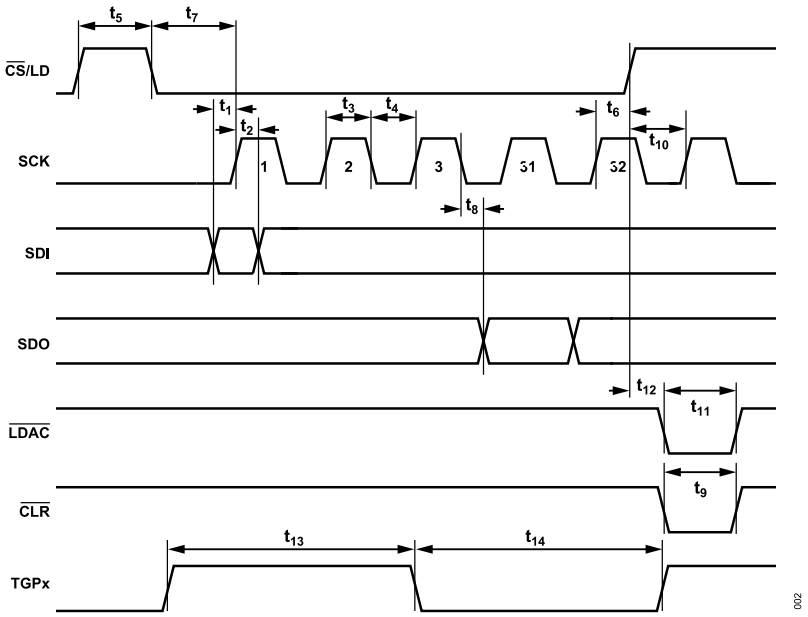


*Figure 2. Serial Interface Timing Diagram*

## ABSOLUTE MAXIMUM RATINGS

*Table 3.*

| Parameter | Rating |
|---|---|
| $V_{CC}$ to GND | −0.3 V to +6 V |
| $IOV_{CC}$ to GND | −0.3 V to +6 V |
| REFL to GND | −0.3 V to +0.3V |
| $V1^+$ to GND | −0.3 V to +22 V |
| $V2^+$ to GND | −0.3 V to $V1^+$, or −0.3 V to +22 V (whichever is smaller) |
| $V^-$ to GND | −22V to +0.3 V |
| $V1^+$ to $V^-$ | −0.3 V to +44 V |
| $V2^+$ to $V^-$ | −0.3 V to +44 V |
| Mux Continuous DC Output Current | ±200 µA |
| $\overline{CS}$/LD, SCK, SDI | −0.3 V to $IOV_{CC}$ + 0.3 V or −0.3 V to +6 V (whichever is smaller) |
| $\overline{LDAC}$, $\overline{CLR}$, $\overline{FAULT}$ to GND | −0.3 V to $IOV_{CC}$ + 0.3 V or −0.3 V to +6 V (whichever is smaller) |
| TGP0, TGP1, TGP2 to GND | −0.3 V to $IOV_{CC}$ + 0.3 V or −0.3 V to +6 V (whichever is smaller) |
| $V_{OUT0}$ to $V_{OUT15}$, MUX to GND | $V^-$ − 0.3 V to $Vx^+$ + 0.3 V, or ±22 V |
| REF, REFCOMP | −0.3 V to $V_{CC}$ + 0.3 V or −0.3 V to 6 V (whichever is smaller) |
| SDO | −0.3 V to $IOV_{CC}$ + 0.3 V or −0.3 V to 6 V (whichever is smaller) |
| Temperature | |
| Operating Range | |
| LTC2688C | 0°C to 70°C |
| LTC2688I | −40°C to +85°C |
| LTC2688H | −40°C to +125°C |
| Storage Range | −65°C to +150°C |
| Junction, $T_{JMAX}$ | 150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$ is the natural convection junction to ambient thermal resistance measured in a one-cubic foot sealed enclosure. $\theta_{JC}$ is the junction to case thermal resistance.

*Table 4. Thermal Resistance*

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 05-08-1728[1] | 33 | 2 | °C/W |
| CB-64-5 | 32.2 | 0.2 | °C/W |

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

### ESD Ratings for LTC2688

*Table 5. LTC2688, 40-Lead LFCSP and 64-Ball WLCSP*

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | 3500 | 2 |
| FICDM | 500 | C4 |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

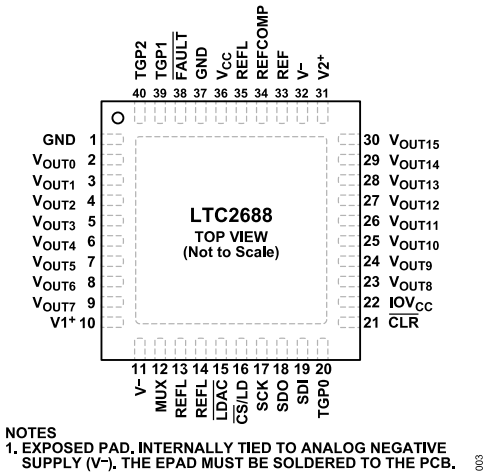


*Figure 3. LFCSP Pin Configuration*

*Table 6. Pin Function Descriptions—LFCSP*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 37 | GND | Analog Ground. Tie GND to a clean analog ground plane. |
| 2 to 9, 23 to 30 | $V_{OUT0}$ to $V_{OUT15}$ | DAC Analog Voltage Outputs. |
| 10 | $V1^+$ | Analog Positive Supply for the $V_{OUT0}$ to $V_{OUT7}$ DAC Outputs. Bypass $V1^+$ to GND with a 1 µF capacitor. $V1^+$ must be greater than or equal to $V2^+$. |
| 11, 32 | $V^-$ | Analog Negative Supply. Bypass $V^-$ to GND with a 1 µF capacitor unless $V^-$ is connected to GND. |
| 12 | MUX | Analog Multiplexer Output. Any of the 16 DAC output pin voltages, current load sense voltages ($V_{SENSE}$), and junction temperatures can be monitored by measuring the voltage at the MUX pin. When the mux is disabled, the MUX pin becomes high impedance. A full listing of available mux functions is given in Table 22. |
| 13, 14, 35 | REFL | Reference Low Pins. Signal ground for all DAC channels and internal reference. Tie the REFL pins to a clean analog ground plane. |
| 15 | $\overline{LDAC}$ | Active Low Asynchronous DAC Update Pin. When $\overline{CS}$/LD is high, a falling edge on $\overline{LDAC}$ updates all DAC registers with the contents of the input registers. When $\overline{LDAC}$ is low, a rising edge on $\overline{CS}$/LD similarly updates all DAC registers. Logic levels are determined by $IOV_{CC}$. If the $\overline{LDAC}$ pin is not used, tie it high to $IOV_{CC}$. Updates can then be performed through SPI commands. |
| 16 | $\overline{CS}$/LD | Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 8 and Table 9) is executed. Logic levels are determined by $IOV_{CC}$. |
| 17 | SCK | Serial Interface Clock Input. Logic levels are determined by $IOV_{CC}$. |
| 18 | SDO | Serial Interface Data Output. Data is clocked out onto SDO by the falling edge of SCK. SDO is high impedance when $\overline{CS}$/LD is high. Logic levels are determined by $IOV_{CC}$. |
| 19 | SDI | Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2688 accepts input word lengths of 24 bits or 32 bits. Logic levels are determined by $IOV_{CC}$. |
| 20, 39, 40 | TGP0, TGP1, TGP2 | Asynchronous Toggle and Sinusoidal Dither Multifunctional Pins. In toggle mode, a falling edge updates the DAC register with data from Input Register A and a rising edge updates the DAC register with data from Input Register B. In sinusoidal dither mode, the toggle pins function as dither clock inputs. DAC outputs update on the rising edge. Toggle and dither operations only affect those DAC channels with their toggle/dither enable bit (ENx) set to 1. When neither toggle nor dither operations are used, tie the TGPx pins to GND, and set EN to 0. Logic levels are determined by $IOV_{CC}$. |
| 21 | $\overline{CLR}$ | Active Low Asynchronous Clear Input. A logic low at this level-triggered input clears the device to zero-scale code and a 0 V to 5 V span range. The control registers are cleared to default values. Logic levels are determined by $IOV_{CC}$. |
| 22 | $IOV_{CC}$ | Digital Input/Output Supply Voltage. 1.71 V ≤ $IOV_{CC}$ ≤ $V_{CC}$ + 0.3 V. Bypass $IOV_{CC}$ to GND with a 0.1 µF capacitor. |
| 31 | $V2^+$ | Analog Positive Supply for the $V_{OUT8}$ to $V_{OUT15}$ DAC Outputs. Bypass the $V2^+$ pin to GND with a 1 µF capacitor. $V2^+$ must be less than or equal to $V1^+$. |
| 33 | REF | Reference Input/Output. The voltage at the REF pin sets the full-scale range of all channels. By default, the internal reference is routed to this pin. The REF pin must be buffered when driving external dc load currents. When set to external reference mode, the internal reference is disconnected, and the REF pin becomes a high impedance input to which a precision external reference can be applied. For low noise and reference stability, tie a capacitor from the REF pin to GND. The value must be |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

*Table 6. Pin Function Descriptions—LFCSP*

| Pin No. | Mnemonic | Description |
|---|---|---|
| | | less than the capacitance at the REFCOMP pin. In external reference mode, the allowable reference input voltage range is 2.0 V to $V_{CC}$ − 0.6 V. |
| 34 | REFCOMP | Internal Reference Compensation. For low noise and reference stability, tie REFCOMP to a 0.1 µF capacitor to GND. Tying REFCOMP to GND causes the device to power up with the internal reference disabled, allowing the use of an external reference at startup. |
| 36 | $V_{CC}$ | Analog Supply Voltage Input. 4.75 V ≤ $V_{CC}$ ≤ 5.25 V. Bypass $V_{CC}$ to GND with a 1 µF capacitor. |
| 38 | $\overline{FAULT}$ | Fault Indicator. $\overline{FAULT}$ is an open-drain, N channel output that pulls low when a fault condition occurs. A fault condition is detected when the junction temperature exceeds 160°C or when a SPI transaction error occurs. The $\overline{FAULT}$ pin is released on the next $\overline{CS}$/LD rising edge. A pull-up resistor of ≥10 kΩ is recommended. |
| 41 | EPAD | Exposed Pad. Internally tied to analog negative supply ($V^-$). The EPAD must be soldered to the PCB. |

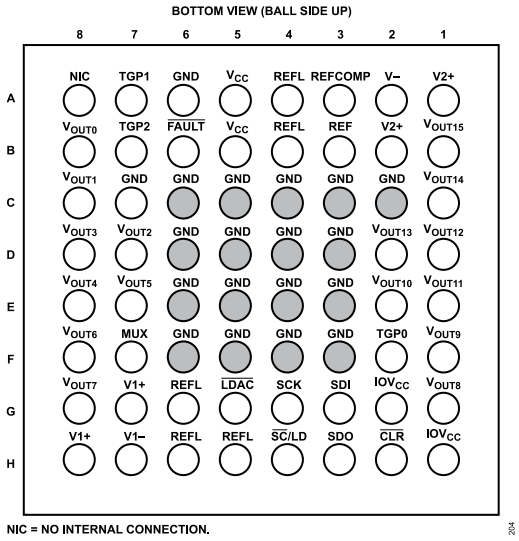


*Figure 4. WLCSP Pin Configuration*

*Table 7. Pin Function Descriptions—WLCSP*

| Pin No. | Mnemonic | Description |
|---|---|---|
| A1, B2 | $V2^+$ | Analog Positive Supply for the $V_{OUT8}$ to $V_{OUT15}$ DAC Outputs. Bypass the $V2^+$ pin to GND with a 1 µF capacitor. $V2^+$ must be less than or equal to $V1^+$. |
| A2, H7 | $V^-$ | Analog Negative Supply. Bypass $V^-$ to GND with a 1 µF capacitor unless $V^-$ is connected to GND. |
| A3 | REFCOMP | Internal Reference Compensation. For low noise and reference stability, tie REFCOMP to a 0.1 µF capacitor to GND. Tying REFCOMP to GND causes the device to power up with the internal reference disabled, allowing the use of an external reference at startup. |
| A4, B4, G6, H5, H6 | REFL | Reference Low Pins. Signal ground for all DAC channels and internal reference. Tie the REFL pins to a clean analog ground plane. |
| A5, B5 | $V_{CC}$ | Analog Supply Voltage Input. 4.75 V ≤ $V_{CC}$ ≤ 5.25 V. Bypass $V_{CC}$ to GND with a 1 µF capacitor. |
| A6, C2, C3, C4, C5, C6, C7, D3, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6 | GND | Analog Ground. Tie GND to a clean analog ground plane. |
| A7, B7, F2 | TGP0, TGP1, TGP2 | Asynchronous Toggle and Sinusoidal Dither Multifunctional Pins. In toggle mode, a falling edge updates the DAC register with data from Input Register A and a rising edge updates the DAC register with data from Input Register B. In sinusoidal dither mode, the toggle pins function as dither clock inputs. DAC outputs update on the rising edge. Toggle and dither operations only affect those DAC channels with their toggle/dither enable bit (ENx) set to 1. When neither toggle nor dither operations are used, tie the TGPx pins to GND, and set EN to 0. Logic levels are determined by $IOV_{CC}$. |
| A8 | NC | |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

*Table 7. Pin Function Descriptions—WLCSP*

| Pin No. | Mnemonic | Description |
|---|---|---|
| B8, C8, D7, D8, E8, E7, F8, G8, G1, F1, E2, E1, D1, D2, C1, B1 | $V_{OUT0}$ to $V_{OUT15}$ | DAC Analog Voltage Outputs. |
| B3 | REF | Reference Input/Output. The voltage at the REF pin sets the full-scale range of all channels. By default, the internal reference is routed to this pin. The REF pin must be buffered when driving external dc load currents. When set to external reference mode, the internal reference is disconnected, and the REF pin becomes a high impedance input to which a precision external reference can be applied. For low noise and reference stability, tie a capacitor from the REF pin to GND. The value must be less than the capacitance at the REFCOMP pin. In external reference mode, the allowable reference input voltage range is 2.0 V to $V_{CC}$ − 0.6 V. |
| B6 | $\overline{FAULT}$ | Fault Indicator. $\overline{FAULT}$ is an open-drain, N channel output that pulls low when a fault condition occurs. A fault condition is detected when the junction temperature exceeds 160°C or when a SPI transaction error occurs. The $\overline{FAULT}$ pin is released on the next $\overline{CS}$/LD rising edge. A pull-up resistor of ≥10 kΩ is recommended. |
| F7 | MUX | Analog Multiplexer Output. Any of the 16 DAC output pin voltages, current load sense voltages ($V_{SENSE}$), and junction temperatures can be monitored by measuring the voltage at the MUX pin. When the mux is disabled, the MUX pin becomes high impedance. A full listing of available mux functions is given in Table 22. |
| G7, H8 | $V1^+$ | Analog Positive Supply for the $V_{OUT0}$ to $V_{OUT7}$ DAC Outputs. Bypass $V1^+$ to GND with a 1 µF capacitor. $V1^+$ must be greater than or equal to $V2^+$. |
| G2, H1 | $IOV_{CC}$ | Digital Input/Output Supply Voltage. 1.71 V ≤ $IOV_{CC}$ ≤ $V_{CC}$ + 0.3 V. Bypass $IOV_{CC}$ to GND with a 0.1 µF capacitor. |
| G3 | SDI | Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2688 accepts input word lengths of 24 bits or 32 bits. Logic levels are determined by $IOV_{CC}$. |
| G4 | SCK | Serial Interface Clock Input. Logic levels are determined by $IOV_{CC}$. |
| G5 | $\overline{LDAC}$ | Active Low Asynchronous DAC Update Pin. When $\overline{CS}$/LD is high, a falling edge on $\overline{LDAC}$ updates all DAC registers with the contents of the input registers. When $\overline{LDAC}$ is low, a rising edge on $\overline{CS}$/LD similarly updates all DAC registers. Logic levels are determined by $IOV_{CC}$. If the $\overline{LDAC}$ pin is not used, tie it high to $IOV_{CC}$. Updates can then be performed through SPI commands. |
| H2 | $\overline{CLR}$ | Active Low Asynchronous Clear Input. A logic low at this level triggered input clears the device to zero-scale code and a 0 V to 5 V span range. The control registers are cleared to default values. Logic levels are determined by $IOV_{CC}$. |
| H3 | SDO | Serial Interface Data Output. Data is clocked out onto SDO by the falling edge of SCK. SDO is high impedance when $\overline{CS}$/LD is high. Logic levels are determined by $IOV_{CC}$. |
| H4 | $\overline{CS}$/LD | Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 8 and Table 9) is executed. Logic levels are determined by $IOV_{CC}$. |

## TYPICAL PERFORMANCE CHARACTERISTICS

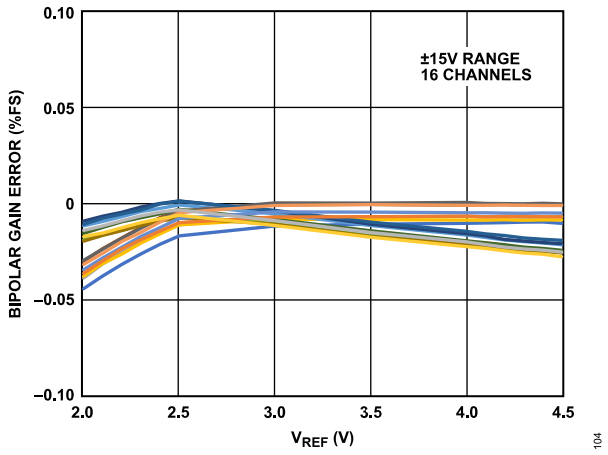


*Figure 5. Bipolar Gain Error vs. $V_{REF}$*

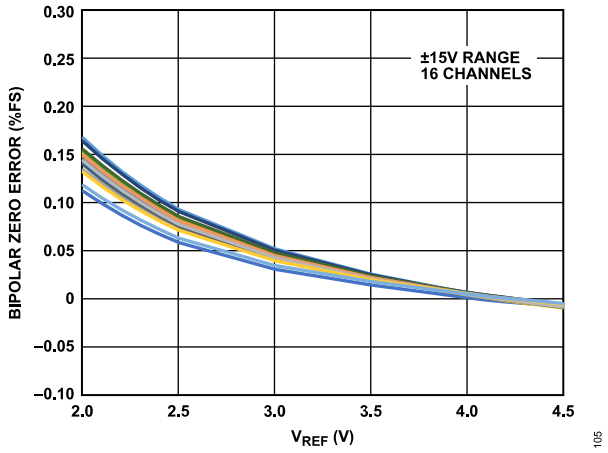


*Figure 6. Bipolar Zero Error vs. $V_{REF}$*

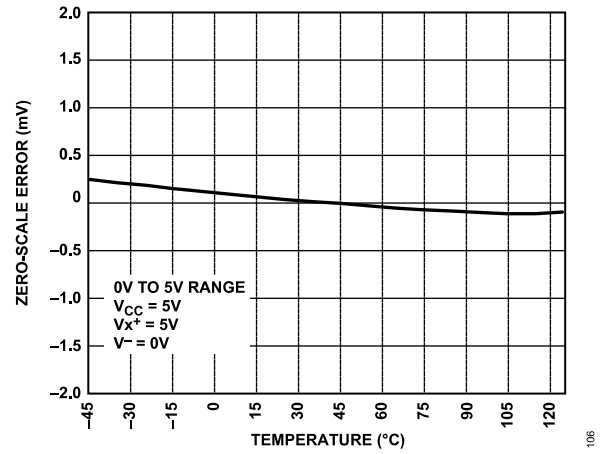


*Figure 7. Zero-Scale Error (ZSE) vs. Temperature*

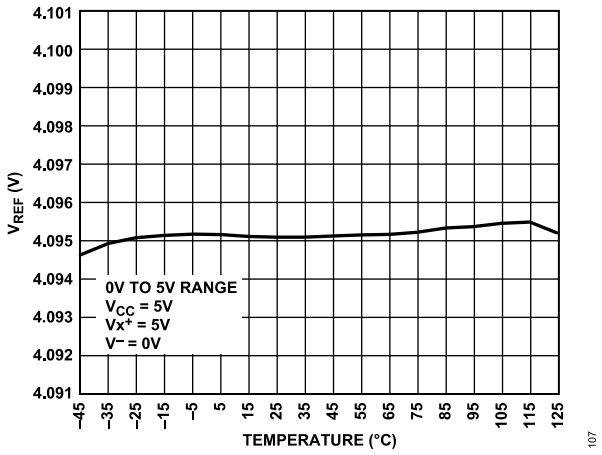


*Figure 8. $V_{REF}$ vs. Temperature*

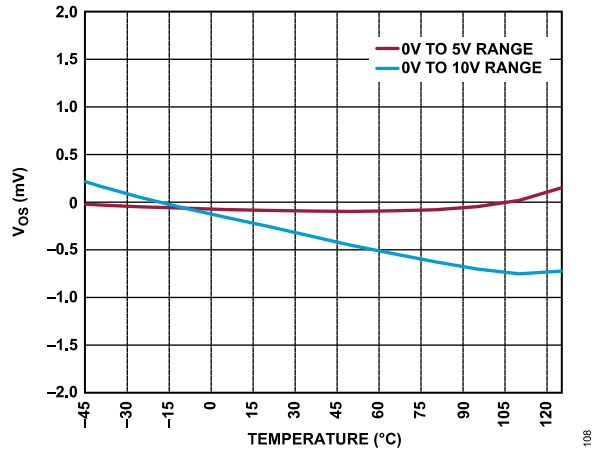


*Figure 9. Unipolar Offset Error ($V_{OS}$) vs. Temperature*

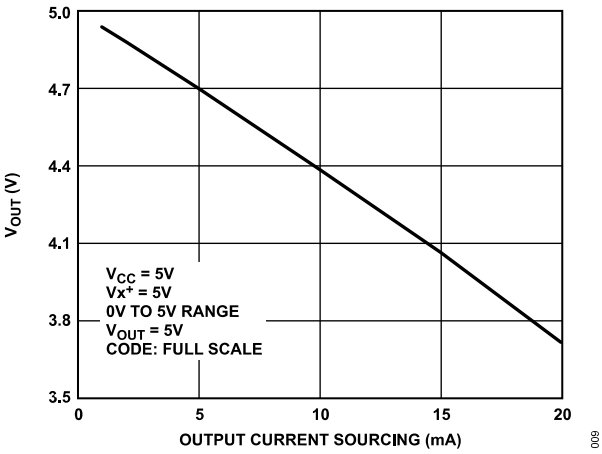


*Figure 10. $V_{OUT}$ vs. Output Current Sourcing*

## TYPICAL PERFORMANCE CHARACTERISTICS

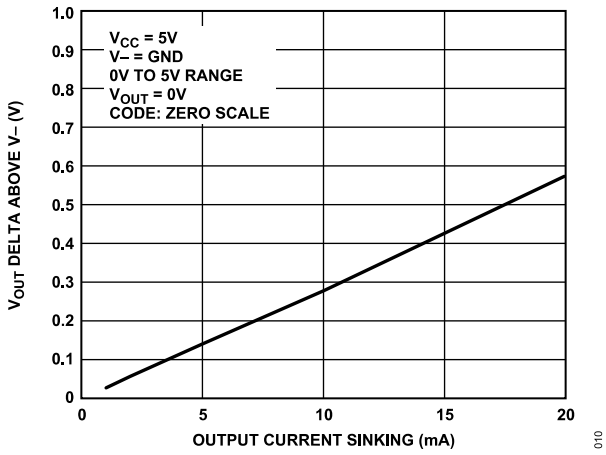


*Figure 11. $V_{OUT}$ Delta Above $V^-$ vs. Output Current Sinking*

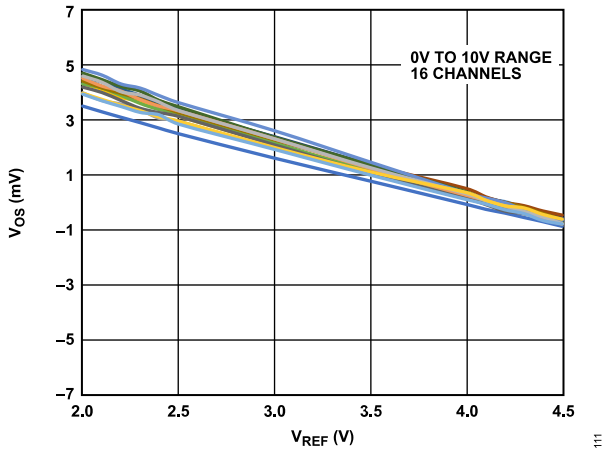


*Figure 12. $V_{OS}$ vs. $V_{REF}$*

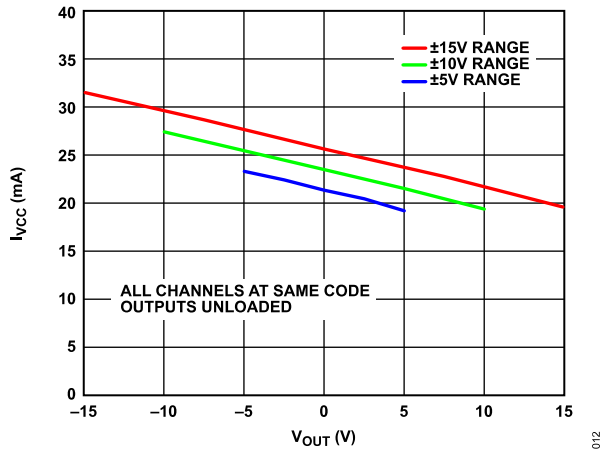


*Figure 13. $I_{VCC}$ vs. $V_{OUT}$*

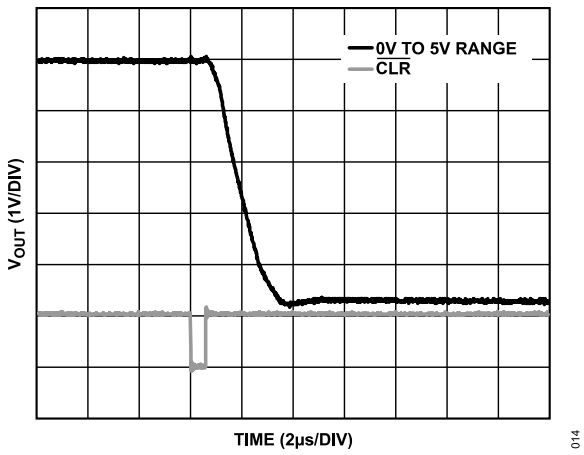


*Figure 14. Hardware $\overline{CLR}$ to Zero Scale*

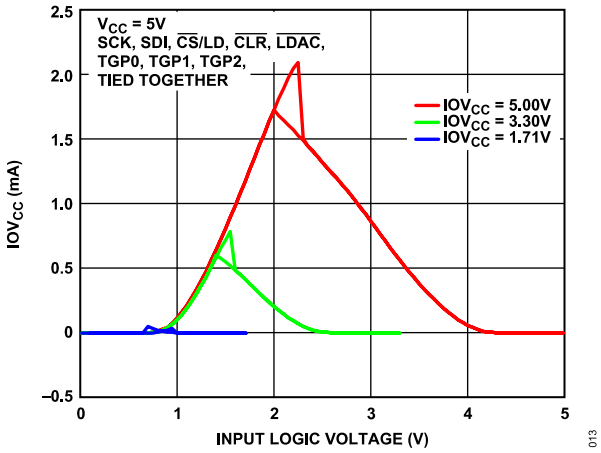


*Figure 15. $IOV_{CC}$ vs. Input Logic Voltage*

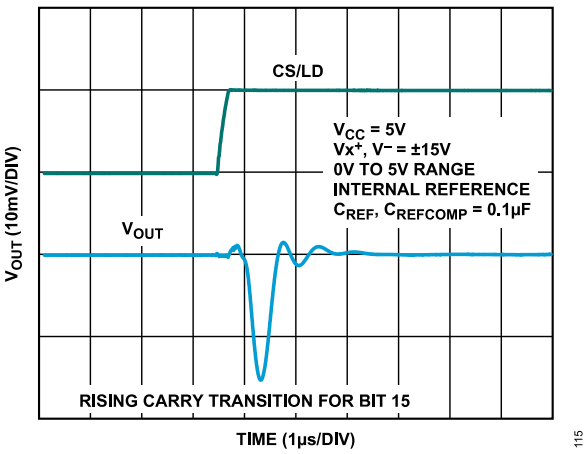


*Figure 16. Glitch Impulse*

## TYPICAL PERFORMANCE CHARACTERISTICS

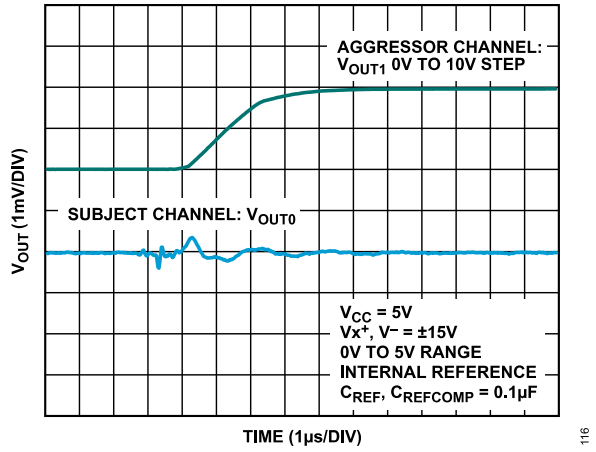


*Figure 17. DAC to DAC Crosstalk*

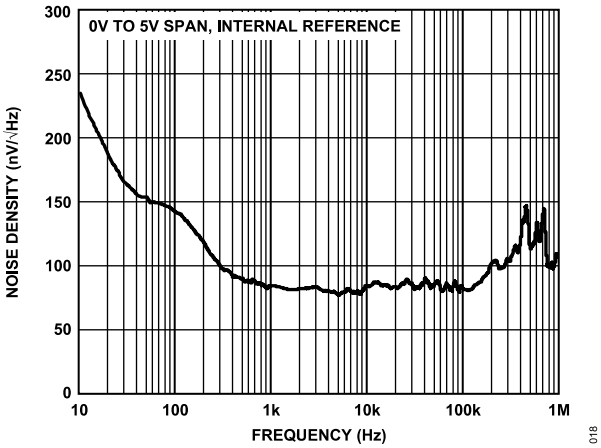


*Figure 18. Noise Density vs. Frequency*

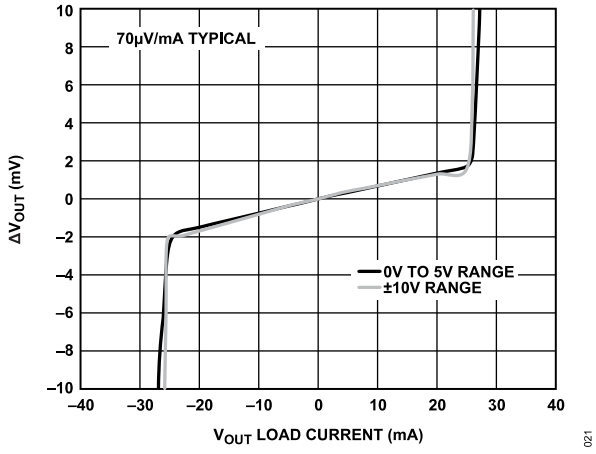


*Figure 19. $\Delta V_{OUT}$ vs. $V_{OUT}$ Load Current*

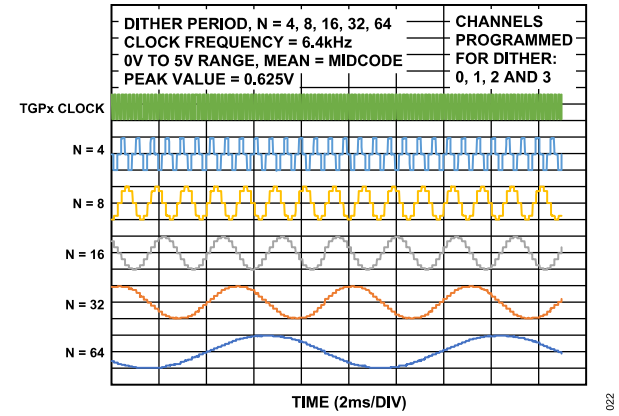


*Figure 20. Sinusoidal Dither Waveform*

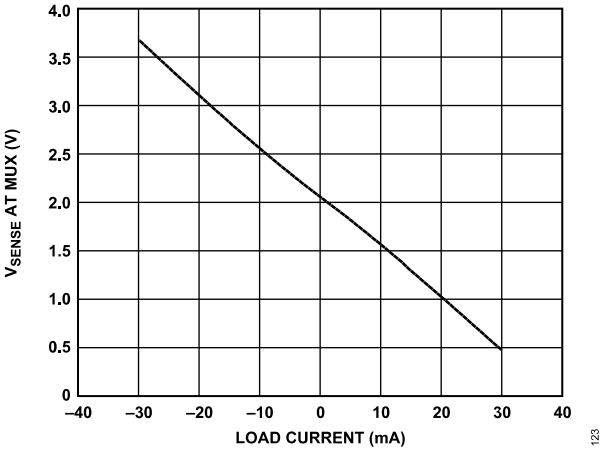


*Figure 21. $V_{SENSE}$ at MUX vs. Load Current*

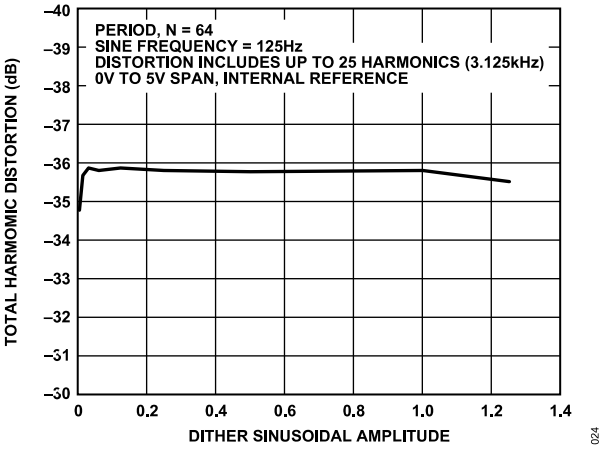


*Figure 22. Total Harmonic Distortion (THD) vs. Dither Sinusoidal Amplitude*

## TYPICAL PERFORMANCE CHARACTERISTICS

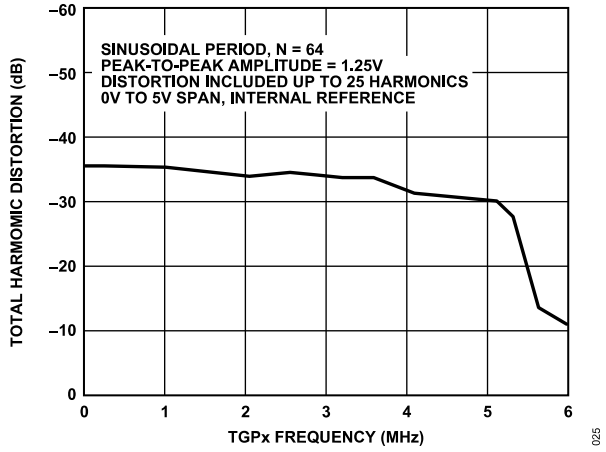


*Figure 23. Total Harmonic Distortion vs. TGPx Frequency*

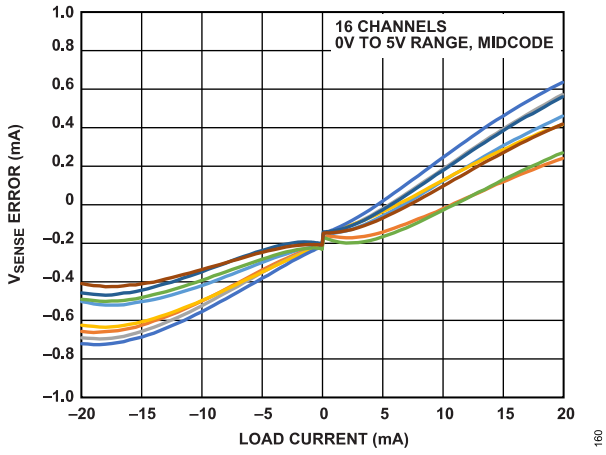


*Figure 24. $V_{SENSE}$ Error vs. Load Current from Equation 2 and Equation 3*

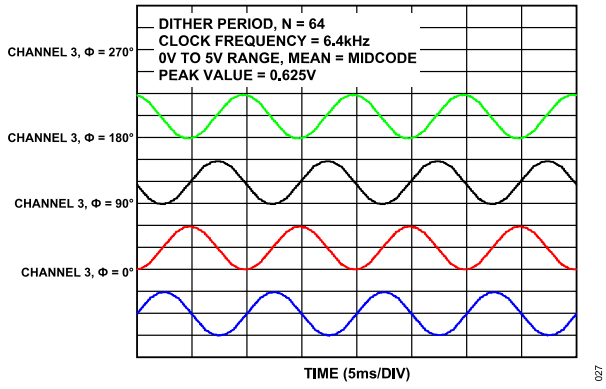


*Figure 25. Sinusoidal Dither for Various Phase Settings*

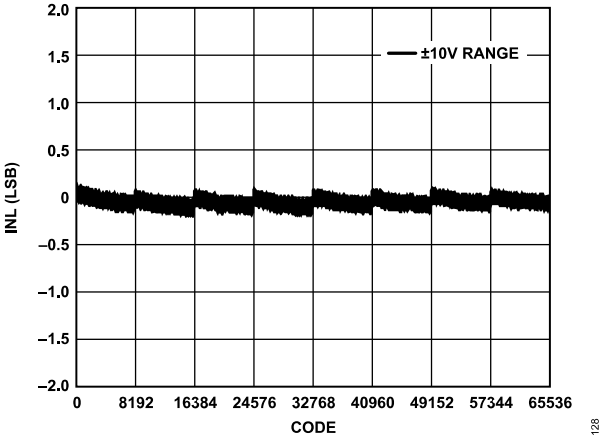


*Figure 26. INL vs. Code*

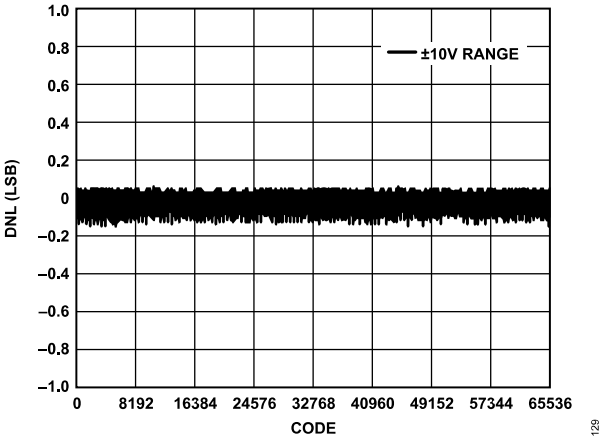


*Figure 27. DNL vs. Code*

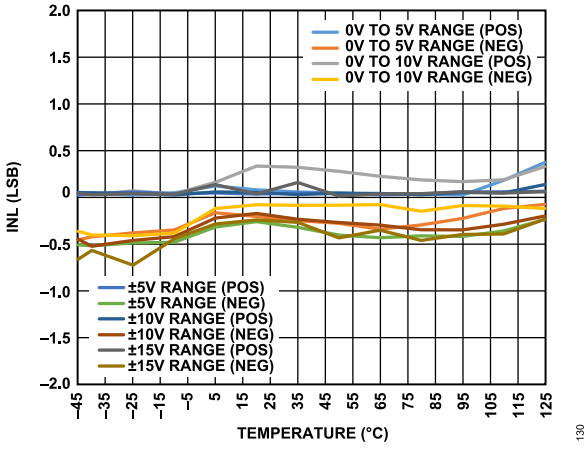


*Figure 28. INL vs. Temperature*

## TYPICAL PERFORMANCE CHARACTERISTICS

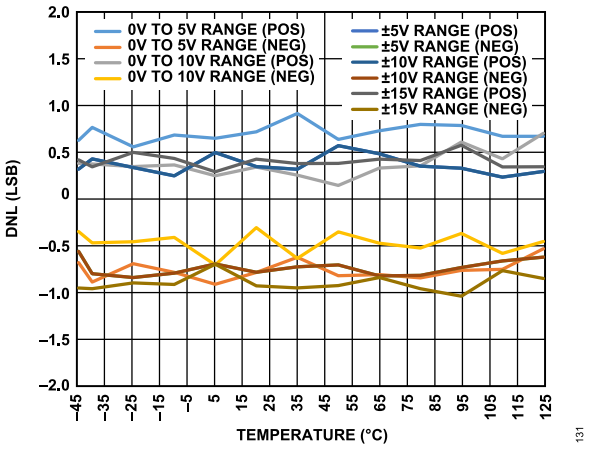


*Figure 29. DNL vs. Temperature*

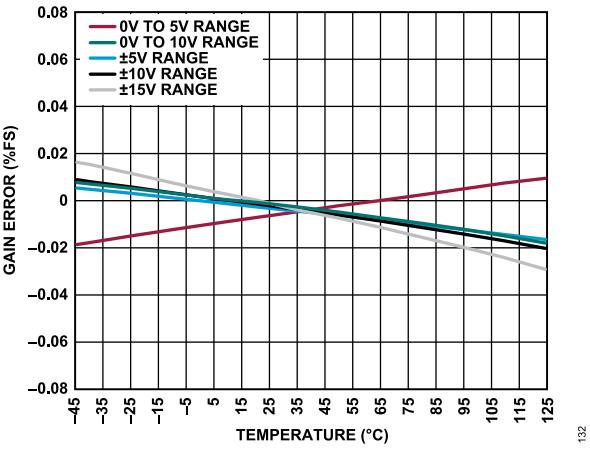


*Figure 30. Gain Error vs. Temperature*

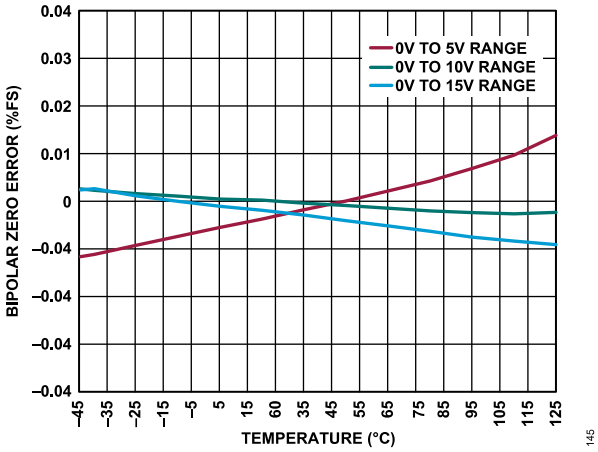


*Figure 31. Bipolar Zero Error vs. Temperature*

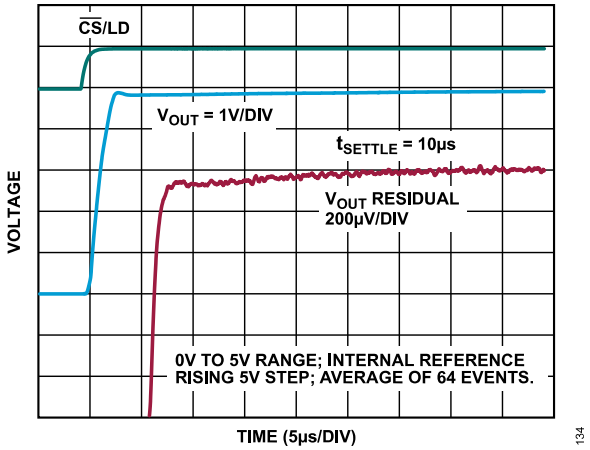


*Figure 32. Settling Time, 5 V*

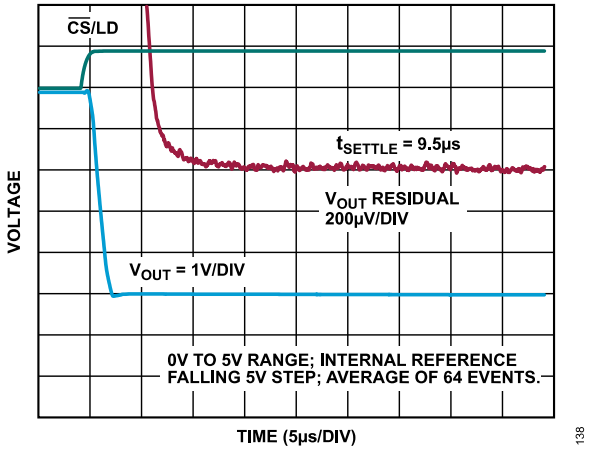


*Figure 33. Settling Time, 5 V (Falling)*

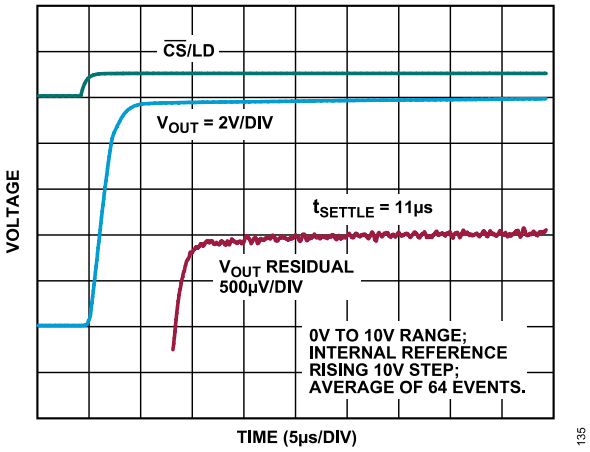


*Figure 34. Settling Time, 10 V*

## TYPICAL PERFORMANCE CHARACTERISTICS

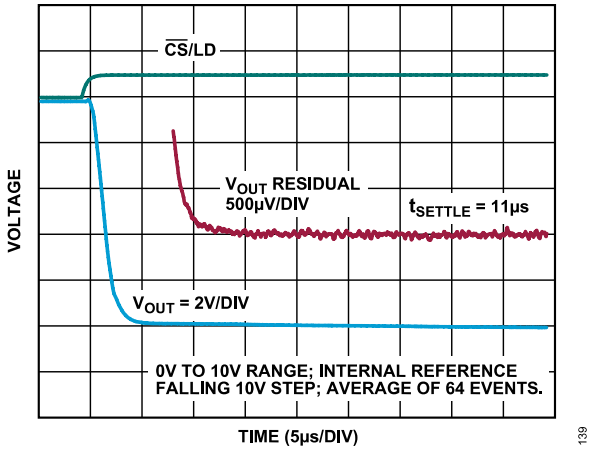


Figure 35. Settling Time, 10 V (Falling)

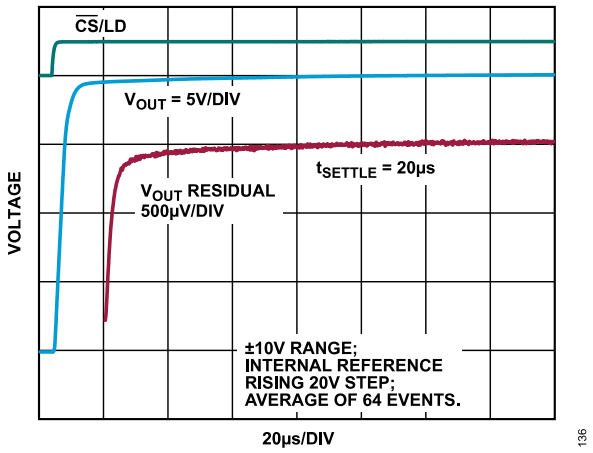


Figure 36. Settling Time, 20 V

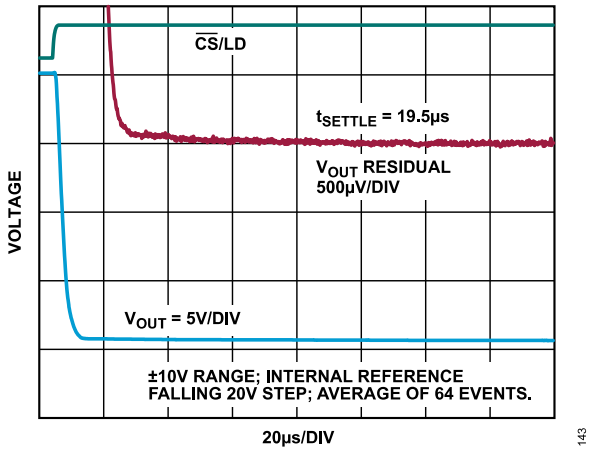


Figure 37. Settling Time, 20 V (Falling)

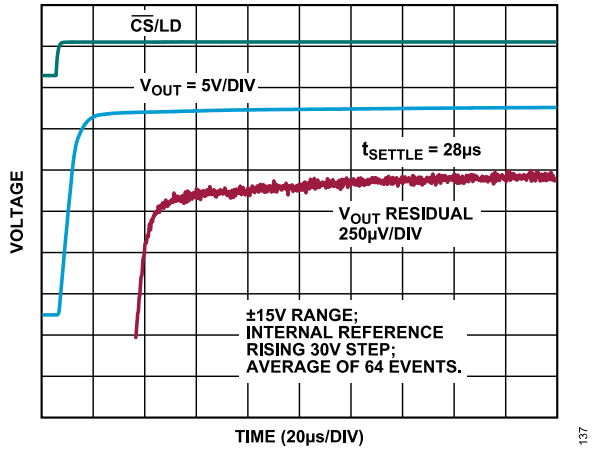


Figure 38. Settling Time, 30 V

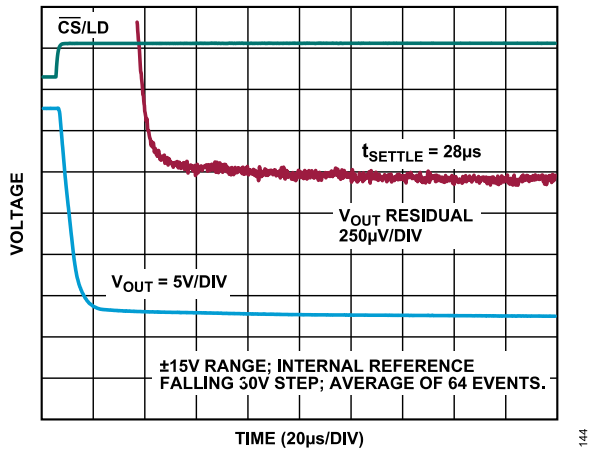


Figure 39. Settling Time, 30 V (Falling)

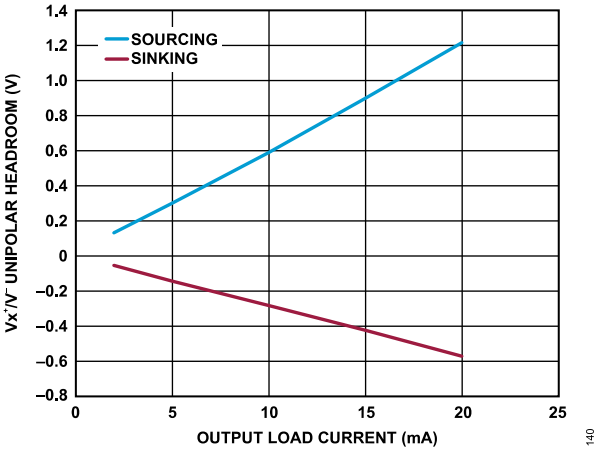


Figure 40. $Vx^+/V^-$ Unipolar Headroom vs. Output Load Current

## TYPICAL PERFORMANCE CHARACTERISTICS

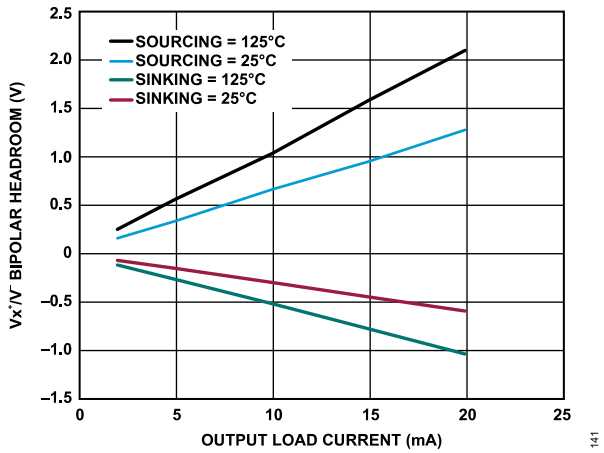


*Figure 41. $Vx^+/V^-$ Bipolar Headroom vs. Output Load Current*

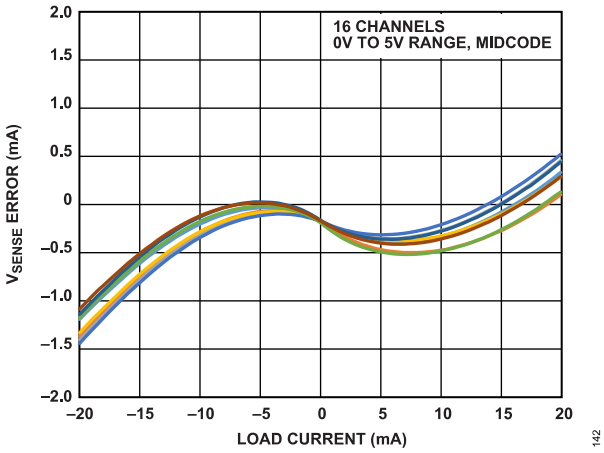


*Figure 42. $V_{SENSE}$ Error vs. Load Current from Equation 5*

## TERMINOLOGY

### Integral Nonlinearity (INL)

Integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL error vs. DAC code plot is shown in Figure 26.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL error vs. DAC code plot is shown in Figure 27.

### Unipolar Offset Error ($V_{OS}$)

Unipolar offset error is the voltage that is measured when zero code is loaded to the DAC register, for unipolar output voltage ranges. Unipolar offset error is expressed in mV.

### $V_{OS}$ Temperature Coefficient

$V_{OS}$ temperature coefficient is a measure of the change in $V_{OS}$ with a change in temperature. It is expressed in ppm/°C.

### Single-Supply Zero-Scale Error

Single-supply zero-scale error is a measurement of the output error when zero code is loaded to the DAC register, and the device is operated with a single supply and $V^-$ is grounded.

### Bipolar Zero Error (BZE)

Bipolar zero error is the deviation of the analog output from the ideal midscale output of 0 V when the DAC register is loaded with midscale code.

### Bipolar Zero Error Temperature Coefficient

Bipolar zero error temperature coefficient is a measure of the change in BZE with a change in temperature. It is expressed in ppm/°C.

### Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as %FSR.

### Gain Error Temperature Coefficient

Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of ppm/°C.

### Power Supply Rejection (PSR)

PSR indicates how the output of the DAC is affected by changes in the supply voltage. PSR is the ratio of the change in $V_{OUTx}$ to a change in $V_{CC}$ for a full-scale output of the DAC. It is measured in dB.

### Settling Time

Settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of $\overline{CS}$/LD.

### Glitch Impulse

Glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the midscale transition.

### DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output or power status of another DAC. It is measured with a full-scale output change on one DAC (or power-down and power-up) while monitoring another DAC output maintained at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

### DAC to DAC Crosstalk

DAC to DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. DAC to DAC crosstalk is measured with a full-scale code change (all 0s to all 1s and vice versa) on one DAC output, using the write and update commands, while monitoring the other DAC output kept at midscale. The energy of the glitch is expressed in nV-sec.

### Output Noise Spectral Density

Output noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

## THEORY OF OPERATION

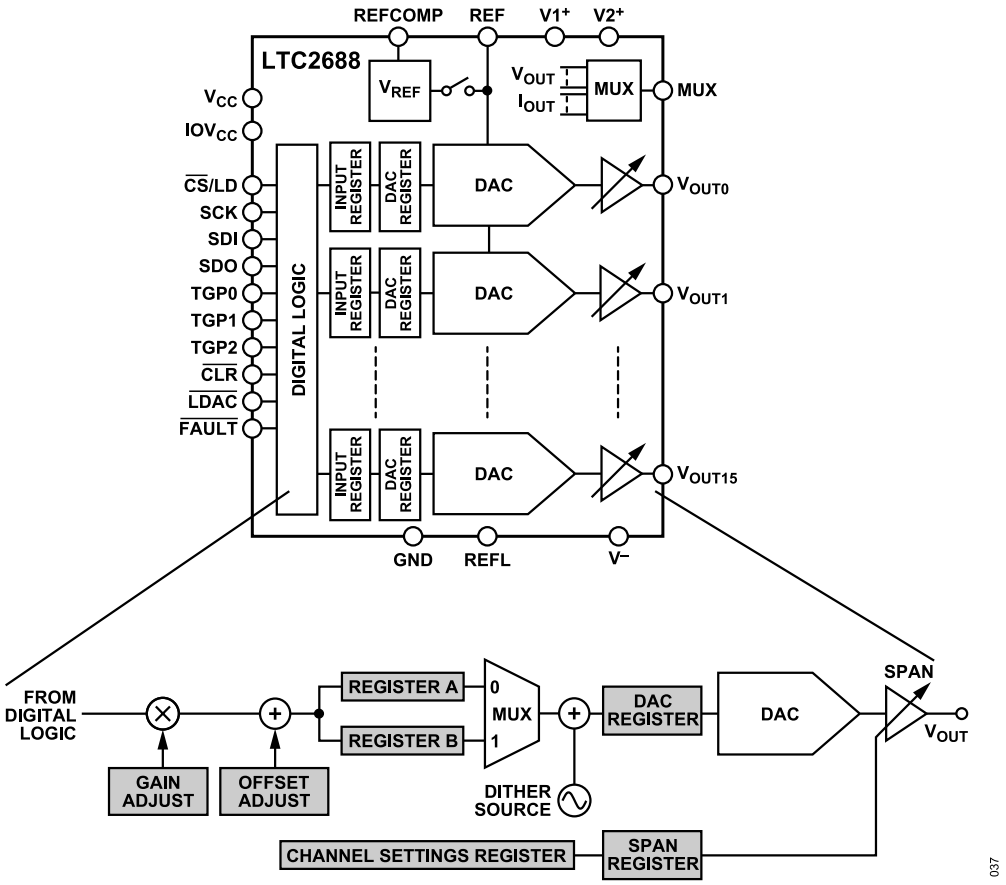


*Figure 43. Block Diagram*

The LTC2688 is a 16-channel, ±15 V DAC with selectable output ranges and an integrated precision reference. The DAC operates on a positive 5 V $V_{CC}$ supply, and the outputs are driven by bipolar supply rails ($V1^+$, $V2^+$, and $V^-$). $V1^+$ and $V2^+$ can operate as low as $V_{CC}$, and the negative $V^-$ supply can operate at ground, making the devices compatible with single-supply systems. $V1^+$ and $V2^+$ can operate as high as +21 V (V1+ must be greater than or equal to $V2^+$). $V^-$ can operate as low as −21 V, making the LTC2688 robust in industrial environments where high voltage fault protection is critical.

The output amplifiers offer true rail-to-rail operation and can source or sink up to 20 mA per DAC channel. The $V1^+$ and $V2^+$ pins can operate at independent voltages to optimize power efficiency. When drawing a load current from the $V1^+$, $V2^+$, or $V^-$ rails, the output voltage headroom with respect to that rail is limited by the typical channel resistance of the output devices.

### POWER-ON RESET

The outputs reset when power is first applied, making system initialization consistent and repeatable. Furthermore, on power-up, the device resets all internal registers to their default values. The default output range for all DAC channel outputs is 0 V to 5 V, and the default DAC code is zero scale.

### POWER SUPPLY SEQUENCING

To minimize channel output overshoot and any excess current during power-up, power up the supplies as follows. If $V_{CC}$ and $Vx^+$ have the same values, tie $Vx^+$ to $V_{CC}$ and power them up first, and then power up $V^-$. If $V_{CC}$ and $Vx^+$ have different values, power up $Vx^+$, then $V_{CC}$, and finally $V^-$. $IOV_{CC}$ does not have a supply sequence requirement. For both scenarios, it is recommended to keep the supply ramp times for all supplies to 100 µs or slower. If an external reference is used, maintain the voltage at REF within the range of $-0.3\ V \le V_{REF} \le V_{CC} + 0.3\ V$ during power-up (see the Absolute Maximum Ratings section) and tie the REFCOMP pin to ground (see the Reference Modes section). Take particular care to observe these limits during power supply turn on and turn off sequences when the voltage at $V_{CC}$ is in transition. On power-up, immediately perform a software reset.

Supply bypassing is critical to achieving optimal performance. For optimal performance, establish at least 1 µF to ground on the $V_{CC}$, $V^+$, and $V^-$ supplies, and establish at least 0.1 µF of low, 100 mΩ, effective series resistance (ESR) capacitance for each supply, as close to the device as possible. The larger capacitor can be omitted for $IOV_{CC}$.

## THEORY OF OPERATION

### SERIAL INTERFACE

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edges of the clock (SCK). Data can only be transferred to the LTC2688 when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified. For the LTC2688, the total word length can be 24 bits (3 bytes) or 32 bits (4 bytes). The leading command/address byte is followed by two data bytes and an optional third that contains an optional 6-bit cyclic redundancy check (CRC) code. See the SPI Cyclic Redundant Check Enable/Disable section for details.

CRC checking is only supported for a word length of 32 bits (4 bytes). In daisy-chain mode, internal register length requires the clock count to be multiples of 32. See the Daisy-Chain Mode section for details.

To ensure data integrity, the device also monitors the number of bits clocked into the chip and issues a fault condition for an invalid number of clock cycles. See the Fault Detection section for details.

Figure 44 and Figure 45 show timing waveforms of a typical 32-bit SPI transaction. The $\overline{CS}$/LD pin must be low while bits are clocked in. The following rising edge of $\overline{CS}$/LD completes the SPI transaction and executes the command. Figure 44 shows a typical 32-bit write command sequence with echo readback. For all write commands, the command word reappears on the SDO pin with a latency of one command cycle (echo readback). This latency allows the user to read back the command from the device and verify the integrity of the data transfer. Figure 45 shows a typical 32-bit read command sequence. In this example, the user reads the fault register. Both the read command and the requested data appear with a latency of one command cycle during the transmission of the next command word.

Figure 46 shows a typical 24-bit read command sequence. A 24-bit read command differs from a 32-bit read command in that only the requested data appears with a latency of one command cycle during the transmission of the next command word. The first eight bits do not show the read command that was executed. Instead, ignore those bits. Note that echo readback is not available when 24-bit command words are used.

For the detailed structure of command words, refer to the Writing Codes to DACs section and the Read Commands section.

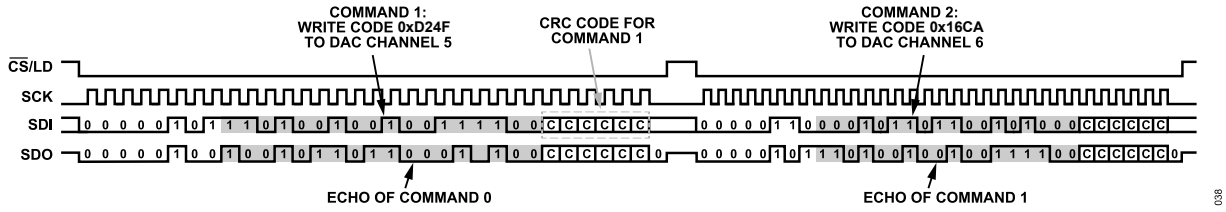


*Figure 44. Typical Write Command Sequence for 32-Bit Words, with Echo Readback*

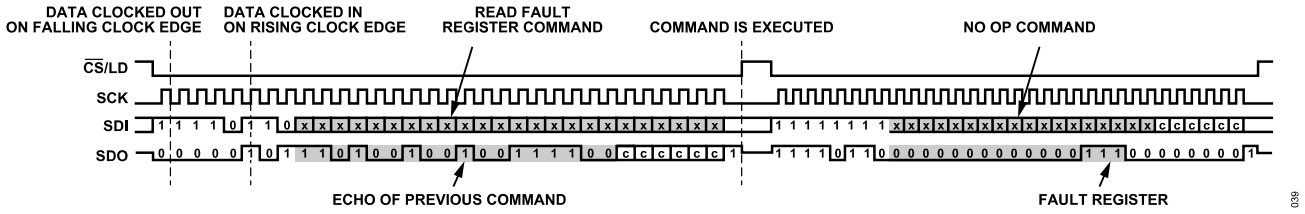


*Figure 45. Typical Read Command Sequence for 32-Bit Words, X = Don't Care*

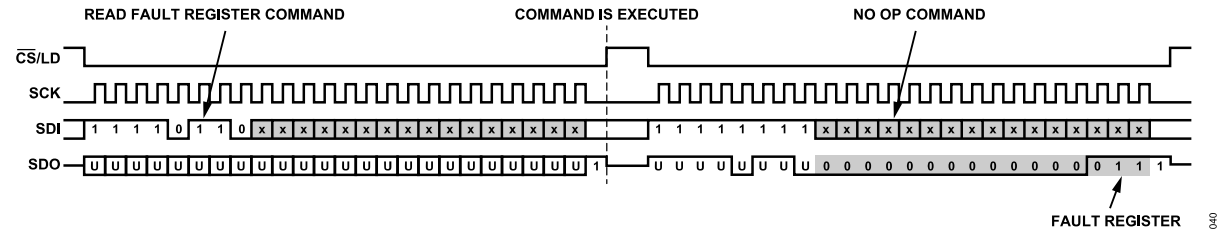


*Figure 46. Typical Read Command Sequence for 24-Bit Words*

## THEORY OF OPERATION

### SPI Command Table

The LTC2688 supports the write and read commands summarized in Table 8 and Table 9. Commands are encoded with the first byte containing the command code. For commands that refer to a specific DAC channel, the chip interprets the last four bits of the command byte as the binary encoded DAC Channel Address A[3:0], see Table 10. The optional CRC error checking is available for all commands, except for the write/read configuration register (Command 7 and Command 24), and the write/read fault register (Command 13 and Command 30). For these commands, CRC error checking is skipped even if the CRC error checking feature is enabled.

*Table 8. Write Operation SPI Commands*

| Command No. | Write Operations | Command Code | Data | CRC (Optional) |
|---|---|---|---|---|
| 0 | Write code to DAC Channel x | 0000 A[3:0] | Data | CRC |
| 1 | Write channel settings to DAC Channel x | 0001 A[3:0] | Data | CRC |
| 2 | Write offset adjust to DAC Channel x | 0010 A[3:0] | Data | CRC |
| 3 | Write gain adjust to DAC Channel x | 0011 A[3:0] | Data | CRC |
| 4 | Write code to and update DAC Channel x | 0100 A[3:0] | Data | CRC |
| 5 | Write code to DAC Channel x, update all DAC channels | 0101 A[3:0] | Data | CRC |
| 6 | Update DAC Channel x | 0110 A[3:0] | Don't care | CRC |
| 7 | Write configuration register | 0111 0000 | Data | Don't care |
| 8 | Write power-down register | 0111 0001 | Data | CRC |
| 9 | Write A/B select register | 0111 0010 | Data | CRC |
| 10 | Write software toggle bit register | 0111 0011 | Data | CRC |
| 11 | Write toggle/dither enable register | 0111 0100 | Data | CRC |
| 12 | Write mux control register | 0111 0101 | Data | CRC |
| 13 | Write fault register | 0111 0110 | Data | Don't care |
| 14 | Write code to all DAC channels | 0111 1000 | Data | CRC |
| 15 | Write code and update all DAC channels | 0111 1001 | Data | CRC |
| 16 | Write channel settings to all DAC channels | 0111 1010 | Data | CRC |
| 17 | Write channel settings and update all DAC channels | 0111 1011 | Data | CRC |
| 18 | Update all DAC channels | 0111 1100 | Don't care | CRC |

*Table 9. Read Operation SPI Commands*

| Command No. | Read Operations | Command Code | Data | CRC (Optional) |
|---|---|---|---|---|
| 20 | Read offset and gain adjusted code of DAC Channel x | 1000 A[3:0] | Don't care | CRC |
| 21 | Read channel settings of DAC Channel x | 1001 A[3:0] | Don't care | CRC |
| 22 | Read offset adjust of DAC Channel x | 1010 A[3:0] | Don't care | CRC |
| 23 | Read gain adjust of DAC Channel x | 1011 A[3:0] | Don't care | CRC |
| 24 | Read configuration register | 1111 0000 | Don't care | Don't care |
| 25 | Read power-down status | 1111 0001 | Don't care | CRC |
| 26 | Read A/B select register | 1111 0010 | Don't care | CRC |
| 27 | Read software toggle bit register | 1111 0011 | Don't care | CRC |
| 28 | Read toggle/dither enable register | 1111 0100 | Don't care | CRC |
| 29 | Read mux control register | 1111 0101 | Don't care | CRC |
| 30 | Read fault register | 1111 0110 | Don't care | Don't care |
| 31 | Read thermal shutdown status register | 1111 0111 | Don't care | CRC |
| 32 | No operation | 1111 1111 | Don't care | CRC |

## THEORY OF OPERATION

### WRITING CODES TO DACS

The LTC2688 has several internal registers for each DAC. A DAC channel has two sets of double buffered registers: one set for the code data, and one set for the span (output range) of the DAC. Double buffering provides the capability to simultaneously update the span and code, which allows smooth voltage transitions when changing output ranges. Double buffering also enables the simultaneous updating of multiple DACs. Each set of double buffered registers comprises an input register and a DAC register, as follows:

- Input register: the write operation shifts data from the SDI pin into a chosen input register. The input registers are holding buffers. Write operations do not affect the DAC outputs directly. In the code datapath, there are two input registers, A and B, for each DAC register. Input Register B is an alternate input register used only in toggle and dither operation, whereas Input Register A is the default input register (see Figure 43).
- DAC register: the update operation copies the contents of an input register to its associated DAC register. The content of a DAC register directly controls the DAC output voltage or range. The update operation also powers up the selected DAC if it was in power-down mode. The datapath and registers are shown in Figure 43. Updates always refresh both code and span data, but the values held in the DAC registers remain unchanged unless the associated input register values have been changed via a write operation. For example, writing a new code and updating the channel updates the code, but the span is unchanged. A channel update can come from a serial update command, an $\overline{\text{LDAC}}$ negative pulse, or a toggle operation.

Table 11 shows the command word structure for Command 0, write code to DAC Channel x. Individual DAC channels are addressed by Bits A[3:0] as shown in Table 10. The MSB bit of the data, D[15:0] is always aligned with the first bit of Byte 1.

*Table 10. DAC Address Mapping*

| | Address | | | |
|---|---|---|---|---|
| DAC No. | A3 | A2 | A1 | A0 |
| DAC0 | 0 | 0 | 0 | 0 |
| DAC1 | 0 | 0 | 0 | 1 |
| DAC2 | 0 | 0 | 1 | 0 |
| DAC3 | 0 | 0 | 1 | 1 |
| DAC4 | 0 | 1 | 0 | 0 |
| DAC5 | 0 | 1 | 0 | 1 |
| DAC6 | 0 | 1 | 1 | 0 |
| DAC7 | 1 | 1 | 1 | 1 |
| DAC8 | 1 | 0 | 0 | 0 |
| DAC9 | 1 | 0 | 0 | 1 |
| DAC10 | 1 | 0 | 1 | 0 |
| DAC11 | 1 | 0 | 1 | 1 |
| DAC12 | 1 | 1 | 0 | 0 |
| DAC13 | 1 | 1 | 0 | 1 |
| DAC14 | 1 | 1 | 1 | 0 |
| DAC15 | 1 | 1 | 1 | 1 |

Several additional commands are supported to write codes to DAC channels and perform update operations. Command 0, Command 4, and Command 5 write a DAC code to DAC Channel x, with x encoded in A[3:0]. In addition to writing a DAC code to DAC Channel x, Command 4 updates DAC Channel x and Command 5 updates all DAC channels. Command 6 only updates DAC Channel x.

Command 14, Command 15, and Command 18 operate on all DAC channels simultaneously. Command 14 writes the same code to all DAC channels, Command 15 writes to and updates all DAC channels, and Command 18 only updates all DAC channels.

All commands that write or update DAC channels follow the same command word structure as shown in Table 11, except for Command 6 and Command 18, for which the D[15:0] data is replaced with X, where X represents don't care bits. Note that C represents the CRC code bits.

*Table 11. Write Code to DAC Channel X, Command 0*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000, A[3:0] | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

*Table 12. Writing DAC Channel Settings, Command 1*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0001, A[3:0] | X | X | X | X | Mode | DIT_ PH1 | DIT_ PH0 | DIT_ PER2 | DIT_ PER1 | DIT_ PER0 | TD_ SEL1 | TD_ SEL0 | S3 | S2 | S1 | S0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

## THEORY OF OPERATION

### SPAN SELECTION AND CHANNEL SETTINGS

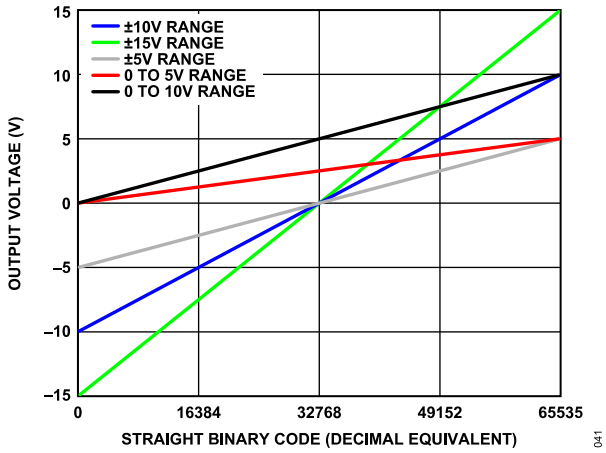


*Figure 47. DAC Transfer Functions for LTC2688, All Voltage Spans and Bit Resolutions, Internal Reference Mode*

The LTC2688 allows individual programming of the voltage span (output voltage range) for each DAC channel (SoftSpan). The device also supports 5% overrange spans. The span selection bits, S[3:0], encode span settings as summarized in Table 13 and Table 14, and the corresponding DAC transfer functions are depicted in Figure 47.

*Table 13. Span Selection Bits S[3:0] Settings*

| | | | | Output Range | |
|---|---|---|---|---|---|
| S3 | S2 | S1 | S0 | Internal Reference | External Reference |
| 0 | 0 | 0 | 0 | 0 V to 5 V | 0 V to 5 × ($V_{REF}$/4.096) |
| 0 | 0 | 0 | 1 | 0 V to 10 V | 0 V to 10 × ($V_{REF}$/4.096) |
| 0 | 0 | 1 | 0 | ±5 V | ±5 × ($V_{REF}$/4.096) |
| 0 | 0 | 1 | 1 | ±10 V | ±10 × ($V_{REF}$/4.096) |
| 0 | 1 | 0 | 0 | ±15 V | ±15 × ($V_{REF}$/4.096) |

*Table 14. Span Selection Bits S[3:0] Settings, 5% Overrange*

| | | | | Output Range | |
|---|---|---|---|---|---|
| S3 | S2 | S1 | S0 | Internal Reference | External Reference |
| 1 | 0 | 0 | 0 | 0 V to 5.25 V | 0 V to 5 × ($V_{REF}$/4.096) |
| 1 | 0 | 0 | 1 | 0 V to 10.5 V | 0 V to 10 × ($V_{REF}$/4.096) |
| 1 | 0 | 1 | 0 | ±5.25 V | ±5 × ($V_{REF}$/4.096) |
| 1 | 0 | 1 | 1 | ±10.5 V | ±10 × ($V_{REF}$/4.096) |
| 1 | 1 | 0 | 0 | ±15.75 V | ±15 × ($V_{REF}$/4.096) |

Use Command 1, detailed in Table 12, to program DAC channel settings and span ranges. Span settings are contained in Bits S[3:0] and the default value is 0x0. Note that X represents the don't care bits and C represents the CRC code bits. If CRC error checking is not used, the third data byte can be omitted (24-bit word length). See the Toggle and Dither Operation section for a detailed description of related registers and functions.

Command 1 writes the settings of DAC Channel x, with DAC Channel Address x encoded in A[3:0]. Command 16 writes settings to all DAC channels, whereas Command 17 also updates all DAC channels.

### READ COMMANDS

Read operations are initiated with read commands as shown in Table 15. The command byte is followed by X (don't care bits), and an optional CRC code. For example, when reading the configuration register, the user must send Command 24 (see Table 15) to the device. The requested data appears at the SDO pin in the next command cycle (see Table 16) and mirrors the syntax of the corresponding write command. Note that the device outputs trailing zeros for the third byte. For a list of supported read commands, refer to Table 9.

*Table 15. Command Word for Reading Configuration Register, Command 24*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 0000 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

*Table 16. SDO Pin Data-Words After the Read Configuration Register Command*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 0000 | RST | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TSD_ DIS | EXT_ REF | SPI_ CRC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## THEORY OF OPERATION

### OFFSET AND GAIN ADJUSTMENT

The LTC2688 supports offset and gain adjustment for each individual DAC channel. Note that the gain operation is performed before the offset correction (see Figure 43). The adjusted DAC code is calculated by multiplying the code data, D[15:0], by the gain adjust code, G[15:0], and then adding the offset adjust code, O[13:0].

### Offset Adjustment

The device supports an offset adjustment range of ±12.5% full scale with a resolution of 1 LSB. Table 17 shows offset adjustment ranges and corresponding codes. Note that negative offsets are encoded in twos complement binary data format.

Use Command 2 (see Table 18) to program offset adjustments. Note that after writing to the offset adjustment registers of a DAC channel, offset adjustment does not take effect until a code is written to the DAC. Use Command 20 to read back the offset adjusted DAC code. Table 19 shows the adjusted data-word that appears at the SDO pin after Command 20 is written.

*Table 17. Offset Correction Range and Codes*

| Offset Adjust Value[1] | O[13:0][1] |
|---|---|
| +12.498 % FS | 0111...111 |
| ... | ... |
| +30.5 ppm FS | 0000...010 |
| +15.3 ppm FS | 0000...001 |
| 0 ppm FS | 0000...000 |
| −15.3 ppm FS | 1111...111 |
| −30.5 ppm FS | 1111...110 |
| ... | ... |
| −12.5 % FS | 1000...000 |

[1] Ellipses (...) indicate a sequential continuation of the numbering scheme.

*Table 18. Writing Offset Adjustment to a DAC Channel, Command 2*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0010 A[3:0] | O13 | O12 | O11 | O10 | O9 | O8 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | X | X | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

*Table 19. SDO Pin Data-Word Readback of Offset and Gain Adjusted DAC Code, Command 20*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1000 A[3:0] | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## THEORY OF OPERATION

### Gain Adjustment

The device supports a gain adjustment range from 1.5× to 0.5×, or ±50%. Table 20 shows gain adjustment ranges and corresponding codes.

Negative gain adjustments are encoded in twos complement binary data format. The following formula shows the calculation of the gain adjustment code, $G^{CODE}$:

$$G^{CODE} = \text{round}\left(2^M \times \frac{G^{\%}}{100}\right) \quad (1)$$

where:
$G^{CODE}$ is the gain adjustment code, G[15:0].
$G^{\%}$ is the desired gain adjustment.
$M$ is the resolution parameter listed in Table 20.

Use Command 3 (see Table 21) to program the gain adjustments.

Note that after writing to the gain registers of a DAC channel, the gain adjustment does not take effect until a code is written to the DAC. Use Command 20 to read back the offset and gain adjusted DAC code.

Table 19 shows the adjusted data-word that appears at the SDO pin after Command 20 is written.

***Table 20. Gain Adjust Range and Codes, M = 16***

| Gain Adjust, $G^{\%}$[1] | Unit | $G^{CODE}$, G[15:0][1] |
|---|---|---|
| +50 | %FS | 0111...111 |
| … | | … |
| +30.5 | ppm FS | 0000…010 |
| +15.3 | ppm FS | 0000…001 |
| 0 | ppm FS | 0000…000 |
| −15.3 | ppm FS | 1111...111 |
| −30.5 | ppm FS | 1111...110 |
| … | | … |
| −50 | %FS | 1000…000 |

[1] The ellipses (…) indicate a sequential continuation of the numbering scheme.

***Table 21. Writing Gain Adjustment to a DAC Channel, Command 3***

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0011 A[3:0] | G15 | G14 | G13 | G12 | G11 | G10 | G9 | G8 | G7 | G6 | 65 | G4 | G3 | G2 | G1 | G0 | X | X | X | C/X | C/X | C/X | C/X | C/X |

## THEORY OF OPERATION

### ANALOG MUX

The LTC2688 includes an analog high voltage multiplexer (mux) for monitoring the 16 DAC output voltages and load currents and takes voltage measurements at the MUX pin (Pin 12). The MUX pin is intended for use with high impedance loads only. Continuous dc output current at the MUX pin must be limited to ±200 µA to avoid damaging internal circuits. The output impedance of the multiplexer is 3.5 kΩ. However, when using the multiplexer to measure load current ($V_{SENSE}$), the output impedance is typically 100 kΩ. The output voltage range of the multiplexer is from $V^-$ to ($V1^+$ − 1.4 V). Note that when the mux is disabled (ENMUX = 0), the MUX pin is high impedance, which is the default at power-up. For enabling the mux and selecting a signal with the M[9:0] bits, use Command 12 (shown in Table 23) to set the mux control register.

*Table 22. Analog Mux Control Addresses*

| M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 | MUX Pin State |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DAC0 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DAC1 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | DAC2 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | DAC3 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | DAC4 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | DAC5 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | DAC6 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | DAC7 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | DAC8 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | DAC9 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | DAC10 Voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | DAC11 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | DAC12 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | DAC13 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | DAC14 voltage output |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | DAC15 Voltage output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DAC0 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DAC1 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | DAC2 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | DAC3 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | DAC4 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | DAC5 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | DAC6 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | DAC7 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | DAC8 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | DAC9 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | DAC10 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | DAC11 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | DAC12 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | DAC13 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | DAC14 $V_{SENSE}$ output |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | DAC15 $V_{SENSE}$ output |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | REFL (Pin 14) |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | $V_{CC}$ |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | $V_{REF}$ |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Voltage proportional to absolute temperature (VPTAT), $T_J$ = 25°C + (VPTAT − 2.44)/(7.95 × $10^{-3}$) |

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*Table 23. Mux Control Register, Command 12*

| Command Code | Byte 1 | | | | | | | | | | | Byte 2 | | | | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0111 0101 | X | X | X | X | X | ENMUX | M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

Setting the ENMUX bit (default value is 0) enables the mux. The M[9:0] bits (default value is 0x000) are mux address bits. See Table 23 for signal selection. To read the mux control register, use Command 29. The data-word containing the mux control register appears at the SDO pin in the next command cycle. See the Read Commands section for details.

If the M[9:0] bits are set to monitor the $V_{SENSE}$ voltage of a DAC channel output, a voltage that represents the load current of the corresponding DAC channel appears at the MUX pin (Pin 12). The DAC channel load current can be calculated using the $V_{SENSE}$ voltage and the DAC channel output voltage, $V_{OUT}$. If $V_{SENSE}$ < 2.048 V, use Equation 2 to calculate the load source current.

$$I_{LOAD\ SOURCE} = \frac{1}{6} \times \sqrt{1 - \frac{V_{SENSE}}{5}} - 0.128 - \frac{\beta \times V_{OUT}}{25,000} \quad (2)$$

If $V_{SENSE}$ > 2.048 V, use Equation 3 to calculate the load sink current.

$$I_{LOAD\ SINK} = \frac{\sqrt{2.048} - \sqrt{V_{SENSE}}}{16.2} - \frac{\beta \times V_{OUT}}{25,000} \quad (3)$$

where:
$I_{LOAD\ SOURCE}$ and $I_{LOAD\ SINK}$ are in amperes.
$I_{LOAD\ SOURCE}$ is a positive value, indicating current is flowing out of the DAC output, and $I_{LOAD\ SINK}$ is a negative value, indicating current is flowing into the DAC channel.
$V_{SENSE}$ and $V_{OUT}$ are in volts.
$\beta$ is calculated as follows:

$$\beta = 1 - \frac{4}{Span\ \ Range} \quad (4)$$

where *Span Range* is the voltage range of the DAC channel (5 for 0 V to 5 V range, 10 for 0 V to 10 V range or ±5 V range, 20 for ±10 V range, and 30 for ±15 V range).

Using Equation 2 through Equation 4, the load current monitor has a typical $V_{SENSE}$ error of under 800 µA (see Figure 24).

Alternatively, use the following simpler formula to measure the load current, $I_{LOAD}$:

$$I_{LOAD} = {(2.048 - V_{SENSE})}/{50} \quad (5)$$

where:
$I_{LOAD}$ is in amperes. A negative $I_{LOAD}$ indicates a sinking load current, and a positive $I_{LOAD}$ indicates a sourcing current. $I_{LOAD}$ has an error of less than 5% (see Figure 42).
$V_{SENSE}$ is in volts.

## TOGGLE AND DITHER OPERATION

The LTC2688 supports toggle and dither operations. Toggle operation enables fast switching of a DAC output between two different DAC codes without any SPI transaction, thereby eliminating communication transactions. Examples include injection of a small ac bias, or independently switching between on and off states. Dither operation adds a small sinusoidal wave to the digital DAC signal path. Dithering is a signal processing technique that involves the injection of ac noise to the signal path to reduce system nonlinearities. Each DAC channel can be programmed independently for either toggle or dither operation.

### Toggle Operation

Figure 48 illustrates toggle operation. Two unique DAC codes are stored in Input Register A and Input Register B. During toggle operation, a mux controlled by the toggle clock (TCK) determines which input register, either A or B, is latched into the DAC register. The user has control over TCK by choosing the toggle signal for each individual DAC channel by selecting TGPx (where x = 0, 1, or 2) or the software toggle bit.

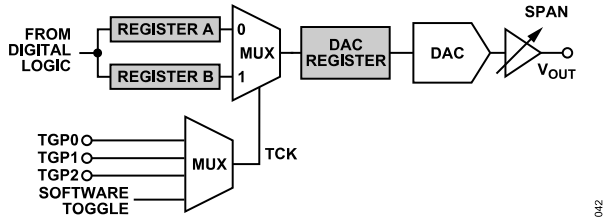


*Figure 48. Toggle Operation*

When the TCK signal is high the DAC outputs a voltage ($V_A$) corresponding to Input Register A, and when TCK is low, the DAC outputs a voltage ($V_B$) corresponding to Input Register B (see Figure 49). The toggle function can be disabled by writing 0x0000 to the toggle/dither enable register (Command 11).

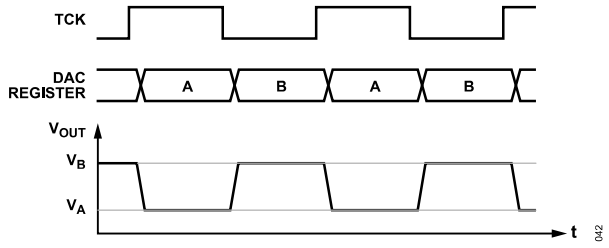


*Figure 49. TCK Timing*

## THEORY OF OPERATION

### Toggle Operation Example

As an example for the LTC2688, to set up Channel 0 for toggling between 32,768 and 32,767, use the TGP2 toggle pin to execute the following command sequence:

1. Write 0x0000 to the A/B select register (Command 9) to select Input Register A.
2. Write Code 0x2000 to Channel 0 (Command 0). Input Register A of Channel 0 is written.
3. Write 0x0001 to the A/B select register (Command 9) to select Input Register B.
4. Write Code 0x1FFF to Channel 0 (Command 0). Input Register B of Channel 0 is written. Input Register A and Input Register B hold the two desired codes. At this stage, Channel 0 is ready for the toggle operation.
5. Write 0x0030 to the channel setting register for Channel 0 (Command 1): mode = 0 and TD_SEL[1:0] = 11. The TGP2 pin is thus selected as the toggle clock input.
6. Write 0x0001 to the toggle/dither enable register (Command 11).
7. Apply the toggle clock signal to the TGP2 pin. The DAC output voltage changes on the rising and falling edges of the toggle clock signal as shown in Figure 49.

### Dither Operation

A dither signal generator injects a digital dither signal into the DAC signal path as shown in Figure 50.

The device generates a sinusoidal dither signal D(n) by accessing a lookup table (see Table 24), and corresponds to

$$D(n) = \sin\left(\frac{2\pi}{N}n + \varphi_0\right)$$

where:
$n$ = 0, 1, 2, ... $N$ − 1.
$N$ is the signal period.
$\varphi_0$ is the phase angle, initial signal phase

Examples of the digital sinusoids are shown in Figure 51 and Figure 52. The user can select the TGPx pins or the software toggle bit as the dither clock (DCK) of the signal generator for each individual DAC channel. Signal parameters, represented by N and $\varphi_0$, can also be selected for each individual channel, which facilitates precise control of signal frequencies and phase relationships between dithered DAC channels. Note that,

$$f_{SIGNAL} = f_{DCK}/N$$

where:
$f_{SIGNAL}$ is the frequency of the dither signal.
$f_{DCK}$ is the dither clock frequency.

Before entering the digital DAC signal path, the sinusoidal dither, D(n), is scaled and offset by values held in Input Register B and Input Register A, respectively, to form the final DAC input as expressed in the following equation.

$$DAC\ Input = A + B \times D(n)$$

The DAC is updated by the rising edge of the designated dither clock signal, DCK, which can be selected as TGPx or the software toggle bit.

*Table 24. Dither Signal Generator Lookup Table Using DIT_PER[2:0] Bits*

| Lookup Table Index | D(n)[1] N = 4, 000 | N = 8, 001 | N = 16, 010 | N = 32, 011 | N = 64, 100 |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0.75 | 0.375 | 0.1875 | 0.09375 |
| 2 | | 1 | 0.75 | 0.375 | 0.1875 |
| 3 | | | 0.9375 | 0.5625 | 0.28125 |
| 4 | | | 1 | 0.75 | 0.375 |
| 5 | | | | 0.84375 | 0.46875 |
| 6 | | | | 0.9375 | 0.5625 |
| 7 | | | | 0.96875 | 0.65625 |
| 8 | | | | 1 | 0.75 |
| 9 | | | | | 0.78125 |
| 10 | | | | | 0.84375 |
| 11 | | | | | 0.875 |
| 12 | | | | | 0.9375 |
| 13 | | | | | 0.96875 |
| 14 | | | | | 0.96875 |
| 15 | | | | | 1 |
| 16 | | | | | 1 |

[1] Blank cells indicate no additional values required for N.

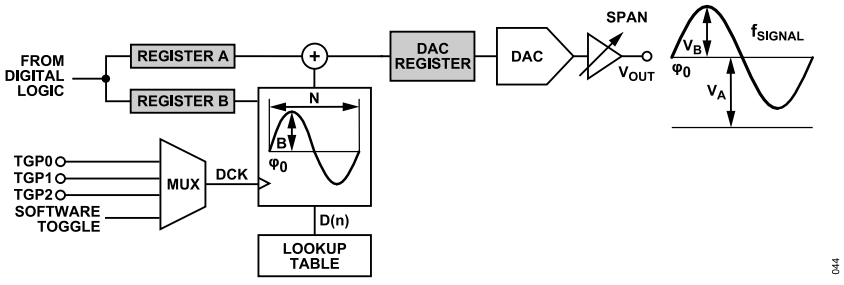


*Figure 50. Dither Signal Operation*

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### Example of Dither Operation

As an example, set up Channel 0 and Channel 1 in dither mode with the following specifications: dc value of 2 V in a ±5 V output range, a sinusoidal amplitude of 10 mV, sinusoidal frequency of 10 kHz, a signal period of N = 64 samples, and use the TGP1 pin as the dither clock input. The dither signals must be out of phase.

For the LTC2688, the dc value to be written to Input Register A is 45,875 = 0xB333.

The range for dither amplitude is 1/4th the span range. Table 25 shows Command 0 for programming the dither signal amplitude for the LTC2688. Note that the user must set two LSBs to 0.

For the LTC2688, Input Register B must be loaded with

$$Code(B) = \frac{10\ \text{mV}}{10\ \text{V}} \times 2^{16} = 66 = 0\text{x}0042 \quad (6)$$

For N = 64, set the toggle frequency to 64 × 10 kHz = 640 kHz. Set the initial phase value to 0 for Channel 0, and to 180 for Channel 1 (see Command 1 in Table 12, Table 30, and Table 31). If no phase relationship is required between different channels, the phase value is set to 0.

Execute the following series of steps to program all necessary registers:

1. Write 0x0000 to the A/B select register (Command 9) to select Input Register A for Channel 0 and Channel 1.
2. Write Code 0xB333 to Channel 0 (Command 0). Input Register A of Channel 0 is written.
3. Write Code 0xB333 to Channel 1 (command 0). Input Register A of Channel 1 is written.
4. Write 0x0003 to the A/B select register (Command 9) to select Register B for Channel 0 and Channel 1.
5. Write Code 0x0042 to Channel 0 (Command 0). Input Register B of Channel 0 is written.
6. Write Code 0x0042 to Channel 1 (Command 0). Input Register B of Channel 1 is written.
7. Write the channel setting register (Command 1) for Channel 0 to set mode = 1, TD_SEL[1:0] = 10, DIT_PER[2:0] = 100, and DT_PH[1:0] = 00. The TGP1 pin is selected as the dither clock input.
8. Write the channel setting register (Command 1) for Channel 1 to set mode = 1, TD_SEL[1:0] = 10, DIT_PER[2:0] = 100, and DT_PH[1:0] = 00. The TGP1 pin is selected as the dither clock input.
9. Write 0x0003 to the toggle/dither enable register (Command 11) to enable dither in Channel 0 and Channel 1.
10. Apply a dither clock of 640 kHz to the TGP1 pin. The DAC outputs are updated with sinusoidal samples at the rising edge of TGP1. Before the toggle enable register is written, the DAC outputs Code A by default. After the toggle enable register is written, the channel is ready for dither.

***Table 25. Bit Alignment for Dither Operation, Command 0***

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000 A[3:0] | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

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### Disabling Dither Operation

Dither operation can be disabled by resetting the toggle/dither enable register (Command 11). After this register is reset, the user must apply at least N clock cycles to ensure completion of the sinusoidal dither signal cycle. Upon finishing the cycle, the dither operation is effectively disabled and regular DAC codes can then be written to the DAC channel. Figure 53 illustrates this mechanism.

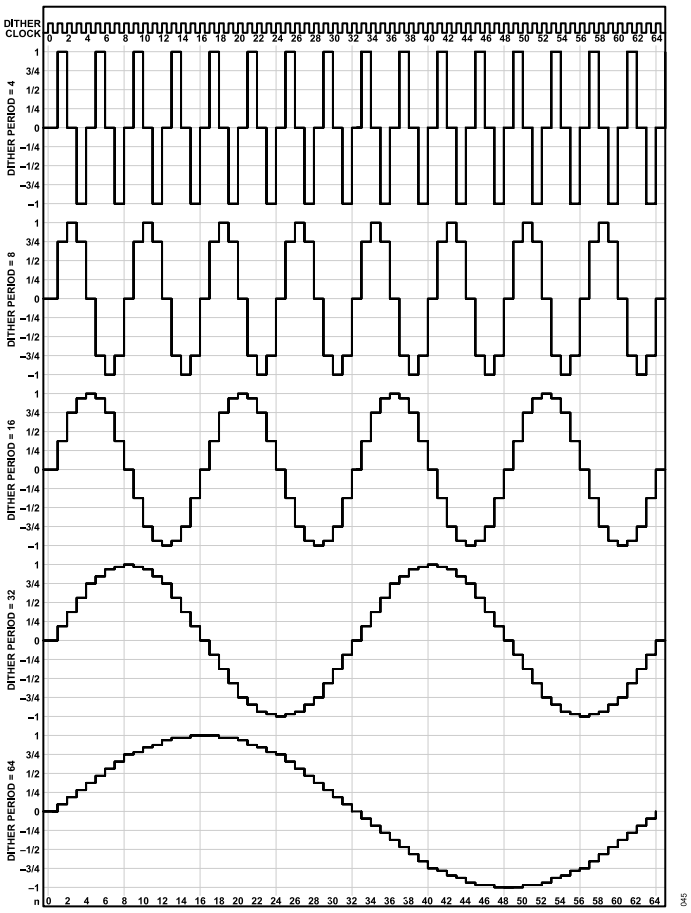


*Figure 51. Sinusoidal Waveforms for Various Values of Dither Period N*

## THEORY OF OPERATION

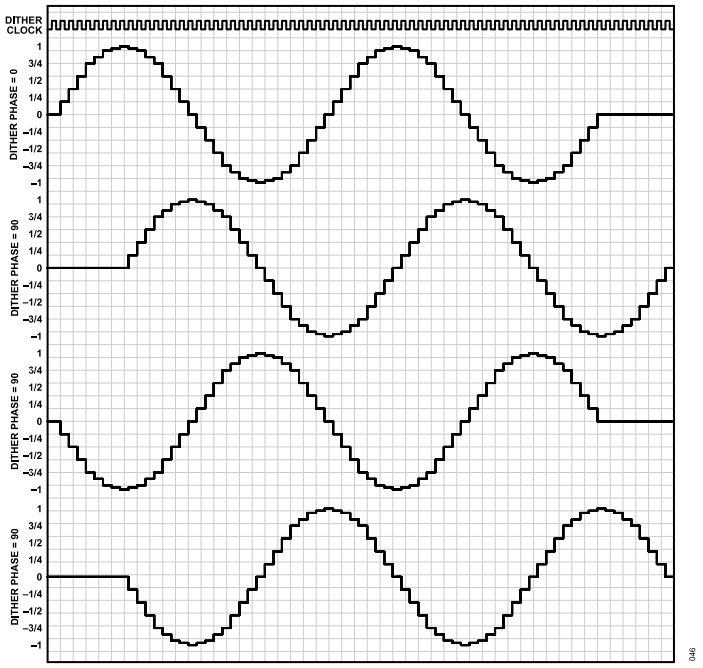


*Figure 52. Sinusoidal Waveforms for Various Values of $\Phi_0$*

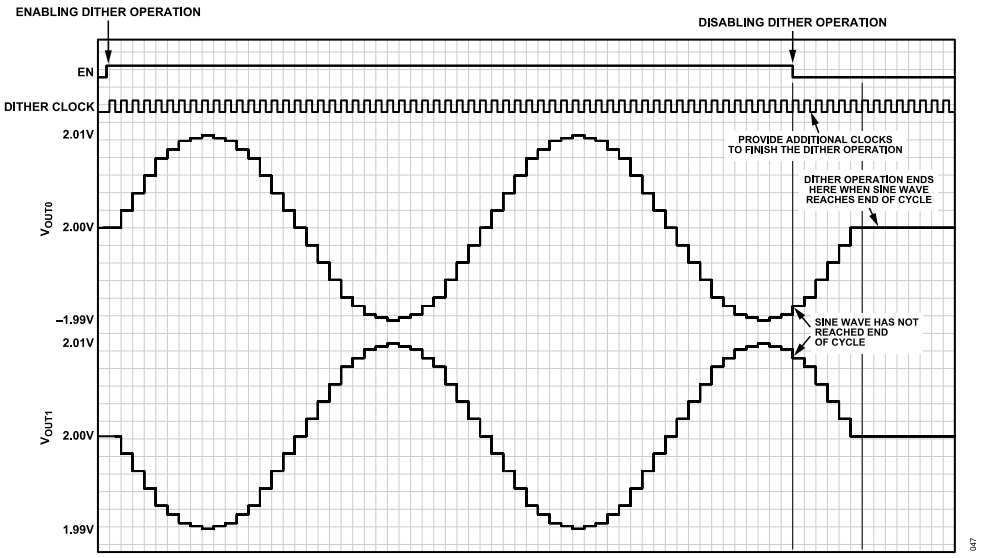


*Figure 53. Termination of Sinusoidal Dither Waveforms*

## THEORY OF OPERATION

### SPI Commands for Toggle/Dither Operations

SPI commands for setting up toggle and dither operation are as follows: write A/B select register (see Table 26), write software toggle bit register (see Table 27), write toggle/dither enable register (see Table 28), and write channel settings register of DAC Channel x (see Table 12).

*Table 26. Write A/B Select Register, Command 9*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0111 0010 | AB15 | AB14 | AB13 | AB12 | AB11 | AB10 | AB9 | AB8 | AB7 | AB6 | AB5 | AB4 | AB3 | AB2 | AB1 | AB0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

*Table 27. Write Software Toggle Bit Register, Command 10*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0111 0011 | TB15 | TB14 | TB13 | TB12 | TB11 | TB10 | TB9 | TB8 | TB7 | TB6 | TB5 | TB4 | TB3 | TB2 | TB1 | TB0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

*Table 28. Write Toggle/Dither Enable Register, Command 11*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0111 0100 | EN15 | EN14 | EN13 | EN12 | EN11 | EN10 | EN9 | EN8 | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

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### Write A/B Select Register

The command shown in Table 26 writes the A/B select register, AB[15:0], controlling access to DAC Input Register A and DAC Input Register B for each DAC channel.

Each of the 16 bits in AB[15:0] controls write access to the A or B register for the respective DAC channel. Set ABx to 0 for DAC Channel x to write to Input Register A, and set ABx to 1 to write to Input Register B. The default value is 0x0000.

For example, AB15 = 0 gives write access to the A Input Register of Channel 15, whereas AB15 = 1 gives write access to the B Input Register of Channel 15.

### Write Software Toggle Bit Register

The command shown in Table 27 writes the software toggle bit register, TB[15:0]. Each of the 16 bits in TB[15:0] acts as a software controlled toggle pin for the respective DAC channel. Note that the transition of a toggle bit is defined by the $\overline{CS}$/LD rising edge at the end of the command frame. The default value is 0x0000.

### Write Toggle/Dither Enable Register

The command shown in Table 29 writes the toggle/dither enable register, EN[15:0]. Set ENx = 1 to enable toggle or dither functionality for the DAC Channel x. Set ENx = 0 to disable toggle or dither functionality. The default value is 0x0000. The toggle/dither enable register is also used as a start or stop function for the dither operation.

In toggle mode, disabling toggle connects the DAC channel to Input Register A. In sinusoidal dither mode, disabling toggle causes the DAC channel to finish the sine wave cycle before connecting to Input Register A. This procedure requires the user to apply enough dither clock cycles to complete the sine wave cycle after toggle functionality is stopped.

***Table 29. Write Toggle/Dither Enable Register, Command 11***

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0111 0100 | EN15 | EN14 | EN13 | EN12 | EN11 | EN10 | EN9 | EN8 | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

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### Write Channel Settings Register of DAC Channel x

Command 1 in Table 12 writes the channel settings register of DAC Channel = A[3:0], where X is don't care and C represents the CRC code bits.

The mode bit selects toggle mode or sinusoidal dither mode. Set to 0 for toggle mode and set to 1 for sinusoidal dither mode (the default value is 0). The dither period can be selected with DIT_PER[2:0], as shown in Table 30 (the default value is 0b000). Note that dither signal frequency ($f_{SIGNAL}$) and dither clock frequency ($f_{DCK}$) are related, as shown in Table 30. Figure 51 illustrates the various dither period settings.

*Table 30. Dither Period Settings*

| DIT_PER[2:0] | N | $f_{SIGNAL}$ |
|---|---|---|
| 000 (Default) | 4 | $f_{DCK}/4$ |
| 001 | 8 | $f_{DCK}/8$ |
| 010 | 16 | $f_{DCK}/16$ |
| 011 | 32 | $f_{DCK}/32$ |
| 100 | 64 | $f_{DCK}/64$ |
| Other Settings Not Allowed | | |

The initial dither phase, $\varphi_0$, of the dither signal can be set with DIT_PH[1:0], as shown in Table 31 (the default value is 0b00). Figure 52 illustrates different initial phase values. The selection of initial dither phase ($\varphi_0$) is useful if two or more channels require sinusoidal waves with a relative phase offset between them. For example, if differential dithered signals are needed, Channel 0 and Channel 1 can be programmed to have the same dither clock signal and the same dither period. However, Channel 0 can be set to have Initial Phase 0° and Channel 1 can be set to have Initial Phase 180° (see Table 31).

*Table 31. Dither Phase Settings*

| DIT_PH[1:0] | Initial Dither Phase, $\varphi_0$ |
|---|---|
| 00 | 0° |
| 01 | 90° |
| 10 | 180° |
| 11 | 270° |

Note that if the initial dither phase ($\varphi_0$) is set to 90° or 270°, the first N/4 clock does not produce dither outputs (see Figure 52).

TD_SEL[1:0] control the toggle/dither select mux that chooses between the three toggle/dither pins and the software toggle/dither bit. The default value is 0b00 (see Table 32).

*Table 32. Toggle/Dither Clock Settings*

| TD_SEL[1:0] | Toggle/Dither Clock |
|---|---|
| 00 | Software toggle bit |
| 01 | TGP0 pin |
| 10 | TGP1 pin |
| 11 | TGP2 pin |

### DAISY-CHAIN MODE

Data transferred to the device from the SDI input is delayed by 32 SCK rising edges before being output at the SDO pin at the next SCK falling edge, suitable for clocking into the microprocessor on the next 32 SCK rising edges.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (that is, SCK, SDI, and $\overline{CS}$/LD). Such a daisy-chain series is configured by connecting the SDO of each upstream device to the SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single-input shift register that extends through the entire chain. Thus, the devices can be addressed and controlled individually by simply concatenating their input words. The first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then, the concentrated input data is transferred to the chain, using the SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the no operation command for all other devices in the chain. When $\overline{CS}$/LD is taken high, the SDO pin presents a high impedance output. Therefore, a pull-up resistor is required at the SDO pin of each device (except the last) for daisy-chain operation.

### POWER-DOWN MODE

For power sensitive applications, power-down mode can reduce the supply current whenever fewer than 16 DAC outputs are needed. When in power-down, the output amplifiers and reference buffers are disabled. The DAC outputs are put into a high impedance state, and the output pins are passively pulled to ground through individual 25 kΩ (minimum) resistors. Any channel or combination of channels can be put into power-down mode by using Command 8 (see Table 33). Command 8 writes the power-down register, P[15:0], controlling the power-down status of each DAC channel, where X is don't care and C represents the CRC code bits for error correction.

Channel x is powered down when Px = 1. Channel x is powered up when Px = 0. The default value is 0x0000.

Applying an update to DAC Channel x, Command 6 also powers up DAC Channel x. A software reset (RST = 1, Command 7) or a $\overline{CLR}$ low pulse also powers up all DAC channels. The power-down register always accurately reflects the power-down status of the DAC channels. Setting all 16 channels in power-down places the LTC2688 in a sleep mode (low current mode). That is, all active circuitry, including the internal reference and bias power down. Note that all on-chip registers retain their value during power-down. Normal operation resumes by undertaking one of the following actions:

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- Resetting one or more power-down (Px) bits in the power-down register (Command 8).
- Any command that involves an update of a DAC channel or a toggle/dither operation of a DAC channel.
- Pulling the asynchronous $\overline{\text{LDAC}}$ pin low (see the Pin Configuration and Function Descriptions section).
- Pulling the $\overline{\text{CLR}}$ pulse low powers up all DAC channels.
- Issuing a software reset by setting RST = 1 (Command 7).

When updating a powered down DAC channel, add wait time to accommodate the extra power-up delay (50 µs). If the entire chip is powered down, allow longer power-up times. The full chip power-up time depends on the charge state of the reference bypass capacitors.

Read the power-down register with Command 25. The data-word containing the power-down register appears at the SDO pin in the next command cycle, and has the same structure as Command 8.

*Table 33. Power-Down Command Structure, Command 8*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0111 0001 | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

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### ASYNCHRONOUS DAC UPDATE USING $\overline{LDAC}$

In addition to the update commands shown in Table 8 and Table 9, the asynchronous, active low $\overline{LDAC}$ pin updates all 16 DAC registers with the contents of the input registers. When $\overline{CS}$/LD is high, a low on the $\overline{LDAC}$ causes all DAC registers to be updated with the contents of the input registers. When $\overline{CS}$/LD is low, a low on the $\overline{LDAC}$ pin before the rising edge of $\overline{CS}$/LD powers up all DAC outputs, but does not cause the outputs to be updated. If $\overline{LDAC}$ remains low after the rising edge of $\overline{CS}$/LD, $\overline{LDAC}$ is recognized, the command specified in the 24-bit word is executed, and the DAC outputs are updated. The DAC outputs are powered up when $\overline{LDAC}$ is taken low, independent of the state of $\overline{CS}$/LD. If $\overline{LDAC}$ is low at the time $\overline{CS}$/LD goes high, any software power-down command that was specified in the input word is inhibited.

### FAULT DETECTION

The LTC2688 provides notifications of operational fault conditions. Use Command 30 to read the fault register. Table 34 lists the fault register bits and their associated trigger conditions for Command 13 and Command 30. The data-word containing the fault register appears at the SDO pin in the next command cycle (see the Read Commands section).

*Table 34. Fault Register Bits and Conditions*

| Bit | Fault Condition |
|---|---|
| TSF | Thermal shutdown fault. If die temperature $T_J$ > 160°C, TSF is set and thermal protection is activated. Disable using Command 7, Register Bit TSD_DIS. See the Thermal Overload Protection section for details. |
| CKF | Clock fault. If an invalid number for clock cycles is detected during a SPI sequence, CKF is set. The clock count must equal integer multiples of 32 (for example: 32, 64, 96, …). The use of only 24 clock cycles is also permitted. |
| CF | Command fault. This fault is triggered if the optional CRC error checking detects a data transmission error. To activate CRC error checking, use Command 7, Bit SPI_CRC. |

The device responds to a fault condition in two different ways.

- Fault register: the device sets the fault register flags (TSF, CFK, and CF) to indicate the cause of the fault. The user can read and reset the fault register with the read/write fault register (Command 30 and Command 13). Note that the TSF, CKF, and CF fault bits are not automatically reset, unless the device undergoes a power cycle, a low on the $\overline{CLR}$ pin, or a software reset.
- $\overline{FAULT}$ pin: when a fault condition is detected, the $\overline{FAULT}$ pin (Pin 38) engages. The $\overline{FAULT}$ pin is a digital open-drain output and pulls low in case of a fault. The $\overline{FAULT}$ pin releases on the next rising edge of $\overline{CS}$/LD.

Disable thermal protection and CRC error checking by using Command 7 to configure the TSD_DIS and SPI_CRC bits (see the Configuration Register section.) To reset the fault register, use Command 13 as shown in Table 35.

*Table 35. Write Fault Register, Command 13*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0111 0110 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TSF | CKF | CF | X | X | X | X | X | X | X | X |

*Table 36. Read Fault Register, Command 30*

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 0110 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TSF | CKF | CF | X | X | X | X | X | X | X | X |

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### CONFIGURATION REGISTER

*Table 37. Configuration Register Command, Command 7*

| Command Code | Byte 1 | | | | | | | | | | | | | Byte 2 | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0111 0000 | RST | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TSD_ DIS | EXT_ REF | SPI_ CRC | X | X | X | X | X | X | X | X |

The LTC2688 has a configuration register that can be set with Command 7 (see Table 37).

#### Software Reset

Use the RST bit for a software reset. Writing a 1 to RST performs a software reset. The RST bit self clears and the default value is 0.

#### Thermal Shutdown Disable

Use the TSD_DIS bit for thermal shutdown disable. When TSD_DIS = 1, thermal shutdown is disabled for all DAC channels. The default value is 0 (enabled).

#### External Reference Mode

Setting EXT_REF = 1 activates external reference mode and disables the REFCOMP charging current. The default value is 0.

#### SPI Cyclic Redundant Check Enable/Disable

The LTC2688 supports error checking for SPI transactions to verify that data has been received correctly in noisy environments. The error checking is based on a 6-bit cyclic redundancy check (CRC-6). To use this feature, the device controlling the LTC2688 must generate a 6-bit checksum that is added to the end of the third data byte of a 32-bit SPI transaction. The CRC error checking algorithm is based on the following polynomial:

$$C(x) = x^6 + x^1 + 1$$

If a data transmission error is detected, the faulty SPI transaction does not execute, a command integrity fault is issued, and the $\overline{\text{FAULT}}$ pin (Pin 38) triggers (see the Fault Detection section). Use Command 7 to enable or disable CRC error checking (see Table 37.

The SPI_CRC bit enables or disables the SPI CRC error checking. SPI_CRC = 1 enables CRC error checking.

By default, CRC error checking is disabled (SPI_CRC = 0). CRC error checking is always skipped for write and read configuration register commands and write and read fault register commands: Command 7, Command 13, Command 24, and Command 30.

#### Read Configuration Register

To read the configuration register, use Command 24. The data-word containing the current configuration register settings appears at the SDO pin in the next command cycle (see the Read Commands section).

### REFERENCE MODES

The LTC2688 has two reference modes: internal and external reference mode. In the internal reference mode, the reference voltage is generated by an on-board reference, whereas in external reference mode, the reference voltage is supplied by an external voltage reference. In both the internal and external reference modes, the voltage at the REF pin and the span range setting determine the full-scale voltage of each DAC channel.

The device includes a precision 4.096 V integrated reference with a typical temperature drift of ±2 ppm/°C. To use the internal reference, leave the REFCOMP pin floating (no dc path to ground). In addition, reset the EXT_REF bit in the configuration register (EXT_REF = 0) using Command 7.

A buffer is required for the internal reference to drive external circuitry. For reference stability and low noise, tie a 0.1 µF capacitor between REFCOMP and GND. In this configuration, the REF pin can drive up to 0.1 µF. To ensure stable operation, the capacitive load on the REF pin must not exceed the load on the REFCOMP pin.

To use an external reference, the REFCOMP pin must be tied to ground, which disables the output of the internal reference at start-up, so that the REF pin becomes a high impedance input. Apply the desired reference voltage at the REF pin after powering up, and set the EXT_REF bit to 1 using Command 7. The acceptable external reference voltage range is as follows:

$$2.0\ \text{V} \le V_{REF} \le V_{CC} - 0.6\ \text{V}$$

#### Integrated Reference Buffer

Each DAC channel has its own integrated high performance reference buffer. The buffers have very high input impedance and do not load the reference voltage source. These buffers shield the reference voltage from glitches caused by DAC switching and, thus, minimize DAC to DAC dynamic crosstalk. Typically, DAC to DAC crosstalk is 1 nV-sec (0 V to 5 V range). See Figure 17 in the Typical Performance Characteristics section.

### VOLTAGE OUTPUTS

The ability of an amplifier to maintain its rated voltage accuracy over a wide range of load conditions is characterized in its load regulation specification. The change in output voltage is measured in milliampere (mA) of forced load current change. The LTC2688 high voltage, rail-to-rail output amplifier has guaranteed load regulation

## THEORY OF OPERATION

when sourcing or sinking up to 20 mA with supply headroom as low as 2.2 V.

DC output impedance is equivalent to load regulation, and can be derived from it by simply calculating a change in units from µV/mA to Ω. The dc output impedance of the amplifier is typically 0.07 Ω when driving a load with at least 2.2 V of headroom.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the typical channel resistance of the output devices—70 Ω for the high-side output device and 30 Ω for the low-side output device. Worst case channel resistances for the high-side and low-side output devices are estimated to be 110 Ω and 60 Ω, respectively. For example, when sourcing 1 mA, the maximum output voltage (below $Vx^+$) is 70 Ω × 1 mA = 70 mV. See Figure 10 and Figure 11 in the Typical Performance Characteristics section. The amplifiers are stable, driving capacitive loads of up to 1 nF.

### THERMAL OVERLOAD PROTECTION

The LTC2688 protects itself from damage if the die temperature exceeds 160°C. Each of the 16 DAC channels has an independent temperature sensor. If a particular channel overheats, it shuts itself down and triggers a TSF fault. That is, the TSF flag in the fault register is set (see Table 34), and the open-drain $\overline{FAULT}$ pin (Pin 38) pulls low. Moreover, the bit corresponding to the channel in thermal shutdown is set in both the power-down register (see Table 33) and the thermal shutdown status register (see Table 38). These registers can be read using Command 25 and Command 31, respectively. All other channels that did not overheat continue to operate normally. However, if all 16 channels trigger thermal shutdown, the entire chip powers down, including reference and bias circuitry. When triggered, all thermally shut down channels remain in shutdown mode, even if the temperature has fallen. To exit thermal shutdown mode. the temperature must first decrease to below about 150°C on all channels. The user can then power up the shutdown channels in one of four different ways:

- Reset the $\overline{FAULT}$ register (Command 13), and reset the power-down register (Command 8).
- Issue a software reset using Command 7.
- Power cycle the device.
- Issue a reset on the $\overline{CLR}$ pin (Pin 21). A $\overline{CS}$/LD rising edge releases the pin regardless of die temperature.

Table 38 shows the structure of the thermal shutdown status register, which can be read with Command 31. TSDx represents the thermal shutdown status of Channel x. Because the total load current of the device can easily exceed 100 mA, carefully evaluate the die heating potential of the system design. Grounded loads as low as 1 kΩ can be used without resulting in excessive heat. Disable thermal protection by using the SPI Command 7 to set the TSD_DIS bit in the configuration register.

***Table 38. Read Thermal Shutdown Status Register, Command 31***

| Command Code | Byte 1 | | | | | | | | Byte 2 | | | | | | | | Byte 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 0111 | TSD 15 | TSD 14 | TSD 13 | TSD 12 | TSD 11 | TSD 10 | TSD 9 | TSD 8 | TSD 7 | TSD 6 | TSD 5 | TSD 4 | TSD 3 | TSD 2 | TSD 1 | TSD 0 | X | X | C/X | C/X | C/X | C/X | C/X | C/X |

## APPLICATIONS INFORMATION

### PRINTED CIRCUIT BOARD LAYOUT

The excellent 70 µV/mA load regulation and ±2 µV dc crosstalk performance of the LTC2688 are achieved partially by minimizing common-mode resistance of signal and power ground. As with any high resolution converter, clean board grounding is important. A low impedance analog ground plane is necessary, as are star grounding techniques. The user is advised to keep the board layer used for star ground continuous to minimize ground resistance. That is, use the star ground concept without using separate star traces. Keep resistance from REFL pin to GND as low as possible.

For optimal performance, stitch the ground plane with arrays of vias on 150 mil to 200 mil centers to form a connection with ground pours from the other board layers. These layout techniques reduce overall ground resistance and minimize ground loop area.

The mechanical stress caused by soldering parts to a PCB may cause the reference output voltage to shift and the temperature coefficient to change. To reduce the effects of stress related shifts, mount the LTC2688 near the short edge of a PCB or in a corner. Using circuit boards that are thicker and smaller, with a lower aspect ratio, reduces mechanical stress. In addition, slots can be cut into the PCB on two sides of the device to reduce stress.

When using the WLCSP package, follow the layout guidelines in AN-617 Application Note, *Wafer Level Chip Scale Package*.

### Using the LTC2688 in 5 V Single-Supply Systems

The LTC2688 can be used in single-supply systems simply by connecting the V− pins to ground along with REFL and GND, while $Vx^+$ and VCC are connected to a 5 V supply. IOVCC can be connected to the 5 V supply or to a logic supply voltage of lower than 5 V.

With the internal reference, use the 0 V to 5 V span for DAC channel outputs. As with any rail-to-rail device, the output is limited to voltages within the supply range. Because the outputs of the device cannot go below ground, the lowest DAC code may limit the output, as shown in Figure 54. Similarly, limiting can occur near full-scale if full-scale error (FSE = $V_{OS}$ + GE) is positive, or if $Vx^+$ is less than the full scale voltage (see Figure 55).

The multiplexer is fully functional in single-supply operation. However, output voltages are limited to between ground and 3.6 V ($Vx^+$ = 5 V).

More flexibility can be afforded by using an external reference. For example, by using a 2.048 V reference, such as the LTC6655, ranges between 0× to 2× and 0× to 4× can be selected, which give full-scale voltages of 2.5 V and 5 V, respectively. Furthermore, the device can be configured for reset to zero scale or midscale codes (see the Span Selection and Channel Settings section).

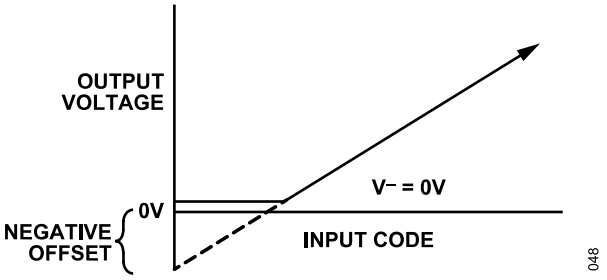



*Figure 54. Effects of 0 V to 5 V Output Range for Single-Supply Operation, Overall Transfer Function*

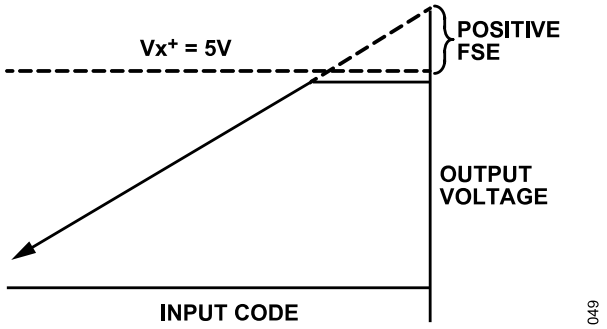



*Figure 55. Effect of Negative Offset for Codes Near Zero Scale*

## COMMAND ADDRESSES

The syntax of the read commands are identical to the corresponding write commands. For instance, Command 24 (read configuration register bits) has the same syntax as the write configuration register, Command 7. The bit structure of Command 16 and Command 17 is the same as Command 1. Blank cells in Table 39 mean not applicable.

***Table 39. Write Commands***

| Command No. | Instruction | Command Address | Bit(s) | Bit Name | Description | Reset Value | R/W |
|---|---|---|---|---|---|---|---|
| 0 | Write code to DAC Channel x | 0x0 | [23:8] | D15 to D0 | 16-bit DAC code of Channel A[3:0]. | All 0 | W |
| 1 | Write channel settings to DAC Channel x (A[3:0]) | 0x1 A[3:0] | 19 | Mode | Toggle mode register. When the mode bit is set, the device is in toggle mode. When the mode bit is reset, the device is in dither mode. | 0 | R/W |
| | | | [18:17] | DIT_PH1, DIT_PH0 | Dither phase, sets the phase of the sinusoidal dither signal (see Table 31). | 00 | R/W |
| | | | [16:14] | DIT_PER2, DIT_PER1, DIT_PER0 | Dither Period N, sets the Period N of sinusoidal dither signal (see Table 30). | 000 | R/W |
| | | | [13:12] | TD_SEL1, TD_SEL0 | Controls the toggle select mux that chooses between the three toggle pins and the software pin (see Table 32). | 00 | R/W |
| | | | [11:8] | S3 to S0 | Span settings (see Table 13 and Table 14). | 0x0 | R/W |
| 2 | Write offset adjust to DAC Channel x | 0x02 A[3:0] | [23:8] | O13 to O0 | DAC offset adjust value of Channel A[3:0]. | All 0 | W |
| 3 | Write gain adjust to DAC Channel x | 0x03 A[3:0] | [23:8] | G15 to G0 | DAC gain adjust value of Channel A[3:0]. | All 0 | W |
| 4 | Write code to DAC Channel x, update DAC Channel x | 0x04 A[3:0] | [23:8] | D15 to D0 | 16-bit DAC code of Channel A[3:0]. | All 0 | W |
| 5 | Write code to DAC Channel x, update all DAC channels | 0x05 | [23:8] | D15 to D0 | 16-bit DAC code of Channel A[3:0]. | All 0 | W |
| 6 | Update DAC Channel x | 0x06 A[3:0] | [5:0] | | Updates the DAC register for Channel x. | | |
| 7 | Write Configuration Register | 0x70 | 23 | RST | Software reset. Writing a 1 to RST performs a software reset. | 0 | W |
| | | | 10 | TSD_DIS | Thermal shutdown disable. When TSD_DIS = 1, thermal shutdown is disabled for all DAC channels. | 0 | R/W |
| | | | 9 | EXT_REF | External reference mode. Setting EXT_REF = 1 sets the external reference mode and disables the REFCOMP charging current. | 0 | R/W |
| | | | 8 | SPI_CRC | SPI cyclic redundancy check. Setting SPI_CRC = 1 enables the CRC. | 0 | R/W |
| 8 | Write power-down register | 0x71 | [23:8] | P15 to P0 | Power-down register controlling the power-down status of all DAC channels. P[15:0] controls DAC Channel x. P[15:0] = 1 powers down the DAC Channel x, P[15:0] = 0 powers up the DAC Channel x. | All 0 | R/W |
| 9 | Write A/B select register | 0x72 | [23:8] | AB15 to AB0 | A/B select register controlling access to DAC Input Register A and Input Register B for each DAC channel. ABx controls DAC Channel x. Reset ABx to write to Input Register A, set ABx to write to Input Register B. | All 0 | R/W |
| 10 | Write software toggle bit register | 0x73 | [23:8] | TB15 to TB0 | Software toggle bit register acting as a software controlled toggle bit for each DAC channel. TBx controls DAC Channel x. When TBx changes from 1 to 0, DAC Channel x updates to Register A. When TBx changes from 0 to 1, DAC Channel x updates to Register B. | All 0 | R/W |
| 11 | Write toggle/dither enable register | 0x74 | [23:8] | EN15 to EN0 | Toggle/dither enable bit register. ENx controls DAC Channel x. Set ENx to enable toggle/dither functionality. Reset ENx to disable toggle/dither functionality. | All 0 | R/W |

## COMMAND ADDRESSES

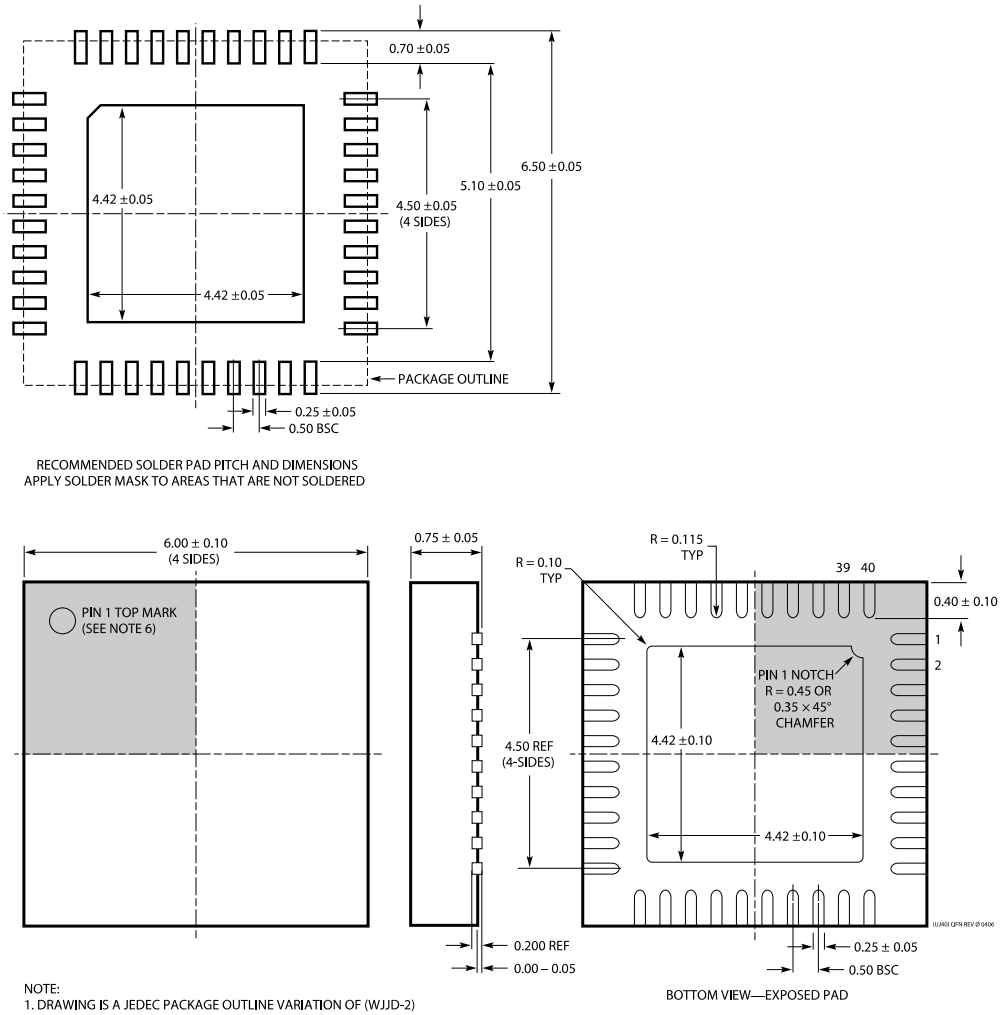
*Table 39. Write Commands*

| Command No. | Instruction | Command Address | Bit(s) | Bit Name | Description | Reset Value | R/W |
|---|---|---|---|---|---|---|---|
| 12 | Write mux control register | 0x75 | 18 | ENMUX | Enable mux. Mux is enabled when ENMUX = 1, and mux is disabled when ENMUX = 0. | 0 | W |
| | | | [17:8] | M8 to M0 | Mux address register for accessing signals at the MUXpin. See Table 22 for address to signal assignment. | All 0 | W |
| 13 | Write fault register | 0x76 | 10 | TSF | Thermal shutdown bit. | 0 | R/W |
| | | | 9 | CKF | Clock integrity fault bit. | 0 | R/W |
| | | | 8 | CF | Command integrity fault bit. | 0 | R/W |
| 14 | Write code to all DAC channels | 0x78 | [23:8] | D15 to D0 | 16-bit DAC code written to all channels. | All 0 | W |
| 15 | Write code to DAC Channel x, update DAC Channel x | 0x79 | [23:8] | D15 to D0 | 16-bit DAC code written to all channels and all channels are updated. | All 0 | W |
| 16 | Write channel settings to all DAC channels | 0x7A | [19:8] | | See Command 1 for the bit structure. | All 0 | R/W |
| 17 | Write channel settings to all DAC channels, update all DAC channels | 0x7B | [19:8] | | See Command 1 for the bit structure. | All 0 | R/W |
| 18 | Update all DAC channels | 0x7C | | | Updates the DAC register for all channels. | 0x0 | R/W |

*Table 40. Read Commands*

| Command No. | Command/Address | Description |
|---|---|---|
| 20 | 0x8, A[3:0] | Read offset and gain adjusted code of DAC Channel x. |
| 21 | 0x9, A[3:0] | Read channel settings of DAC Channel x |
| 22 | 0xA, A[3:0] | Read offset adjust of DAC Channel x |
| 23 | 0xB, A[3:0] | Read gain adjust of DAC Channel x |
| 24 | 0xF0 | Read configuration register |
| 25 | 0xF1 | Read power-down status |
| 26 | 0xF2 | Read A/B select register |
| 27 | 0xF3 | Read software toggle bit register |
| 28 | 0xF4 | Read toggle/dither enable register |
| 29 | 0xF5 | Read mux control register |
| 30 | 0xF6 | Read fault register |
| 31 | 0xF7 | Read thermal shutdown status register |
| 32 | 0xFF | No operation |

## OUTLINE DIMENSIONS




NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

***Figure 56. 40-Lead Lead Frame Chip Scale Package [LFCSP]***
***6 mm × 6 mm Body and 0.75 mm Package Height***
***05-08-1728***
***Dimensions shown in millimeters***

## OUTLINE DIMENSIONS

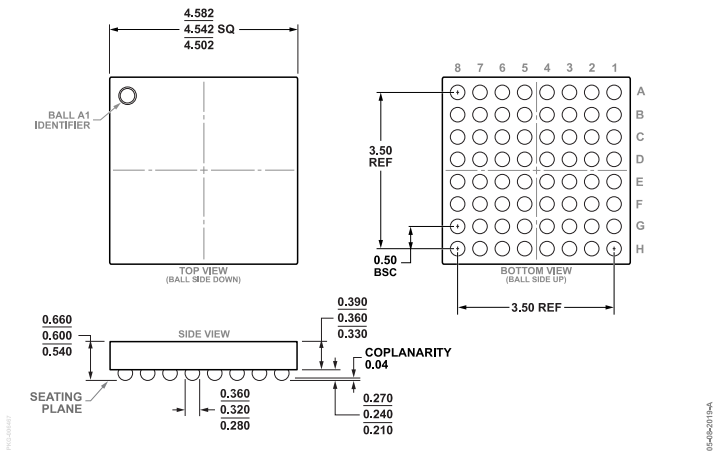



*Figure 57. 64-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-64-5)*
*Dimensions shown in millimeters*

Updated: August 12, 2021

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| LTC2688CUJ-16#PBF | 0°C to +70°C | LFCSP:LEADFRM CHIP SCALE | | 05-08-1728 |
| LTC2688CUJ-16#TRPBF | 0°C to +70°C | LFCSP:LEADFRM CHIP SCALE | Reel, 2000 | 05-08-1728 |
| LTC2688IUJ-16#PBF | −40°C to +85°C | LFCSP:LEADFRM CHIP SCALE | | 05-08-1728 |
| LTC2688IUJ-16#TRPBF | −40°C to +85°C | LFCSP:LEADFRM CHIP SCALE | Reel, 2000 | 05-08-1728 |
| LTC2688HUJ-16#PBF | −40°C to +125°C | LFCSP:LEADFRM CHIP SCALE | | 05-08-1728 |
| LTC2688HUJ-16#TRPBF | −40°C to +125°C | LFCSP:LEADFRM CHIP SCALE | Reel, 2000 | 05-08-1728 |
| LTC2688HCB-16#TRPBF | −40°C to +125°C | WLCSP:WAFER LEVEL CHIP SCALE | Reel, 5000 | CB-64-5 |

[1] Z = RoHS Compliant Part.

## EVALUATION BOARDS

| Model[1] | Description |
|---|---|
| DC2873A-B | LTC2688 16-Bit Evaluation Board (LFCSP Package) |

[1] The DC2873A-B is RoHS compliant.