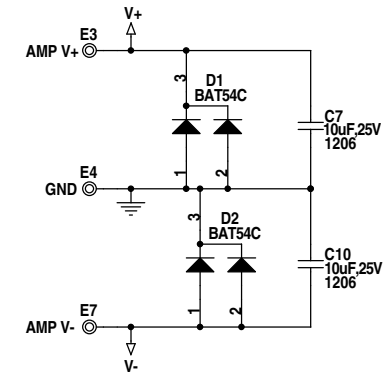


NOTES: UNLESS OTHERWISE SPECIFIED

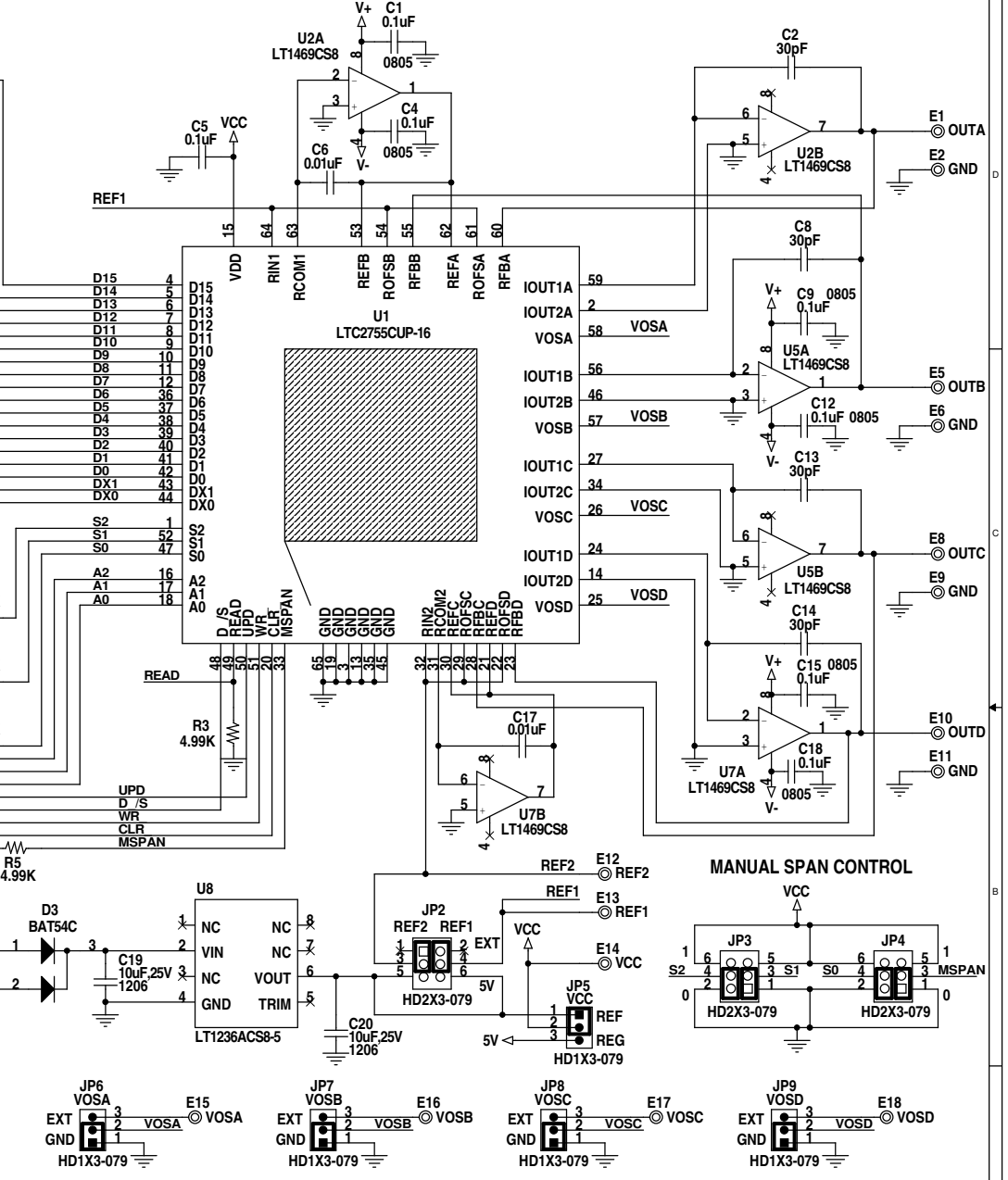
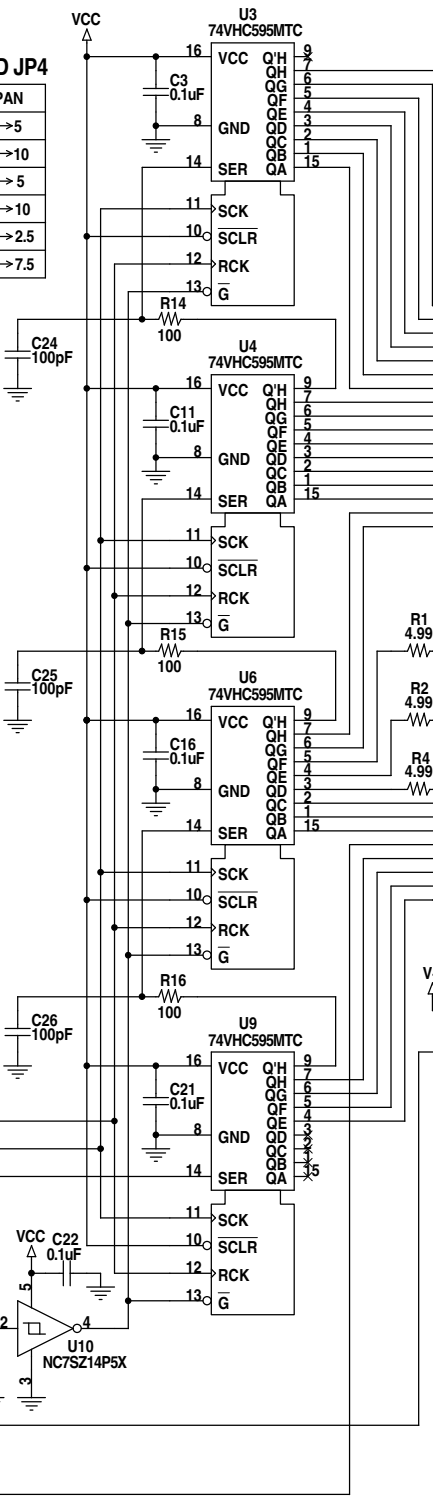
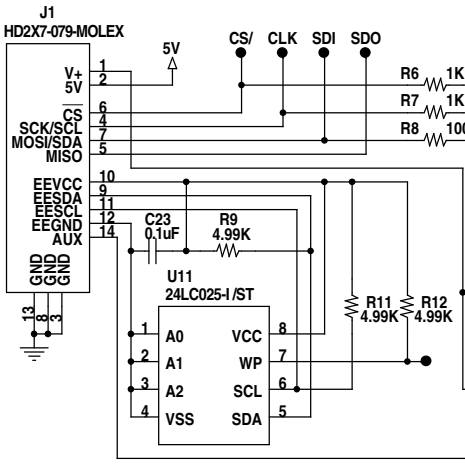
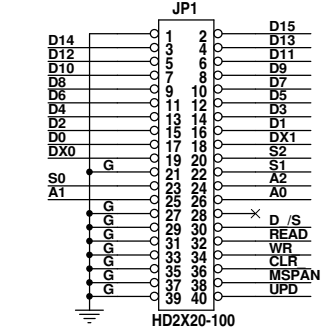
1. ALL RESISTORS ARE IN OHMS, 0402.
- ALL CAPACITORS ARE IN MICROFARADS, 0402.
2. INSTALL SHUNTS ON JUMPERS AS SHOWN.

FOR JP3 AND JP4

S2	S1	S0	SPAN
0	0	0	0 → 5
0	0	1	0 → 10
0	1	0	-5 → 5
0	1	1	-10 → 10
1	0	0	-2.5 → 2.5
1	0	1	-2.5 → 7.5



PARALLEL INTERFACE



CUSTOMER NOTICE

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.

THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

CONTRACT NO.
 APPROVALS
 DRAWN:
 CHECKED:
 APPROVED:
 ENGINEER: MARK T.
 DESIGNER: KIM T.

LINEAR TECHNOLOGY

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QUAD, PARALLEL, IOUT, 16-BIT DAC

DATE: Tuesday, October 02, 2007

REV A-1

SHEET 1 OF 1