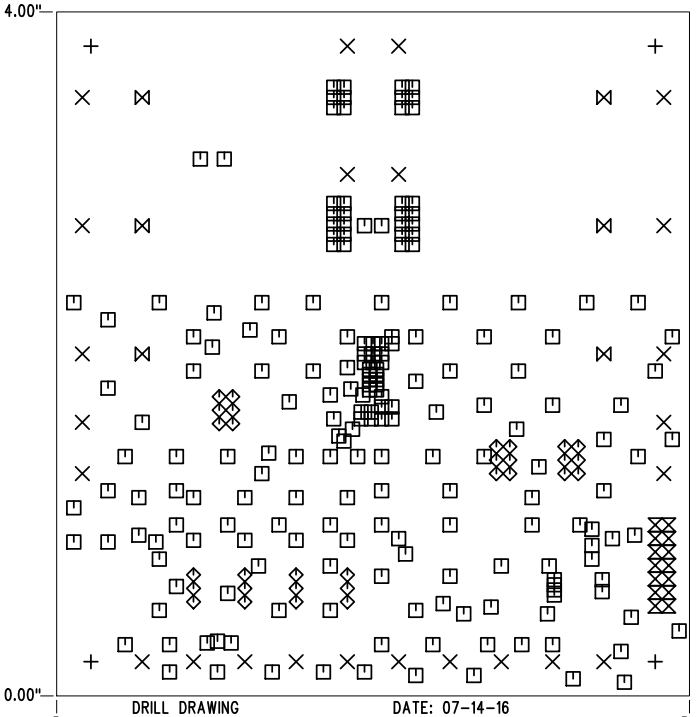
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
–	1	1ST PROTOTYPE	SAL A.	07-14-16

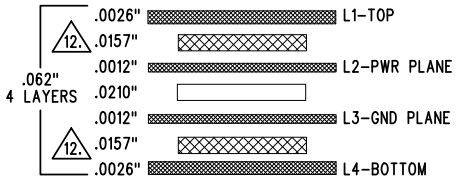
SHOWN FROM TOP SIDE



DRILL DRAWING
LINEAR TECHNOLOGY
DC2561A-1 LTC2992IDE DUAL WIDE RANGE I2C POWER MONITOR
DATE: 07-14-16

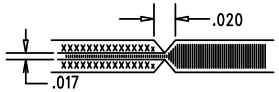
SIZE	QTY	SYM	PLATED	TOL
0.19	4	+	NO	+/-0.003"
0.063	24	X	YES	+/-0.003"
0.012	204	□	YES	+/-0.003"
0.035	30	◇	YES	+/-0.003"
0.04	14	⧖	YES	+/-0.003"
0.207	6	⋈	YES	+/-0.003"

LAYER STRUCTURE



NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC-A-600.
2. MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.
   -FINISHED THICKNESS TO BE 0.062" +/- .005"
   -TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
   -FLAMMABILITY RATING: 94 V-O MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN. 0.00" ARE PRIMARY DATUMS.
4. DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
   -ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
   -HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
5. FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
   -GOLD IMMERSION BOTH SIDES.
   -FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
7. PCBS ARE TO BE RoHS COMPLIANT.
8. SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



9. A. CONTROLLED 50 OHM +/-10% IMPEDANCE FOR SINGLE ENDED STRIP LINE FOR LAYER 1-2 AND LAYER 6-5, USING 0.006" TRACE AT 2GHz FREQ.

10. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
0.XX" = ±0.01"
0.XXX" = ±0.005"
INTERPRET DIM AND TOL PER ASME Y14.5M-1994
THIRD ANGLE PROJECTION

APPROVALS	
PCB DES.	KIM T.
APP ENG.	SAL A.

SCALE = NONE

1630 MCCARTHY BLVD
MILPITAS, CA 95035
PH: (408)432-1900
www.linear.com

TITLE: FABRICATION DRAWING

DUAL WIDE RANGE I2C POWER MONITOR

SIZE	IC NO.	REV
N/A	LTC2992IDE DEMO CIRCUIT 2561A	1

FILENAME: DC2561A-1.PCB SHT 1 OF 1