DESCRIPTION

Demo Circuit 449 is a VRM for powering AMD Hammer™ CPUs in desktop or server computers. It has two inputs (12V ±10% and 5V) and one output ($V_{CC\text{-}CORE}$ from 0.8V to 1.55V at 45A max). DC449 has two different versions: DC449A-A is a *2-phase* VRM using the LTC3719 PolyPhase® controller, designed primarily for desktop applications, while DC449A-B is a *4-phase* VRM using the LTC3719 and LTC1629-6 PolyPhase controllers for server applications. The PolyPhase technique minimizes the input and output ripple currents, thereby reducing the size and cost of input and output capacitors. The output voltage is programmed by the internal VID attenuator of the LTC3719, which complies with AMD Hammer VRM VID table.

It is recommended that this demo board be evaluated on a VRM host test board as specified by the *AMD Hammer Processor VRM Design Guide*, which specifies the input, output and control interfaces for the VRM. A simplified schematic of the AMD Hammer processor VRM test board is shown in Figure 1.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary

PARAMETER	CONDITION	VALUE
Input Voltage		10.8V–13.2V, 12V typical
Output Voltage		VID programming. 0.8V–1.55V
Output Current	Maximum, with Air Flow (100LFM)	45A at 1.55V output
Load Regulation	0A to full load, with AVP	≤30mV typical
Transient Response (DC449A-A)	Load step between 0A and 20A, 30A/μs slew rate, with AVP	≤50mV
Transient Response (DC449A-B)	Load step between 0A and 14A, 30A/μs slew rate, with AVP	≤50mV
Efficiency (DC449A-A)	Room temperature, V_{IN} = 12V, V_{OUT} = 1.55V	86.2% at 42A load current 74.7% at 3A load current
Efficiency (DC449A-B)	Room temperature, V_{IN} = 12V, V_{OUT} = 1.55V	87.3% at 45A load current 66% at 3A load current

OPERATING PRINCIPLES

Demonstration circuit 449A-A features the LTC3719, while demo circuit 449A-B features the LTC3719 and LTC1629-6 PolyPhase current mode controllers. Each controller is capable of driving two synchronous buck channels 180 degrees out of phase to reduce the input and output capacitor ripple current. LTC3719 has an internal VID table compatible to the AMD Hammer processor VRM. In demonstration circuit 449A-B, the LTC1629-6 provides the clock out signal to synchronize the LTC3719 to achieve 4-phase operation.

Figure 7 shows the schematic diagram of 449A-A. In order to supply 45A current to the output, two Si7448DPs are paralleled for each top switch and three Si7448DPs are paralleled for each bottom switch. The switching frequency is about 150kHz. This results in the use of a 1.0μH/21A inductor in each phase. The demo board design uses a Sumida CEP125-1R0 inductor. Any inductor with a similar inductance value and 21A current rating should do the job. The current sensing resistor is about 2mΩ.

Figure 8 shows the schematic diagram of 449A-B. In order to supply 45A current to the output, one Si7448DP is used for each top or bottom MOSFET switch. The switching frequency is about 210kHz. This results in the use of a 0.8μH/13.2A inductor in each phase. The demo board design uses a Sumida CDEP105-0R8MC-88 in-

ductor. Any inductor with a similar inductance value and 13A current rating should do the job. The current sensing resistor is about 3mΩ.

Different output currents may require different inductors and current sensing resistors. Refer to the LTC3719 data sheet for more design information.

The transient load test of the VRM is conducted with the network specified by the AMD Hammer Processor VRM host test board schematic, as shown in Figure 1. To handle the load transient resulting from high current slew rate and large load steps, low ESR capacitors are required at the output terminal. To minimize the VRM profile, this design uses ten ceramic capacitors (22µF/6.3V, X5R) for the output cap. With a 20A (14A

for the 449A-B) load step and 30A/µs current slew rate, as shown in Figure 5 and Figure 6, the output voltage variation is less than ±50mV.

Active voltage positioning (AVP) can be implemented with the addition of R4 and R7. This AVP technique reduces the output capacitor with no loss in the efficiency. (See Linear Technology Design Solution 10 for more details on active voltage positioning.)

Figure 4 shows the measured overall efficiency vs. load current. With a 12V input and 1.55V output, the overall efficiency is above 86% at 42A output for the 449A-A and 87% at 45A for the 449A-B. Good efficiency is also maintained in the load range between 3A and 42A (45A for the 449A-B).

QUICK START PROCEDURE

Demonstration circuit 449 is easy to set up to evaluate the performance of the LTC3719 and LTC1629-6. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below:

1. Mount the DC449 on the VRM host test board.

2. Connect a 12V/10A power supply to the VIN 12V terminal and a 5V/0.5A power supply to VIN 5V terminal on the VRM test board. Connect ENABLE pin on the test board to VIN 5V.

3. Connect output load to the Vcc core terminal of the VRM test board. If a constant-current mode electronic load is used, preset the load current to 0.2A. Otherwise, the I-V characteristics of the electronic load may trigger the foldback current limit of the LTC3719 and prevent normal start-up.

4. Close all the VID jumpers on the test board (VID = 0000). Apply a 5V input voltage on VIN 5V first. Then,

apply a 12V ±10% input voltage on VIN 12V. The regulation of output voltage should be measured at VSEN+ and VSEN– terminals on the VRM test board. It should be in the range of 1.55V ±35mV.

5. The core output current may increase after the CORE voltage reaches the steady state. **It is necessary to apply a cooling fan to the board if the output current is beyond 35A.** When the output current is 42A (45A for the 449A-B) and VID = 00000, the input current should be less than 8A.

6. To properly evaluate the efficiency of the DC449, the input and output voltages should be measured across the input and output capacitors of DC449.

7. Connect the ENABLE pin to GND. The Vcc core output should be shut down. The Vcc core output voltage should come back in 1.55V ±35mV range if the ENABLE pin is connected to VIN 5V again.

L_{IN} = INPUT SMOOTHING CHOKE
        0.5µH 4-PHASE
        1.0µH 2- OR 3-PHASE
C_{IN} = OSCON 16SA1000M
N1 = 6
C1 = OSCON 4SP820M
N2 = 4
C2 = MURATA GRM44-1 107k 6.3V
N3 = 10
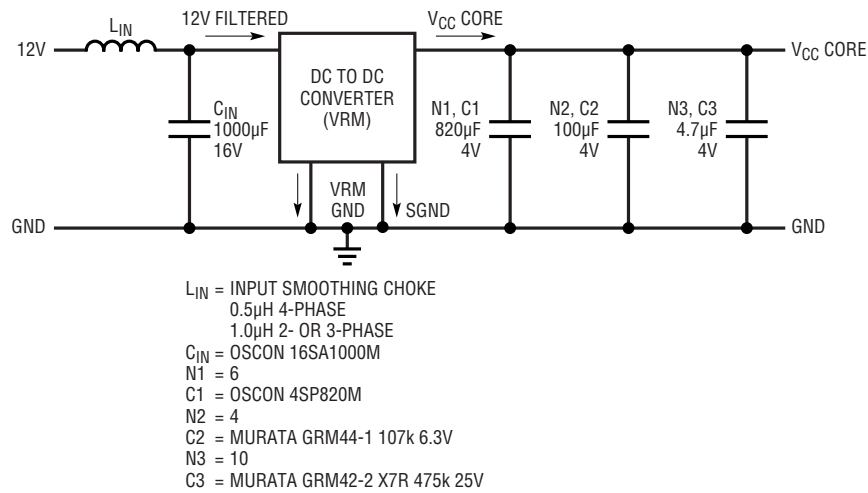C3 = MURATA GRM42-2 X7R 475k 25V

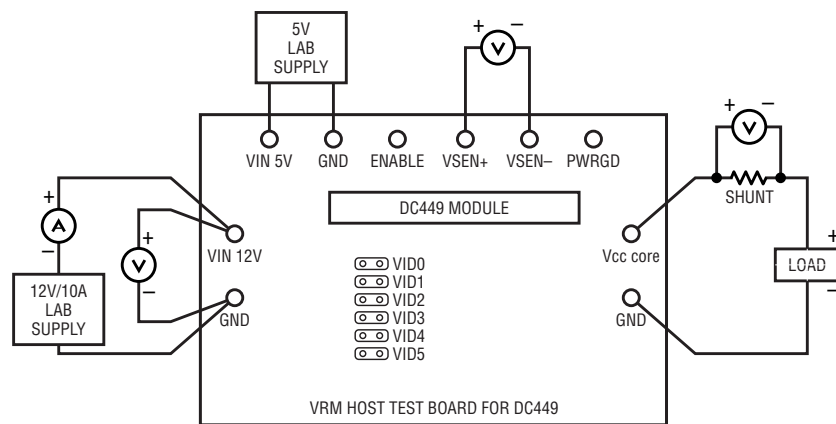**Figure 1. AMD Hammer® Processor VRM Host Test Board Schematic (simplified)**

Figure 2. Proper Measurement Equipment Setup

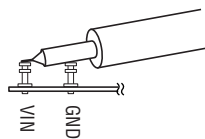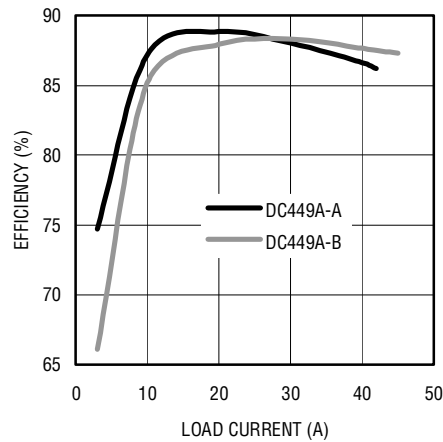**Figure 3. Scope Probe Placement for Measuring Input or Output Ripple**
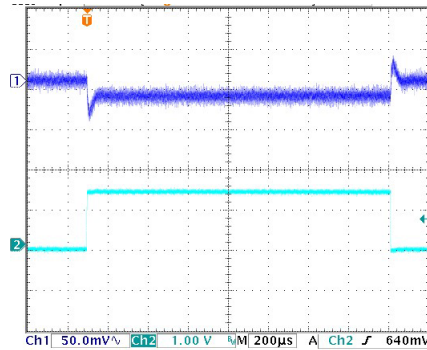
Figure 4. Measured Efficiency vs. Load Current

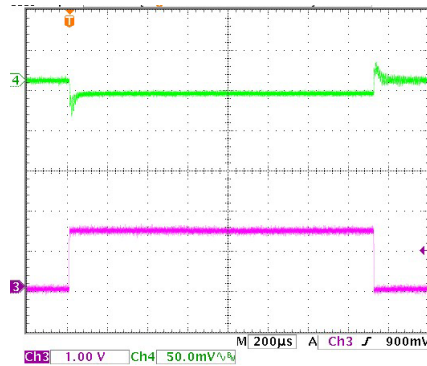**Figure 5. Load Transient Waveforms at 20A Step and 30A/µs Slew Rate (DC449A-A)**

Figure 6. Load Transient Waveforms at 14A Step and 30A/µs Slew Rate (DC449A-B)

Figure 7. Schematic for DC449A-A

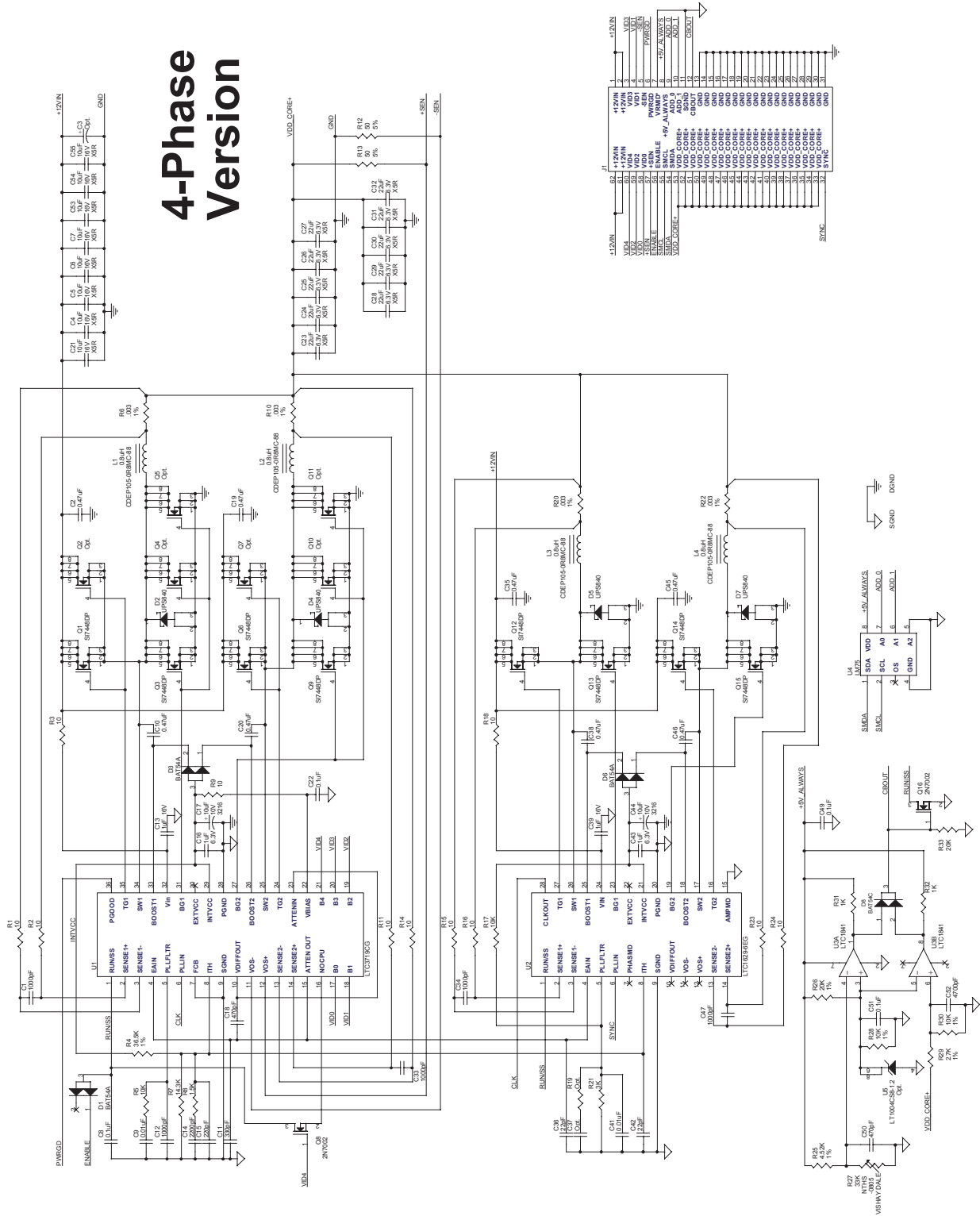**Figure 8. Schematic for DC449A-B**