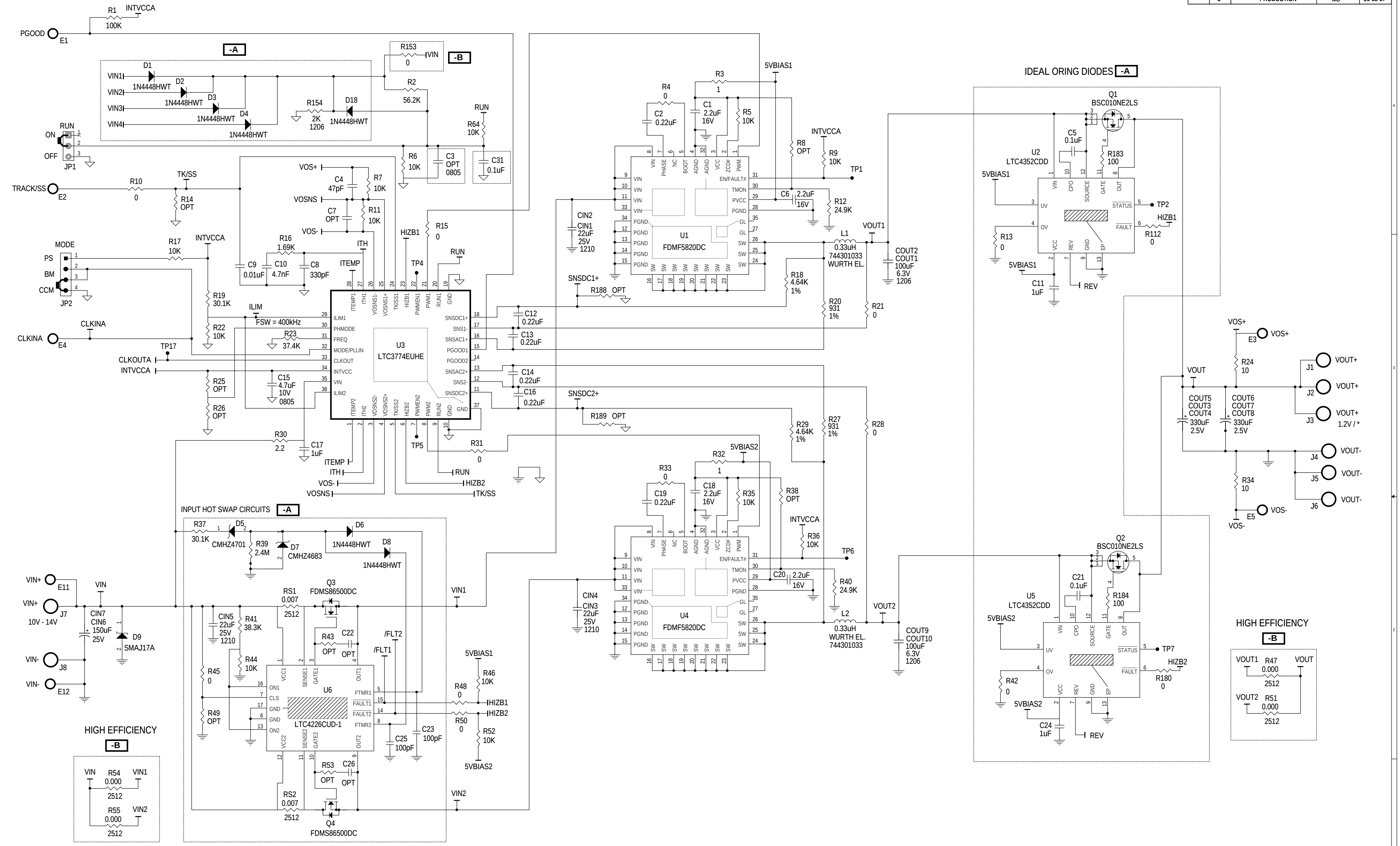
REVISION HISTORY				
ECO	REV	DESCRIPTION	APPROVED	DATE
—	3	PRODUCTION	MS	01-18-17



*		IOUT(MAX)
-A	N+1 MOSFET FAILURE PROTECTION	90A
-B	HIGH EFFICIENCY CONVERTER	120A

NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 0603.
2. ALL CAPACITORS ARE 0603.

-A: STUFFED ON -A ASSEMBLY ONLY
-B: STUFFED ON -B ASSEMBLY ONLY
OPT, OPTIONAL: NOT STUFFED

APPROVALS	
PCB DES.	LT
APP ENG.	MS

SCALE = NONE

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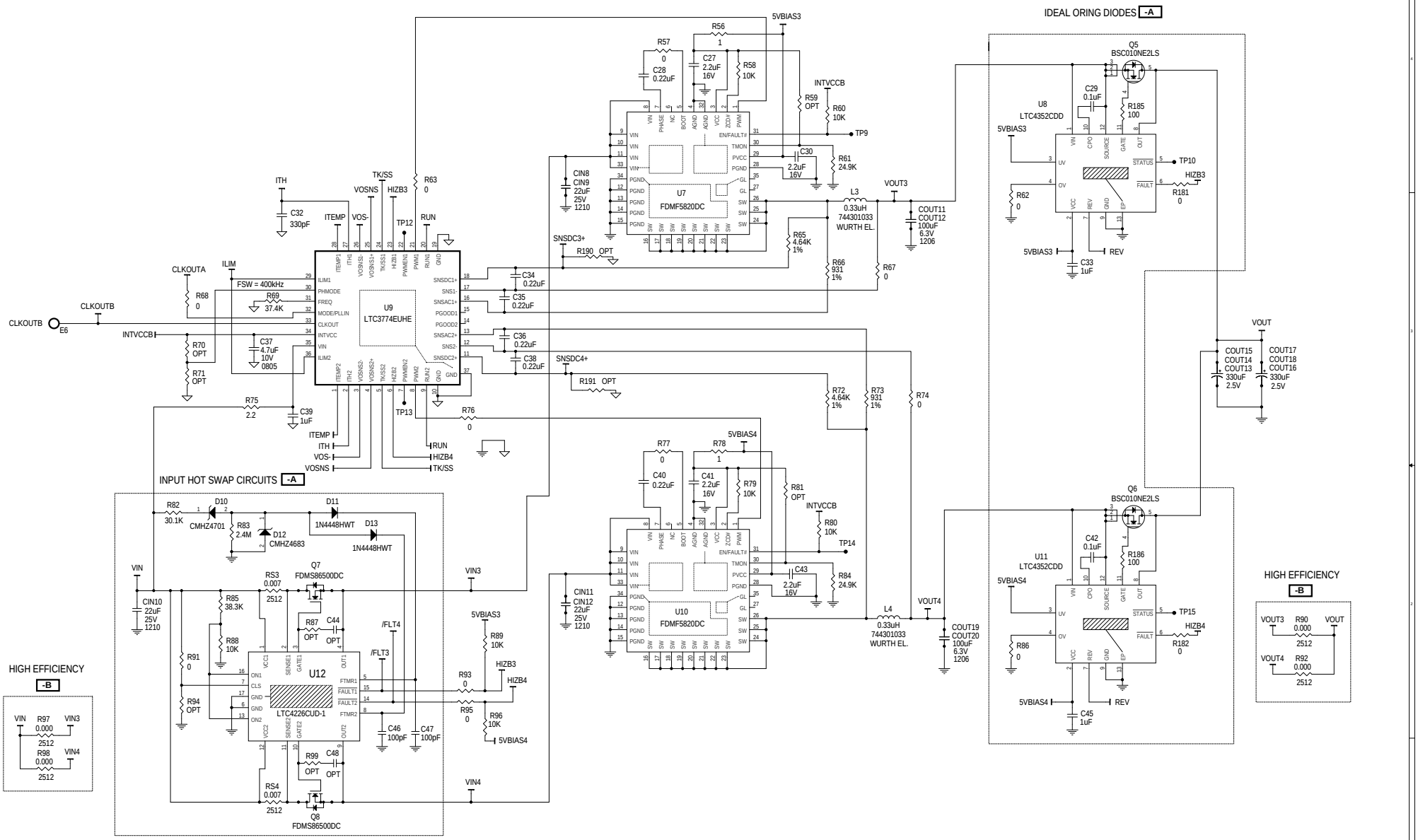
TITLE: SCHEMATIC
4 PHASE HIGH CURRENT STEP-DOWN CONVERTER WITH VERY LOW DCR INDUCTOR

SIZE	IC NO.	REV.
N/A	LTC3774EUHE DC2111A	3

DATE: Wednesday, January 18, 2017 SHEET 1 OF 3



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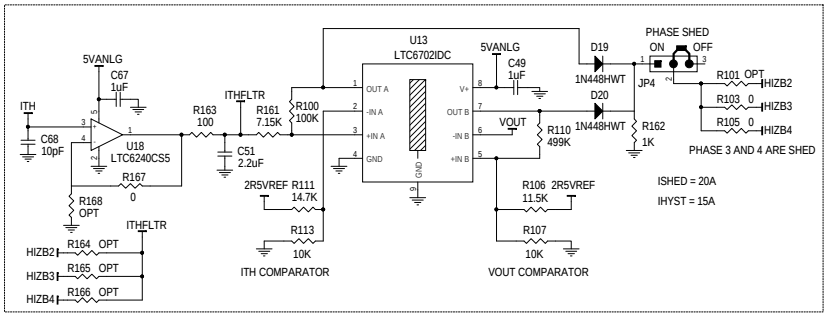
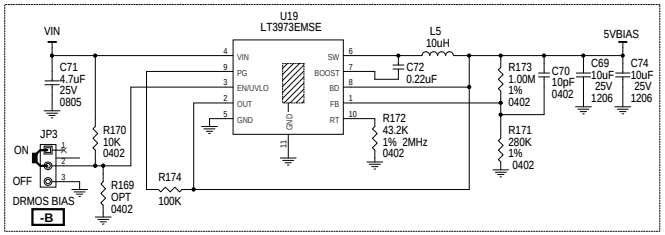
N/A	LTC3774EUHE DC2111A	3

DATE: Wednesday, January 18, 2017 SHEET 2 OF 3

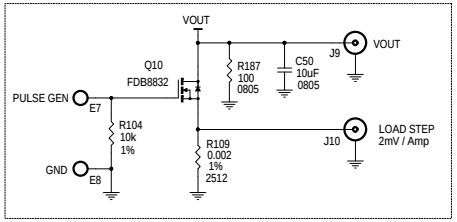
OPTIONAL PHASE SHEDDING CIRCUIT



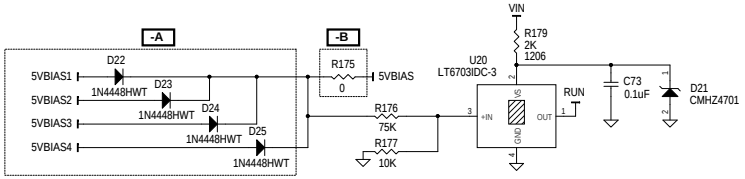
DRMOS BIAS SUPPLY FOR HIGH EFFICIENCY CONVERTER -B



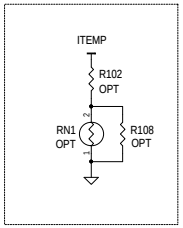
DYNAMIC LOAD CIRCUIT



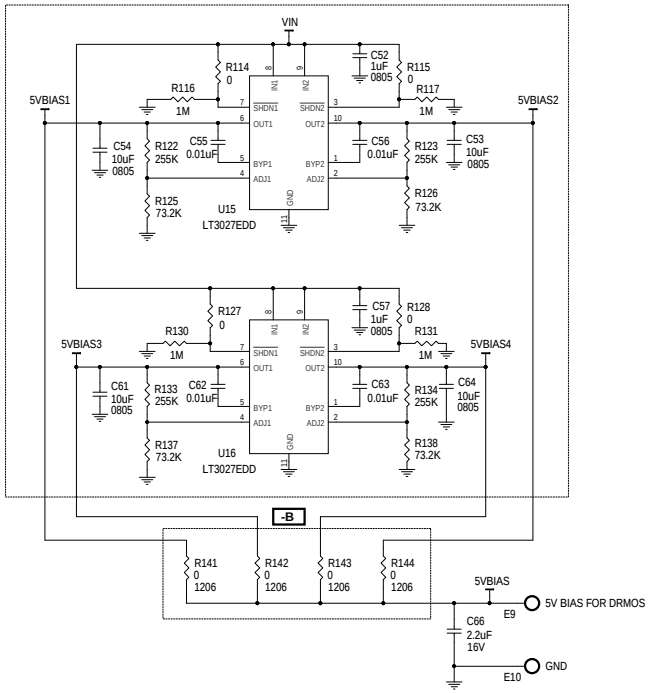
Note 1:
The 5.5VBIAS voltages were increased from 5.0V to 5.5V to comply with the FDMF5820DC PCN.
This PCN changed the maximum allowable PWM voltage stress from 6V to VCC+0.3V.
For cases where the 5V bias needs to be 5.0V, use this setup:
Tie the VIN pin of the LTC3774 to INTVCC and tie these two pins to the 5V bias with a 2.2 Ohm resistor.
Place a 4.7uF cap from the combined VIN and INTVCC pins to ground.



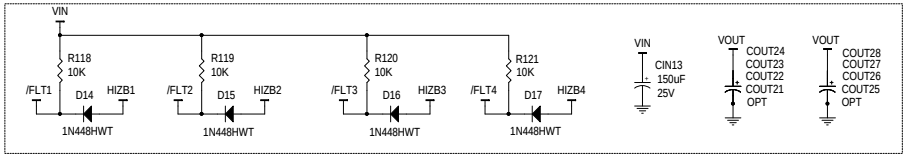
OPTIONAL NTC COMPENSATION NETWORK



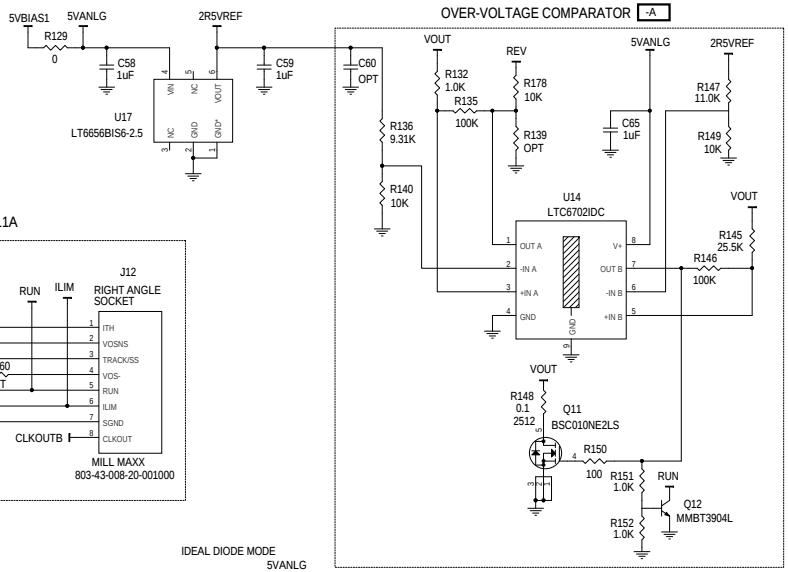
-A DRMOS BIAS SUPPLY FOR MOSFET FAILURE PROTECTION CIRCUIT



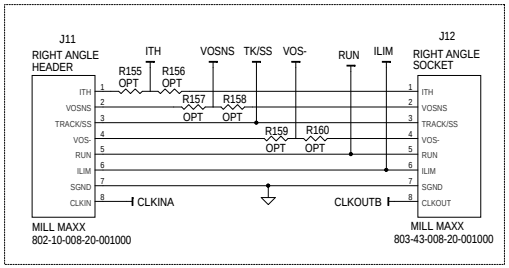
OPTIONAL COMPONENTS



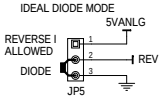
OVER-VOLTAGE COMPARATOR -A



CONNECT TO PARALLEL DC2111A



IDEAL DIODE MODE



Note 2:
Over-voltage comparator A permits the LTC3774 converter
to sink current during a VOUT over-voltage event by placing the ideal diodes in the "REVERSE I ALLOWED" mode when VOUT exceeds 1.3V.
To allow comparator A to work as intended, remove the jumper at JP5.
Comparator B is a back-up OVP comparator intended for cases where the VOUT sense lines are shorted together or
VOUT is shorted to an external source and the ideal diodes are in the "DIODE" mode.
When VOUT exceeds 1.5V, comparator B pulls down the RUN pin and turns on a MOSFET to discharge VOUT.
VOUT and the RUN pin are released once VOUT falls below 0.4V.

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