

A Closed-Loop, Wideband, 100A Active Load

Brute Force Marries Controlled Speed

Jim Williams

Introduction

Digital systems, particularly microprocessors, furnish transient loads in the 100A range that a voltage regulator must service. Ideally, regulator output is invariant during a load transient. In practice, some variation is encountered and becomes problematic if allowable operating voltage tolerances are exceeded. 100A load steps, characteristic of microprocessors, exacerbate this issue, necessitating testing the regulator and associated components under such transient loading conditions. To meet this need, a closed-loop, 500kHz bandwidth, linearly responding, 100A capacity active load is described below.

Study of this approach is prefixed by a brief review of conventional test load types and noting their shortcomings¹.

Basic Load Transient Generator

Figure 1 diagrams a conceptual load transient generator. The regulator under test drives DC and switched resistive loads, which may be variable. The switched current and output voltage are monitored, permitting comparison of the nominally stable output voltage versus load current under static and dynamic conditions. The switched current is either on or off; there is no controllable linear region.

Figure 2 develops the concept by including electronic load switch control. Operation is straightforward. The input

pulse switches the FET via a drive stage, generating a transient load current out of the regulator and its output capacitors. The size, composition and location of these capacitors has a pronounced effect on transient response and must be quite carefully considered. Although the electronic control facilitates high speed switching, the architecture cannot emulate loads between the minimum

Note 1: See Reference 1, from which the immediately following material partially derives, for details and descriptions of very wideband load transient generators, albeit at much lower currents.

LT, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

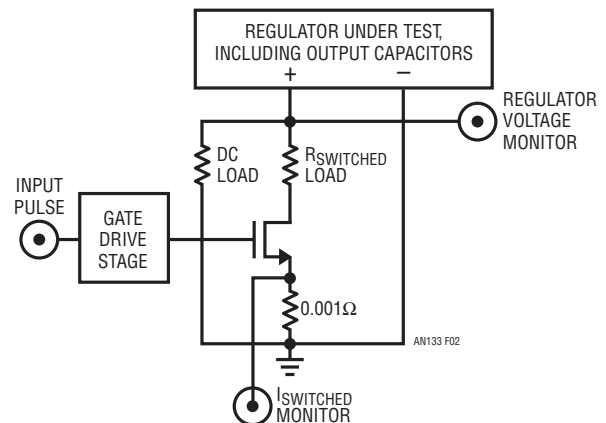


Figure 2. Conceptual FET Based Load Tester Permits Input Pulse Controlled Step Loading. As Before, Switched Current Is Either On or Off; There Is No Controllable Linear Region

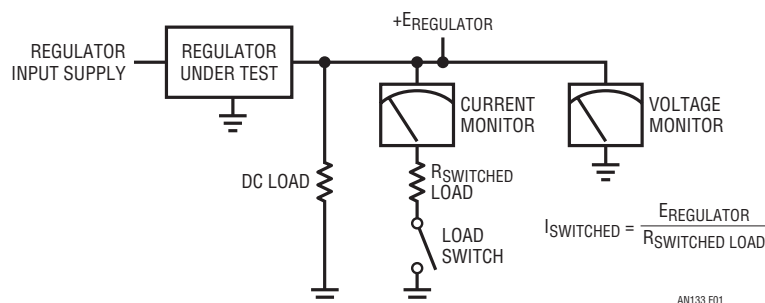


Figure 1. Conceptual Regulator Load Tester Includes Switched and DC Loads and Voltage/Current Monitors. Resistor Values Set DC and Switched Load Currents. Switched Current Is Either On or Off; There Is No Controllable Linear Region

an133f

Detailed Circuitry Discussion

Figure 5's detailed schematic of the 100A capacity load tester follows Figure 4's outline. A1, responding to DC and pulse inputs and current indicating feedback from A3, sets Q1's conductivity via the actively biased Q4-Q5 gate drive stage. A2 determines stage bias under all conditions by comparing Q5's averaged collector voltage to a reference and controlling Q3's conduction, closing a loop. C1, instructed by the average input value, shuts down FET gate drive via Q2 under harmful conditions². SW1, sensing heat sink temperature, contributes thermally activated Q1 shutdown. Q6 and the Zener prevent Q1 turn-on if the

-15V supply is not present by diverting Q4 bias. A1's 1k resistor precludes A1 damage due to 15V supply loss. Trims optimize dynamic response, determine loop DC baseline idle current, set dissipation limit and control gate drive stage bias. The DC trims are self-explanatory. The "loop compensation" and "FET response" AC trims at A1 are more subtle. They are adjusted for the best compromise between loop stability, edge rate and pulse purity. A1's loop compensation trim sets roll-off for maximum

Note 2: The protection scheme is patterned after techniques utilized in high power pulse generators. See Reference 2 and 3.

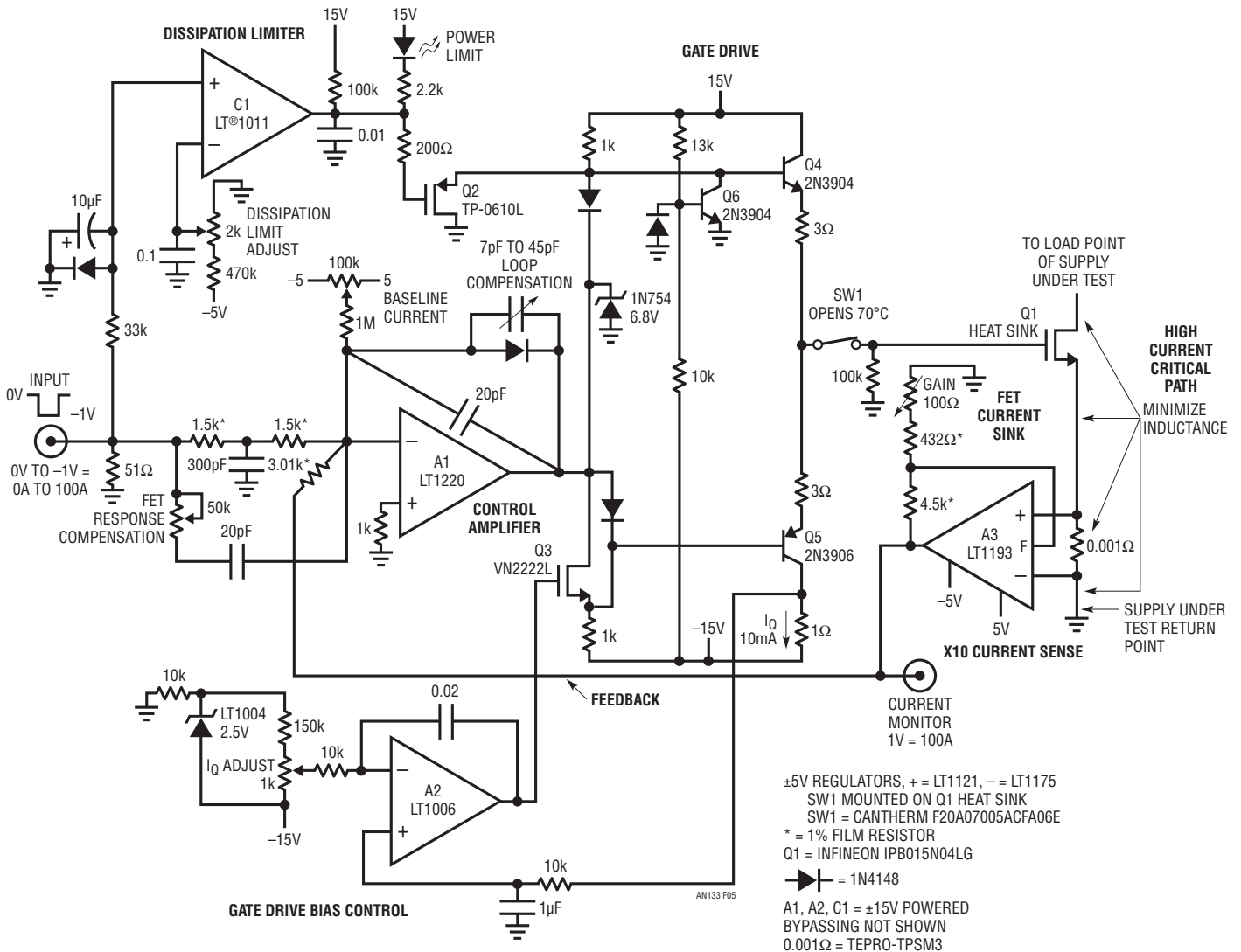


Figure 5. Detailed Circuitry Follows Figure 4's Concept. A1, Responding to DC and Pulsed Inputs, Sets Q1 Conductivity via Actively Biased Gate Drive Stage. A3, Sensing Q1 Current, Closes A1's Feedback Loop. C1, Instructed by Average Input Value, Shuts Down Q1 Gate Drive Under Harmful Conditions. Q6 Guards Against Lost -15V Supply. SW1 Adds Thermal Limiting. Trims Optimize Dynamic Response, Determine Loop Baseline Idle Current, Set Dissipation Limit and Control Gate Drive Stage Bias

an133f

Application Note 133

bandwidth while accommodating phase shift introduced by Q1's gate capacitance and, to a lesser extent, by A3. The "FET response" adjustment partially compensates Q1's inherent nonlinear gain characteristic, improving front and rear pulse corner fidelity³.

Circuit Testing

The circuit is initially tested using a fixture equipped with massive, low loss, wideband bypassing shown in Figure 6. Additionally, the importance of exceptionally low inductance layout in the high current path cannot be overstated. Every attempt must be made to minimize inductance in the 100A path; such current density at high speed demands low inductance if waveform purity is desirable. Figure 7 shows

results with the circuit properly trimmed and a minimized inductance high current path. The 100A amplitude, high speed waveform is exceptionally pure with just discernible top-front and bottom-rear corner infidelities⁴. AC trim effects on waveform presentation are studied by deliberate mis-adjustment. Figure 8's overdamped response is typical of excess A1 feedback capacitance. The current pulse is well controlled but edge rate is slow. Figure 9's inadequate A1 feedback capacitance decreases transition time but

Note 3: The trimming procedure is not described here in order to maintain text flow and focus. For detailed trimming information see Appendix B, "Trimming Procedure".

Note 4: See Appendices A, "Verifying Current Measurement" and C, "Instrumentation Considerations" for guidance on obtaining Figure 7's performance level.

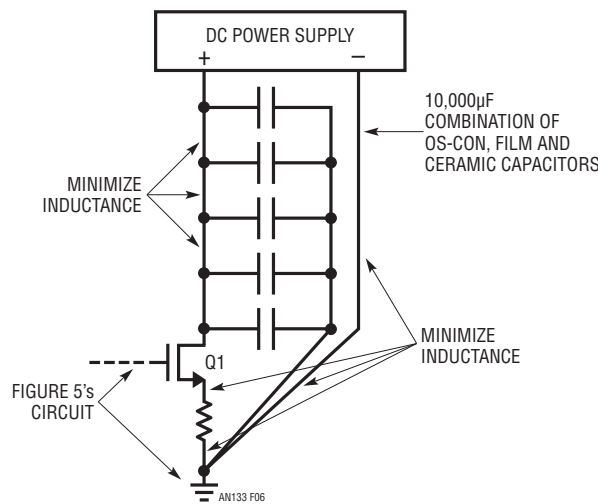


Figure 6. Fixturing Tests Figure 5's Dynamic Response. Massive, Broadband Bypassing Combined with Low Inductance Layout Provides Low Loss, High Current Power to Q1

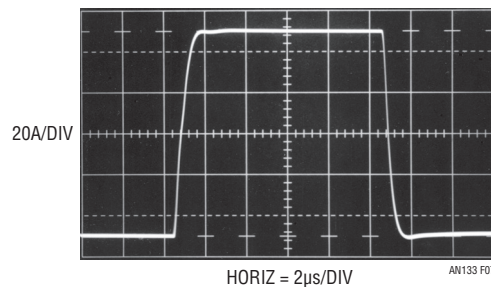


Figure 7. Optimized Dynamic Response Trims Yield Exceptionally Pure, 100A Q1 Current Pulse. Residual Top-Front and Bottom-Rear Corner Infidelities Are Just Discernable

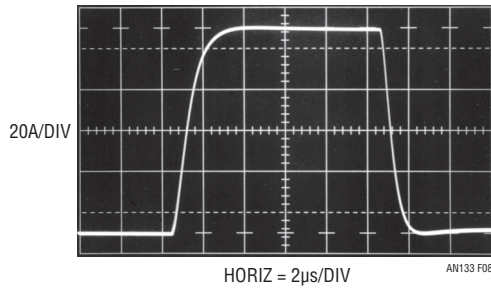


Figure 8. Overdamped Response Characteristic of Excessive A1 Feedback Capacitor Value

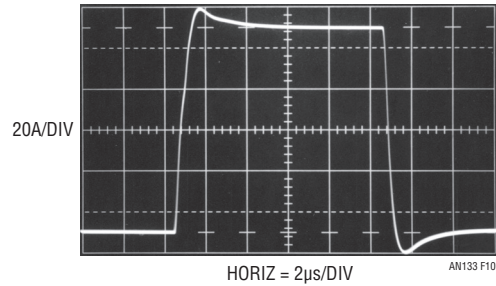


Figure 10. Corner Peaking Due to Overstated FET Response Compensation

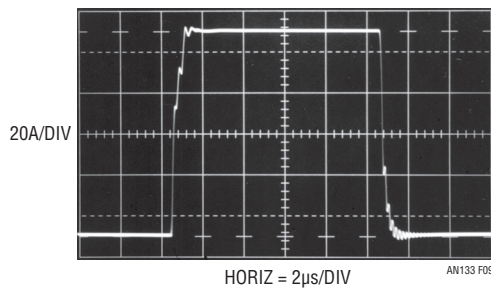


Figure 9. Inadequate A1 Feedback Capacitor Decreases Transition Time But Promotes Instability. Further Capacitor Reduction Causes Oscillation

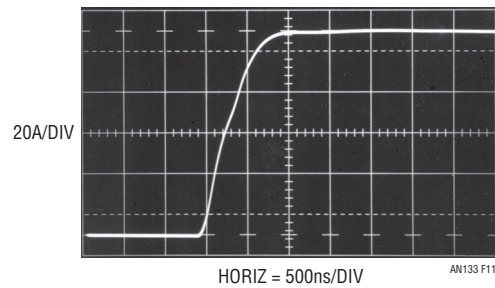


Figure 11. Optimized Dynamic Trims Allow 650 Nanosecond Rise Time, Corresponding to $\approx 540\text{kHz}$ Bandwidth

promotes instability. Further capacitance reduction will cause loop oscillation because loop phase shift becomes a significant feedback lag⁵. Figure 10's corner peaking is due to overstated FET response compensation.

If the AC trims are restored to nominal values, Figure 11's leading edge indicates 650 nanosecond rise time, equivalent to $\approx 540\text{kHz}$ bandwidth. The trailing edge (Figure 12), taken under the same conditions as the previous figure, is somewhat faster at 500 nanosecond fall time.

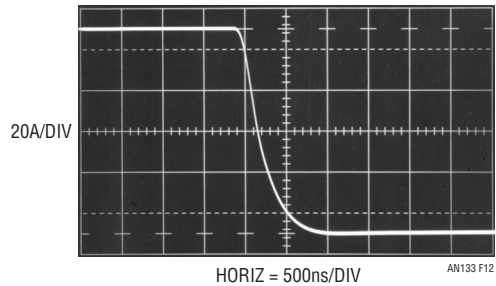


Figure 12. Same Conditions as Figure 11 Show 500 Nanosecond Fall Time

Note 5: Sorry, no photo available. Uncontrolled 100 Ampere amplitude loop oscillation is too thrilling for documenting.

Application Note 133

Layout Effects

None of the previous responses, even the mis-compensated examples, can be remotely approached if parasitic inductance is present in the high current path. Figure 13 deliberately places only 20nH parasitic inductance in Q1's drain path. Figure 14a displays enormous waveshape degradation deriving from the inductance and the loop's subsequent response. A monstrous error dominates

the leading edge before recovery occurs at the pulse middle-top. Additional aberration is evident in the falling edge turn-off. It is especially noteworthy that the photo's horizontal scale is 5× slower than Figure 7's optimized response, repeated here for emphasis as Figure 14b. The lesson is clear. High speed 100A excursions do not tolerate inductance.

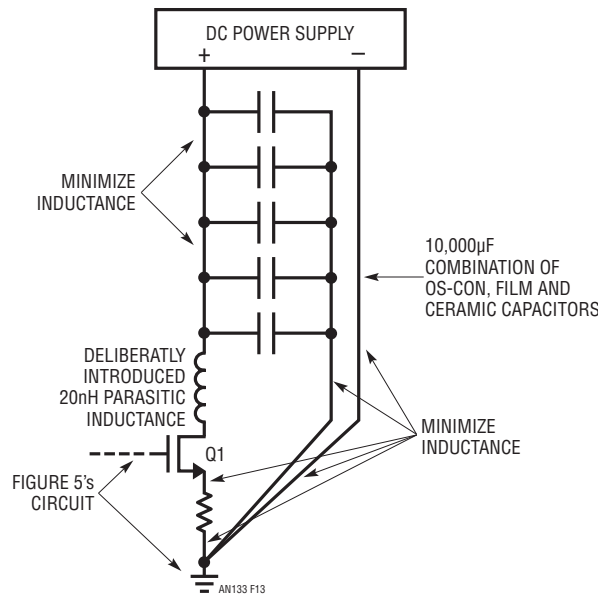


Figure 13. Deliberately Introduced Parasitic 20nH Inductance Tests Figure 5's Layout Sensitivity

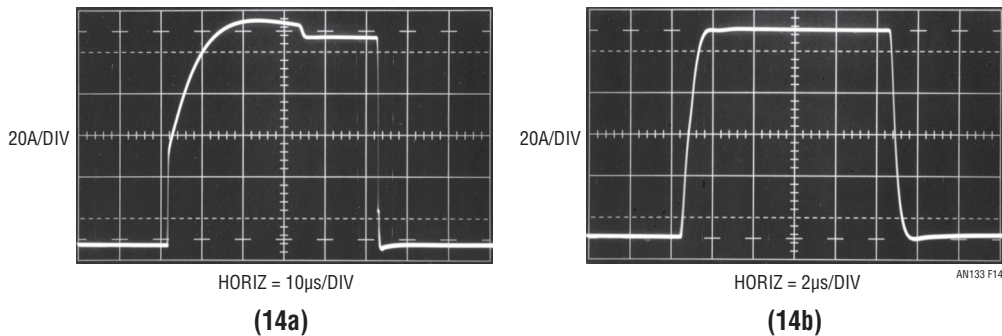


Figure 14. 1.5" of 0.075" (20nH) Flat Copper Braided Wire Completely Distorts (Figure 14a) Text Figure 7's (Shown Here as Figure 14b) Response. Note 5× Horizontal Scale Change

Regulator Testing

Regulator testing is possible after the above compensation and layout issues have been addressed. Figure 15 describes a test arrangement for an LTC[®]3829 based, 6-phase, 120A buck regulator⁶. Trace A, Figure 16 shows the 100A load pulse. Trace B's regulator response is well controlled on both edges.

The active loads true linear response and high bandwidth permit wide ranging load waveform characteristics. While the step load pulse shown above is the commonly desired

Note 6: This regulator is conveniently incarnated as LTC demonstration board 1675A.

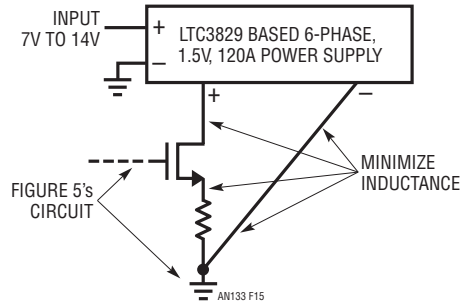


Figure 15. Test Arrangement for LTC3829 Based 6-Phase, 120A Buck Regulator Emphasizes Low Impedance Connections to Figure 5's Circuit

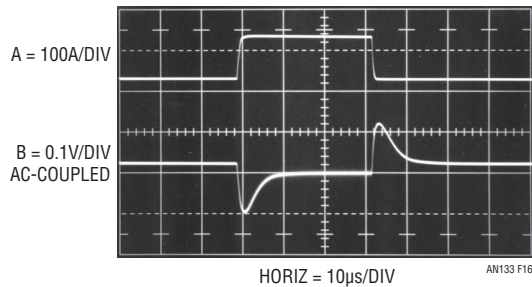


Figure 16. Figure 5's Circuit Subjects Figure 15's Regulator to 100A Pulsed Load (Trace A). Response (Trace B) Is Well Controlled on Both Edges

Application Note 133

test, essentially any load profile is easily generated. Figure 17's burst of 100A, 100kHz sinewaves is an example. Response is crisp, with no untoward dynamics despite

the high speed and current involved. In Figure 18, an 80 microsecond burst of 100A peak-peak noise forms the load. Figure 19 summarizes active load characteristics.

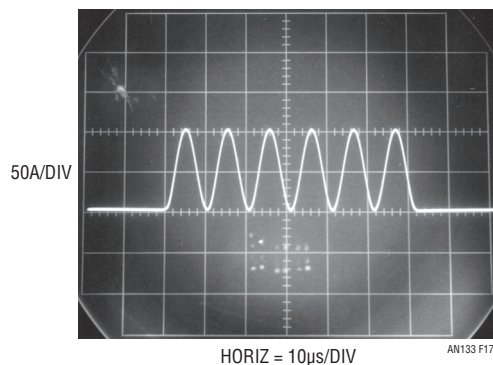


Figure 17. Figure 5 Supplies 100kHz, 100A Sinewave Load Transient Profile. Circuit's Wide Bandwidth and Linear Operation Permit Wide Ranging Load Waveform Characteristics

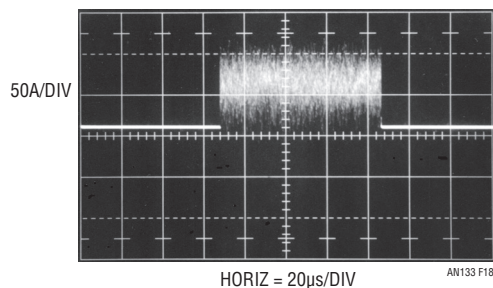
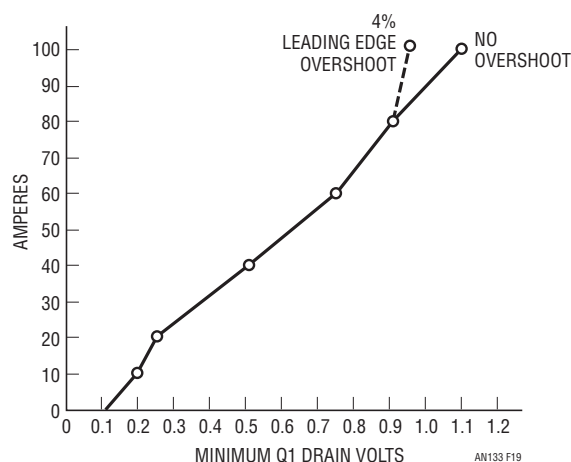


Figure 18. Active Load Circuit Sinks 100A Peak-Peak in Response to Gated Random Noise Input

Active Load Characteristics

CURRENT ACCURACY (REFERRED TO INPUT)	— 1% FS
TEMPERATURE DRIFT	— 100ppm/°C OF READING + 20mA/°C
CURRENT REGULATION vs SUPPLY	— >60dB PSRR
BANDWIDTH	— 540kHz AT 100A ($t_{RISE} = 650ns$) 435kHz AT 10A ($t_{RISE} = 800ns$)
COMPLIANCE VOLTAGES FOR FULL OUTPUT CURRENT	— 0.95V MIN (SEE PLOT) MAX SET BY 70°C Q1 THERMAL DISSIPATION LIMITER



Minimum Compliance Voltage vs Load Current

Figure 19. Active Load Tabular Characteristics. Current Accuracy/Regulation Errors Are Small, Bandwidth Mildly Retards at Low Current. Compliance Voltage Is Below 1V at 100A with 4% Leading Edge Overshoot, 1.1V with No Overshoot

an133f

REFERENCES

1. Williams, Jim, "Load Transient Response Testing For Voltage Regulators", Linear Technology Corporation, Application Note 104, October 2006.
2. Hewlett-Packard Company, "HP-214A Pulse Generator Operating and Service Manual", "Overload Adjust", Figure 5-13. See also, "Overload Relay Adjust", pg. 5-9. Hewlett-Packard Company, 1964.
3. Hewlett-Packard Company, "HP-214B Pulse Generator Operating and Service Manual", "Overload Detection/Overload Switch ...", pg. 8-29. Hewlett-Packard Company, March, 1980.

APPENDIX A

Verifying Current Measurement

Theoretically, Figure 5's Q1 source and drain current are equal. Practically, questions center on potential effects of residual inductances and the huge (28000pF!) gate capacitance of the 1.5mΩ FET specified. If these or other terms impact drain-source current equivalence at speed A3's indicated instantaneous current could be erroneous. Verification is necessary and Figure A1 diagrams a method. An added "top-side" 1mΩ shunt and its attendant X10 differential amplifier duplicate the circuit's resident "bottom-side" current sensing section. Figure A2's results happily eliminate concern over dynamic Q1 current differences. The two 100A pulse outputs are identical in amplitude and shape, promoting confidence in circuit operation.

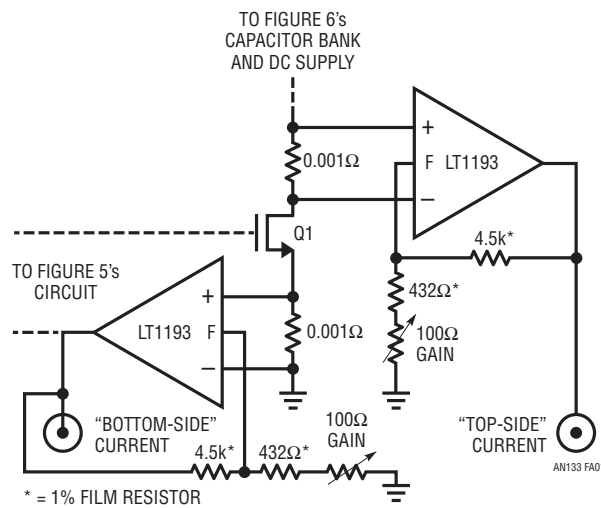


Figure A1. Arrangement For Observing Q1's "Top" and "Bottom" Dynamic Currents

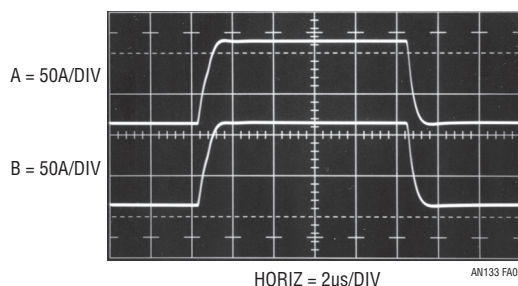


Figure A2. Q1 "Top" (Trace A) and "Bottom" (Trace B) Currents Show Identical Characteristics Despite High Speed Operation

APPENDIX B

Trimming Procedure

Trimming Figure 5's circuit is a 7-step procedure which should be performed in the numerical order listed below. Out-of-sequence adjustments are permissible assuming the dissipation limiter circuitry is working and adjusted.

1. Set all adjustments to mid-range except A1's feedback capacitor, which should be at full capacity.
2. Apply no input, bias Q1's drain from a 1V DC supply, turn on power and trim "Base Line Current" for 0.5A through Q1. Monitor this current with an ammeter in Q1's drain line.
3. Turn power off. Lift Q2's source lead and let it float. *This disables the dissipation limit circuitry, leaving Q1 vulnerable to damage from inappropriate inputs. Follow the remainder of this step in strict accordance with the instructions given.* Turn power on, bias Q1's drain from a 1V supply and apply a -0.1000V DC input while monitoring Q1's drain current with an ammeter. Trim the "Gain" adjustment for a 10.50A meter reading¹. Make this adjustment fairly quickly as Q1 is dissipating 10 Watts. Turn power off and reconnect Q2's source lead².
4. Turn power on with no input applied and Q1's drain unbiased. Trim the " I_Q " adjustment for +10mV at A2's positive input measured with respect to the -15V rail. Turn off power.
5. Bias and bypass Q1's drain in accordance with text Figure 6. Set the drain DC power supply for 1.5V output and turn on power. Apply a 1kHz, -1V amplitude, $5\mu\text{s}$ wide pulse. Slowly increase pulse width until C1 trips, shutting down circuit output and illuminating the "Power Limit" LED. Tripping should occur at about $12\mu\text{s}$ to $15\mu\text{s}$ pulse width. If it does not, adjust the "Dissipation Limit" potentiometer to bring the trip point within these limits. This sets allowable full-amplitude (100A) duty cycle at about 1.5% .
6. Under the same operating conditions as Step 5, set input pulse width at $10\mu\text{s}$ and adjust A1's capacitive trim for the fastest positive going edge obtainable at A3's output without introducing pulse distortion. Pulse clarity should approach text Figure 7 with somewhat degraded top-front and bottom-rear corner rounding.
7. Adjust "FET Response Compensation" to correct the corner rounding noted in Step 6. Some interaction may occur with Step 6's adjustment. Repeat Step 6 and 7 until A3's output waveform looks like text Figure 7.

Note 1: The tight trim targets are mandated by trimming gain at only 10% of scale. This is certainly undesirable but less painful than trimming at 100% of scale which would force astronomical (and brief) dissipation in Q1 and the milliohm shunt.

Note 2: It is worth mention that the primary uncertainty necessitating gain trimming is the sense lines mechanical placement at the milliohm shunt.

APPENDIX C

Instrumentation Considerations

The pulse edge rates discussed in the text are not particularly fast, but high fidelity response requires some diligence. In particular, the input pulse must be cleanly defined and devoid of parasitics which would unfairly make circuit output pulse shape look bad. The pulse generators pre-shoot, rise time and pulse-transition aberrations are well out of band and filtered by A1's 2.1MHz ($t_{RISE} = 167ns$) input RC network. These terms are not a concern; almost all general purpose pulse generators should perform well. A potential offender is excessive tailing after transitions. Meaningful dynamic testing requires a rectangular pulse shape, flat on top and bottom within 1% to 2%. The circuit's input band shaping filter removes the aforementioned high speed transition related errors but will not eliminate lengthy tailing in the pulse flats. The pulse generator should be checked for this with a well compensated probe at the circuit input. The oscilloscope should register the desired flat top/bottom waveform characteristics. In making this measurement, if high speed transition related events are bothersome, the probe can be moved to the band limiting 300pF capacitor. This is defensible practice because the waveform at this point determines A1's input signal bandwidth.

Some pulse generator output stages produce low level DC offset when their output is nominally at its zero volt state. The active load circuit will process such DC potentials as legitimate signal, resulting in DC load baseline current shift.

The active loads input scale factor of $1V = 100A$ means that a 10mV "zero" state error produces 1A of DC baseline current shift. A simple way to check a pulse generator for this error is to place it in external trigger mode and read its output with a DVM. If offset is present it can be accounted for, nullified with the circuit's "baseline current" trim or another pulse generator can be selected.

Parasitic effects due to probe grounding and instrument interconnection should be kept in mind. At pulsed 100A levels parasitic current is easily induced into "grounds" and interconnections, distorting displayed waveforms. Probes should be coaxially grounded, particularly at A3's output current monitor and preferably anywhere else. Additionally, it is convenient and common practice to externally trigger the oscilloscope from the pulse generator's trigger output. There is nothing wrong with this, in fact it is recommended to insure a stable trigger as probes are moved between points. This practice does, however, potentially introduce ground loops due to multiple paths between the pulse generator, the circuit and the oscilloscope. This can falsely cause apparent distortion in displayed waveforms. This effect is avoidable by using a "trigger isolator" at the oscilloscope external trigger input. This simple coaxial component typically consists of isolated ground and signal paths, often coupled to a pulse transformer to provide a galvanically isolated trigger event. Commercial examples include the Deerfield Labs 185 and the Hewlett-Packard 11356A. Alternately, a trigger isolator is easily constructed in a small BNC equipped enclosure as shown in Figure C1.

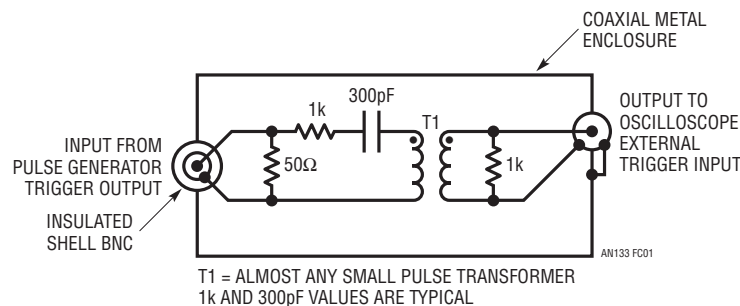
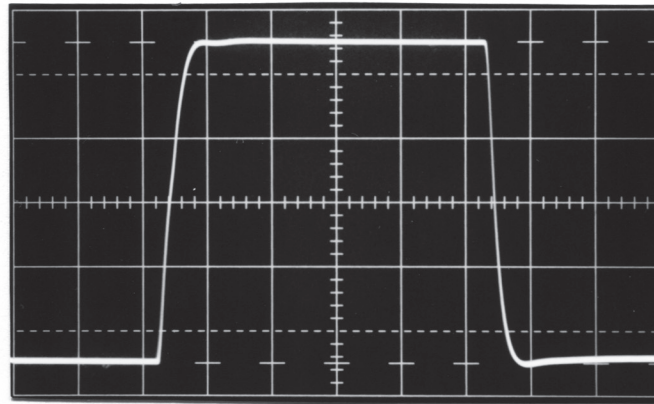


Figure C1. Trigger Isolator Floats Input BNC Ground Using Insulated Shell BNC Connector. Capacitively Coupled Pulse Transformer Avoids Loading Input, Maintains Isolation, Delivers Trigger to Output. T1 Secondary Resistor Terminates Ringing

Power Uncorrupted

20 Amperes/Div.



2 μ s/Div.

J. Williams, with apologies to
LORD ACTON
(1834 - 1902)