Modeling and Loop Compensation Design of Switching Mode Power Supplies

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INTRODUCTION

Today's electronic systems are becoming more and more complex, with an increasing number of power rails and supplies. To achieve optimum power solution density, reliability and cost, often system designers need to design their own power solutions, instead of just using commercial power supply bricks. Designing and optimizing high performance switching mode power supplies is becoming a more frequent and challenging task.

Power supply loop compensation design is usually viewed as a difficult task, especially for inexperienced supply designers. Practical compensation design typically involves numerous iterations on the value adjustment of the compensation components. This is not only time consuming, but is also inaccurate in a complicated system whose supply bandwidth and stability margin can be affected by several factors. This application note explains the basic concepts and methods of small signal modeling of switching mode power supplies and their loop compensation design. The buck step-down converter is used as the typical example, but the concepts can be applied to other topologies. A user-friendly LTpowerCAD™ design tool is also introduced to ease the design and optimization.

IDENTIFYING THE PROBLEM

A well-designed switching mode power supply (SMPS) must be quiet, both electrically and acoustically. An under-compensated system may result in unstable operations. Typical symptoms of an unstable power supply include: audible noise from the magnetic components or ceramic capacitors, jittering in the switching waveforms, oscillation of output voltage, overheating of power FETs and so on.

However, there are many reasons that can cause undesirable oscillation other than loop stability. Unfortunately, they all look the same on the oscilloscope to the inexperienced supply designer. Even for experienced engineers, sometimes identifying the reason that causes the instability can be difficult. Figure 1 shows typical output and switching node waveforms of an unstable buck supply. Adjusting the loop compensation may or may not fix the unstable supply because sometimes the oscillation is caused by other factors such as PCB noise. If you do not have a list of possibilities in your mind, uncovering the underlying cause of noisy operation can be very time-consuming and frustrating.

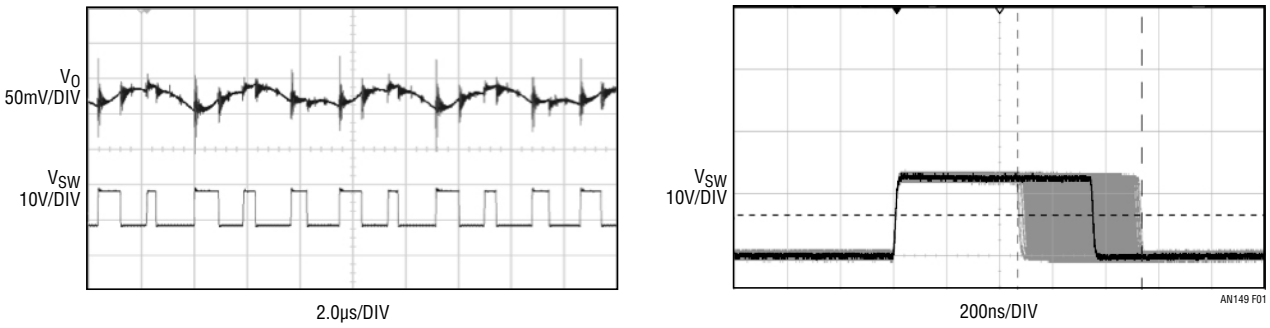


Figure 1. Typical Output Voltage and Switching Node Waveforms of an "Unstable" Buck Converter

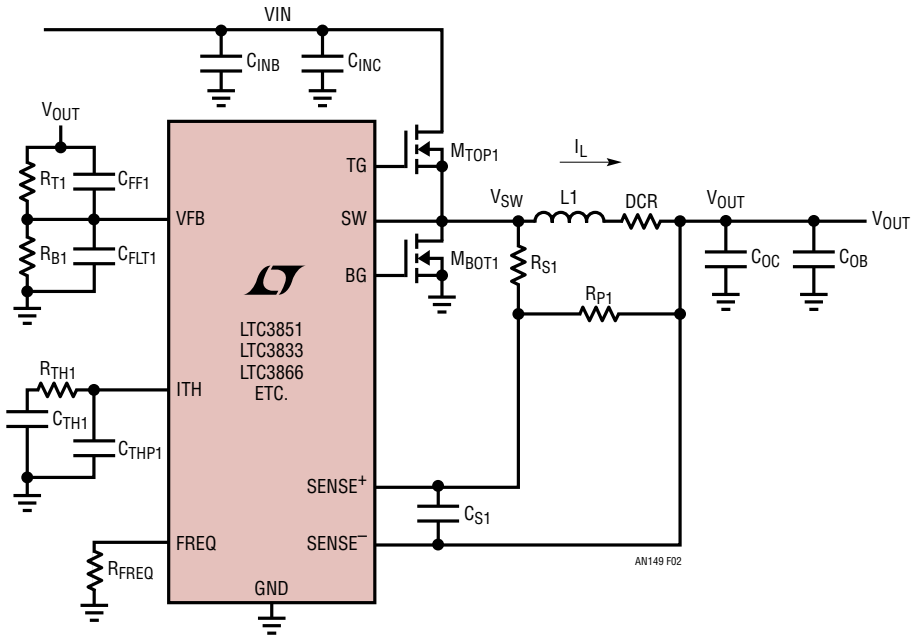
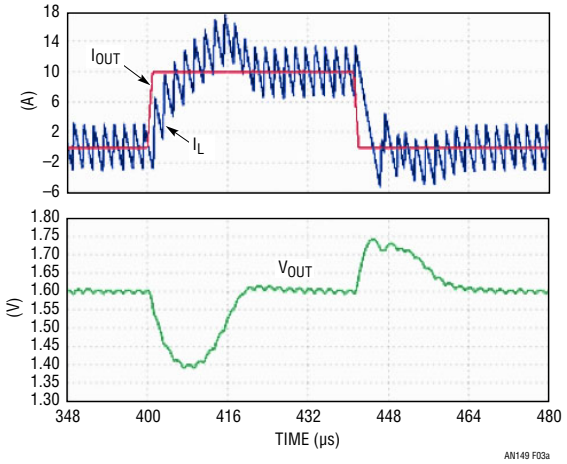


Figure 2. A Typical Buck Step-Down Converter

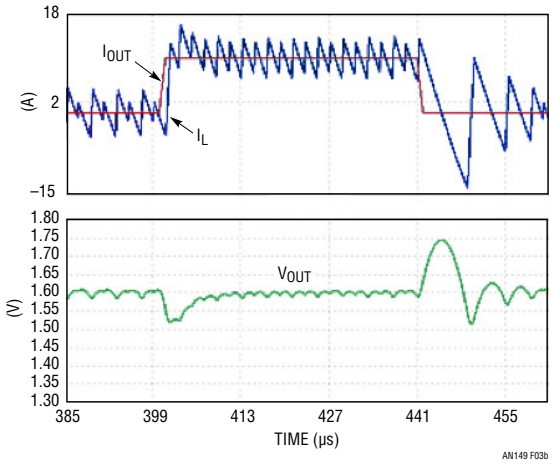
(LTC3851, LTC3833, LTC3866, etc.)

For switching mode power converters, such as an LTC®3851 or LTC3833 current-mode buck supply shown in Figure 2, a fast way to determine whether the unstable operation is caused by the loop compensation is to place a large, 0.1µF, capacitor on the feedback error amplifier output pin (ITH) to IC ground. (Or this capacitor can be placed between the amplifier output pin and feedback pin for a voltage mode supply.) This 0.1µF capacitor is usually considered large enough to bring down the loop bandwidth to low frequency, therefore ensuring voltage loop stability. If the supply becomes stable with this capacitor, the problem can likely be solved with loop compensation.

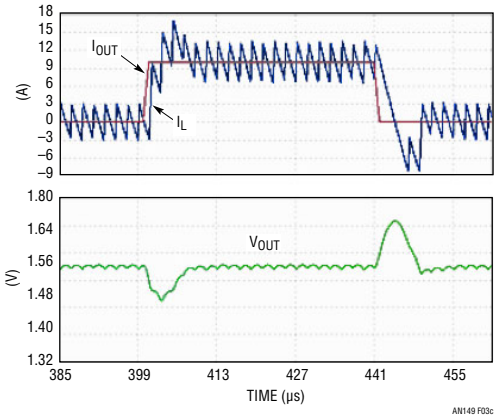
An over-compensated system is usually stable, however, with low bandwidth and slow transient response. Such design requires excessive output capacitance to meet the transient regulation requirement, increasing the overall supply cost and size. Figure 3 shows typical output voltage and inductor current waveforms of a buck converter during a load step up/down transient. Figure 3a is for a stable but low bandwidth (BW) over-compensated system, where there is large amount of V_{OUT} undershoot/overshoot during transient. Figure 3b is for a high bandwidth under-compensated system, which has much less V_{OUT} undershoot/overshoot but the waveforms are not stable in steady state. Figure 3c shows the load transient of a well-designed supply with a fast and stable loop.



a) Lower Bandwidth and Stable



b) Higher Bandwidth but Unstable



c) Optimum Design with Fast and Stable Loop

Figure 3. Typical Load Transient Responses of a) An Over-Compensated System; b) An Under-Compensated System; c) Optimum Design with a Fast and Stable Loop

SMALL SIGNAL MODELING OF PWM CONVERTER POWER STAGE

A switching mode power supply (SMPS), such as the buck step-down converter in Figure 4, usually has two operating modes, depending on the on/off state of its main control switch. Therefore, the supply is a time-variant, nonlinear system. To analyze and design the compensation with conventional linear control methods, an averaged, small signal linear model is developed by applying linearization techniques on the SMPS circuit around its steady state operating point.

Modeling Step 1: Changing to a Time-Invariant System by Averaging over T_S

All the SMPS power topologies, including buck, boost or buck/boost converters, have a typical 3-terminal PWM switching cell, which includes an active control switch Q and passive switch (diode) D. To improve efficiency, the diode D can be replaced by a synchronous FET, which is still a passive switch. The active terminal "a" is the active switch terminal. The passive terminal "p" is the passive switch terminal. In a converter, the terminals a and p are always connected to a voltage source, such as V_{IN} and ground in the buck converter. The common terminal "c" is connected to a current source, which is the inductor in the buck converter.

To change the time-variant SMPS into a time-invariant system, the 3-terminal PWM cell average modeling method can be applied by changing the active switch Q to an averaged current source and the passive switch (diode) D to an averaged voltage source. The averaged switch Q current equals $d \bullet i_L$ and the averaged switch D voltage equals $d \bullet v_{ap}$, as shown in Figure 5. The averaging is applied over a switching period T_S. Since the current and voltage sources are the products of two variables, the system is still a nonlinear system.

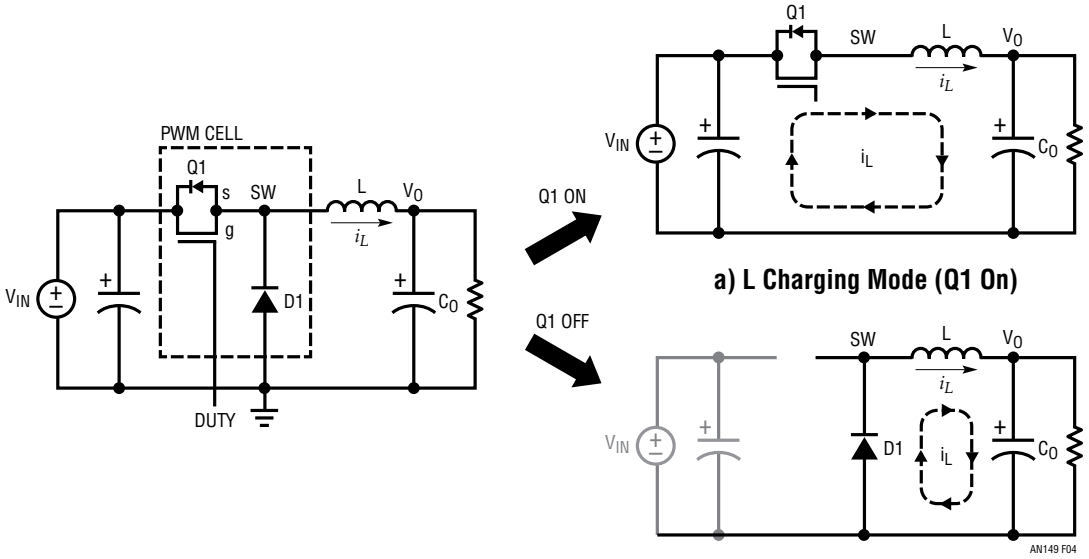


Figure 4. A Buck Step-Down DC/DC Converter and Its Two Operating Modes within One Switching Period T_S

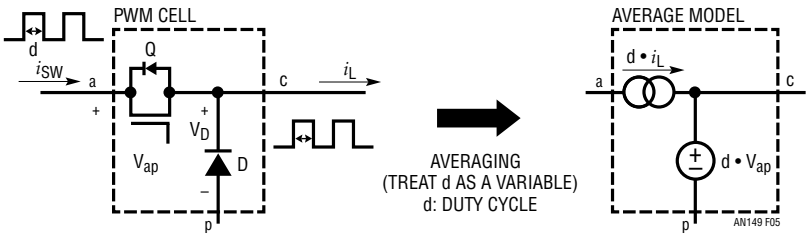


Figure 5. Modeling Step 1: Changing 3-Terminal PWM Switching Cell to Averaged Current and Voltage Sources

Modeling Step 2: Linear Small Signal AC Modeling

The next step is to expand the product of variables to get the linear AC small signal model. For example, a variable $x = X + \hat{x}$, where X is the DC steady state operating point and $\hat{x}$ is the AC small signal variation around X. Therefore, the product of two variables $x \bullet y$ can be rewritten as:

$$x \bullet y = (\hat{x} + X) \bullet (\hat{y} + Y) = \underbrace{\hat{x} \bullet Y + X \bullet \hat{y}}_{\text{SMALL SIGNAL AC}} + \underbrace{X \bullet Y}_{\text{DC(OP)}} + \underbrace{\cancel{\hat{x} \bullet \hat{y}}}_{\text{IGNORE}}$$

Figure 6. Expand the Product of Two Variables for Linear Small Signal AC Part and DC Operating Point

Figure 6 shows that the linear small signal AC part can be separated from the DC operating point (OP) part. And the product of two AC small signal variations ($\hat{x} \bullet \hat{y}$) can be ignored, since it is an even smaller value variable. Following this concept, the averaged PWM switching cell can be rewritten as shown in Figure 7.

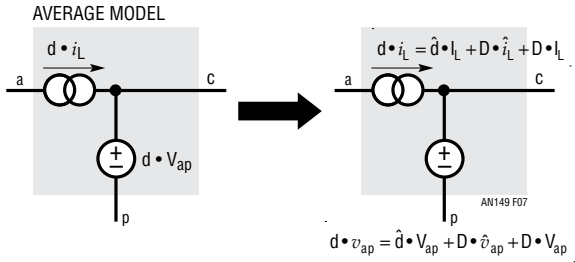


Figure 7. Modeling Step 2: AC Small Signal Modeling by Expanding the Products of Variables

By applying this two-step modeling technique to a buck converter, as shown in Figure 8, the buck converter power stage can be modeled as simple voltage source, $\hat{d} \bullet V_{IN}$, followed by an L/C 2nd-order filter network.

Based on the linear circuit in Figure 8, since the control signal is the duty cycle d and the output signal is v_{OUT}, the buck converter can be described by the duty-to-output transfer function $G_{dv}(s)$ in the frequency domain:

$$G_{dv}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{V_{IN} \bullet \left(1 + \frac{s}{s_{z\_ESR}}\right)}{1 + \frac{s}{\omega_o \bullet Q} + \frac{s^2}{\omega_o^2}} \quad (1)$$

where,

$$s_{z\_ESR} = 2\pi f_{z\_ESR} = \frac{1}{r_C \bullet C} \quad (2)$$

$$\omega_o = 2\pi f_{wo} = \frac{1}{\sqrt{L \bullet C}} \bullet \sqrt{\frac{1 + \frac{r_L}{R}}{1 + \frac{r_C}{R}}} \approx \frac{1}{\sqrt{L \bullet C}} \quad (3)$$

$$Q = \frac{1}{\omega_o} \bullet \frac{1}{\frac{L}{r_L + R} + C \bullet \left(r_c + \frac{r_L \bullet R}{r_L + R}\right)} \quad (4)$$

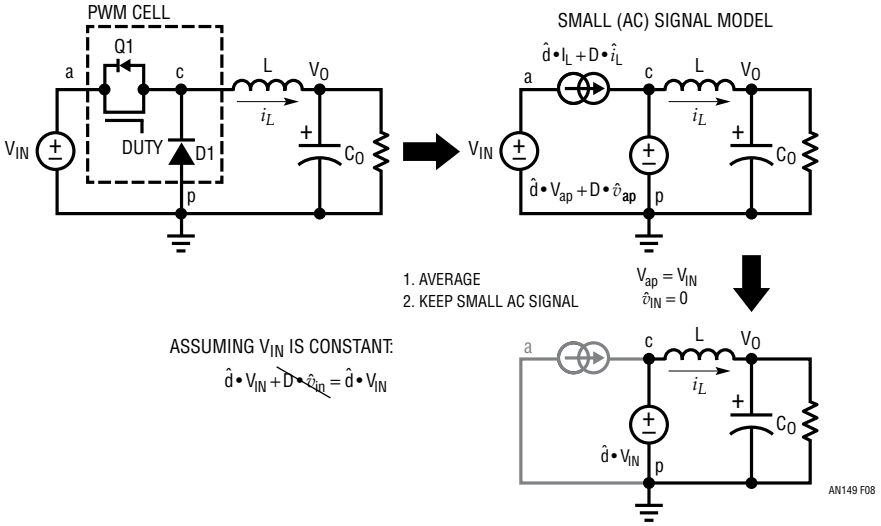


Figure 8. Changing a Buck Converter into an Averaged, AC Small Signal Linear Circuit

Function $G_{dv}(s)$ shows that the buck converter power-stage is a 2nd-order system with two poles and one zero in the frequency domain. The zero s_{Z_ESR} is generated by the output capacitor C and its ESR r_C. The resonant double poles ϖ_0 are generated by the output filter inductor L and capacitor C.

Since the poles and zero frequencies are functions of the output capacitor and its ESR, the bode plots of function $G_{dv}(s)$ varies with different choices of supply output capacitor, as shown in Figure 9. The small signal behavior of the buck converter power stage highly depends on the choice of output capacitors. If the supply has small output capacitance or very low-ESR output capacitors, the ESR zero frequency can be much higher than the resonant pole frequency. The power stage phase delay can be close to –180 degrees. As a result, it can be difficult to compensate the loop when the negative voltage feedback loop is closed.

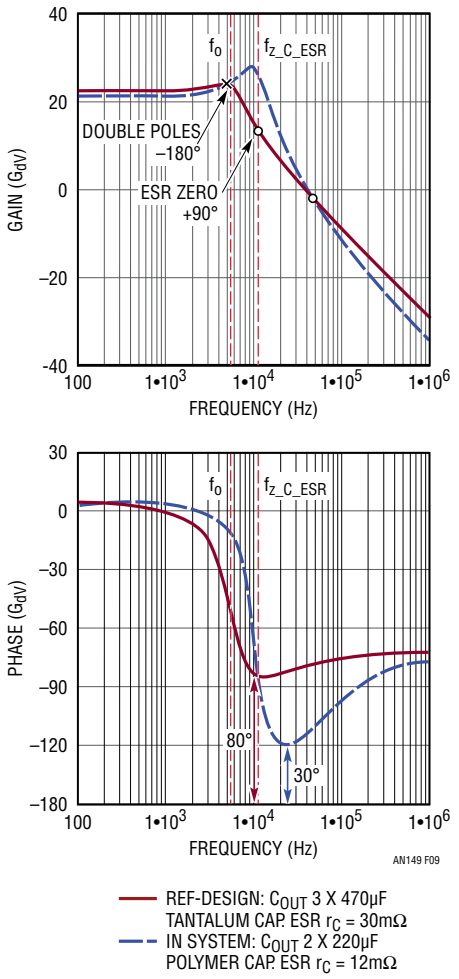


Figure 9. C_{OUT} Capacitor Variation Causes Significant Power Stage $G_{dv}(s)$ Phase Variation.

Small Signal Model of the Boost Step-Up Converter

Using the same 3-terminal PWM switching cell average small signal modeling method, the boost step-up converter can be modeled too. Figure 10 shows how to model and convert the boost converter to its linear AC small signal model circuit.

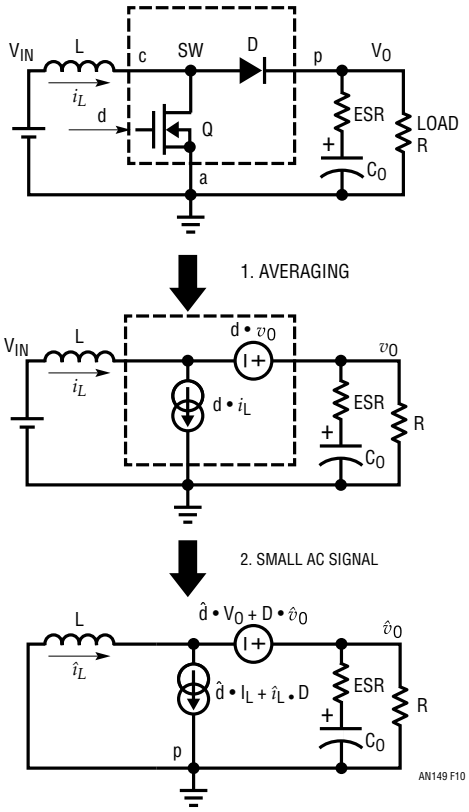


Figure 10. AC Small Signal Modeling Circuit of a Boost Step-Up Converter

The boost power stage transfer function $G_{dv}(s)$ can be derived in Equation (5). It is also a 2nd-order system with L/C resonance. Different from the buck converter, the boost converter has a right-half-plane zero (RHPZ) in addition to the C_{OUT} ESR zero. The RHPZ causes increased gain but reduced (negative) phase. Equation 6 also shows that the RHPZ varies with duty cycle and load resistance. Since the duty-cycle is a function of V_{IN}, the boost power stage transfer function $G_{dv}(s)$ varies with V_{IN} and load current. At low V_{IN} and heavy load I_{OUT_MAX}, the RHPZ is at its lowest frequency and causes significant phase lag. This makes it difficult to design a high-bandwidth boost converter. As a general design rule, to ensure loop stability, people design the boost converter bandwidth at less

than 1/10 of its lowest RHPZ frequency. Several other topologies, such as the positive-to-negative buck/boost, flyback (isolated buck/boost), SEPIC and CUK converters, all have an undesirable RHPZ and cannot be designed for high bandwidth, fast transient solutions.

$$G_{dv}(s) = \frac{\hat{v}_o}{\hat{d}} \quad (5)$$

$$= \frac{\frac{V_{IN}}{(1-D)^2}\left(1 - s \bullet \frac{L}{R \bullet (1-D)^2}\right) \bullet (1 + s \bullet r_c \bullet C)}{1 + s \bullet \frac{L}{R(1-D)^2} + s^2 \bullet \frac{LC}{(1-D)^2}}$$

$$f_{RHPZ} = \frac{(1-D)^2 \bullet R_{LOAD}}{2\pi \bullet L} \quad (6)$$

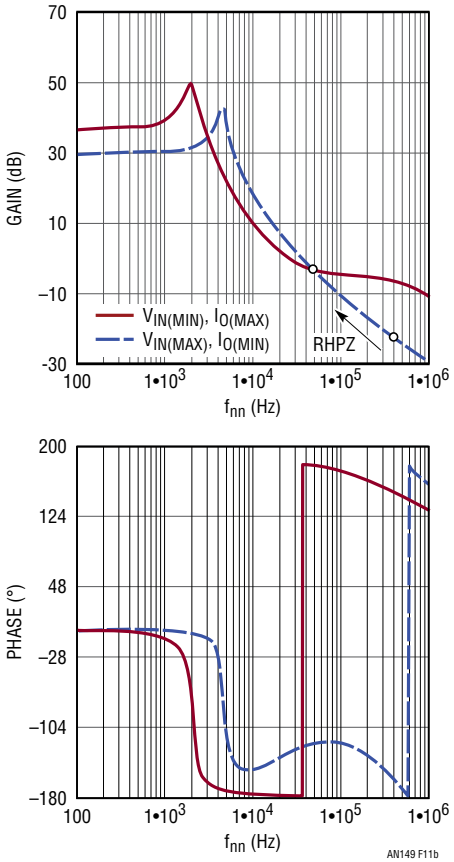


Figure 11. Boost Converter Power Stage Small Signal Duty-To-V_O Transfer Function Varies with V_{IN} and Load

CLOSE THE FEEDBACK LOOP WITH VOLTAGE MODE CONTROL

The output voltage can be regulated by a closed feedback loop system. For example in Figure 12, when the output voltage V_{OUT} increases, the feedback voltage V_{FB} increases and the output of the negative feedback error amplifier decreases, so the duty cycle d decreases. As a result, V_{OUT} is pulled back to make $V_{FB} = V_{REF}$. The compensation network of the error op amp can be a Type I, Type II or Type III feedback amplifier network. There is only one control loop to regulate the V_{OUT}. This control scheme is referred to as voltage mode control. Linear Technology's LTC3861 and LTC3882 are typical voltage mode buck controllers.

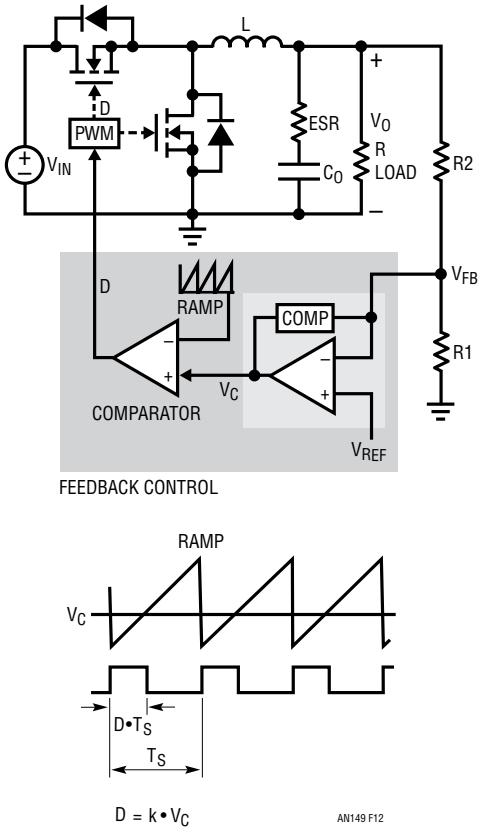


Figure 12. Voltage Mode Buck Converter Diagram with Closed Voltage Feedback Loop

To optimize a voltage mode PWM converter, as shown in Figure 13, a complicated Type III compensation network is usually needed to design a fast loop with sufficient phase margin. As shown in Equation 7 and Figure 14, this compensation network has 3 poles and 2 zeros in the frequency domain: the low frequency integration pole (1/s) provides high DC gain to minimize DC regulation error, the double-zeros are placed around the system resonant frequency f_0 to compensate the –180° phase delay caused by power stage L and C, the 1st high frequency pole is placed to cancel C_{OUT} ESR zero at f_{ESR}, and the 2nd high frequency pole is placed after the desired bandwidth f_C to attenuate switching noise in the feedback loop. The Type III compensation is quite complicated, since it requires six R/C values. It is a time consuming task to find the optimum combination of these values.

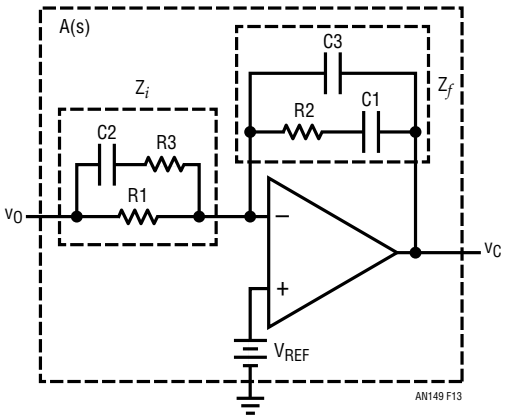


Figure 13. A Type III Feedback Compensation Network for a Voltage Mode Converter

$$\frac{\hat{V}_C}{\hat{V}_O} = -\frac{\omega_1\left(1+\frac{s}{\omega_{Z1}}\right)\left(1+\frac{s}{\omega_{Z2}}\right)}{s\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \quad (7)$$

Where

$$\omega_1 = \frac{1}{R_1(C_1+C_3)},$$

$$\omega_{Z1} = \frac{1}{R_2C_1},\ \omega_{Z2} = \frac{1}{C_2(R_1+R_3)},$$

$$\omega_{P1} = \frac{1}{R_3C_2},\ \omega_{P2} = \frac{1}{R_2\frac{C_1C_3}{C_1+C_3}}$$

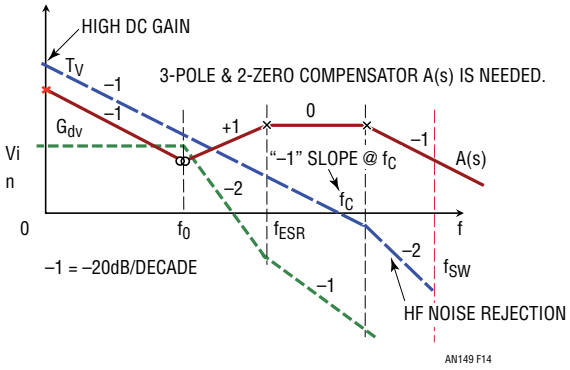
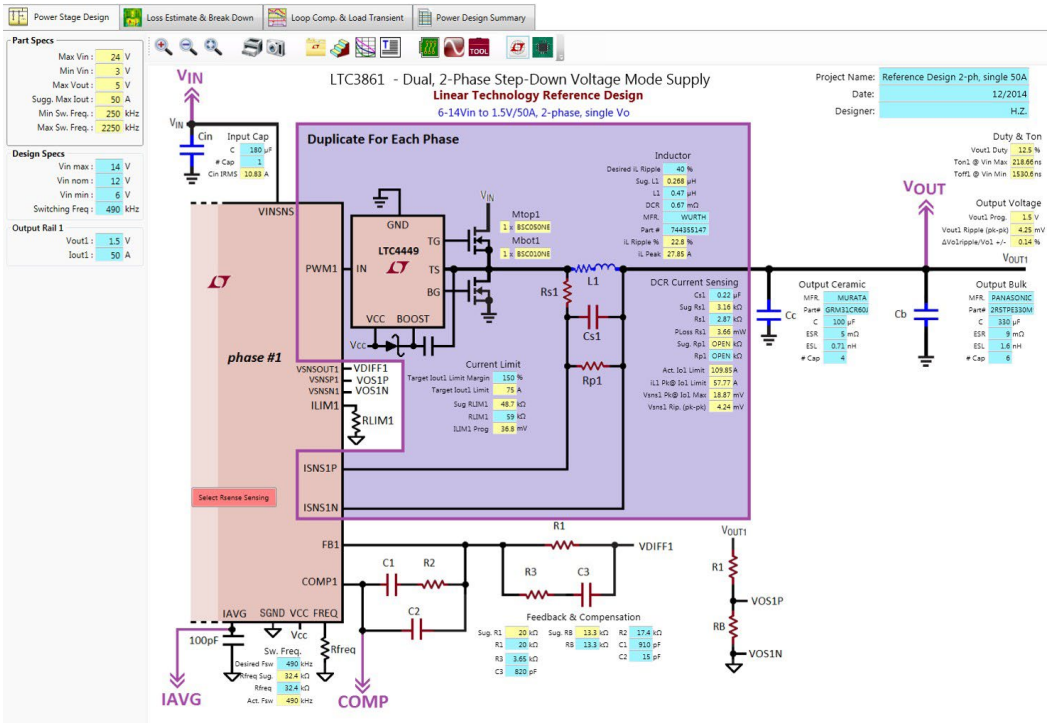
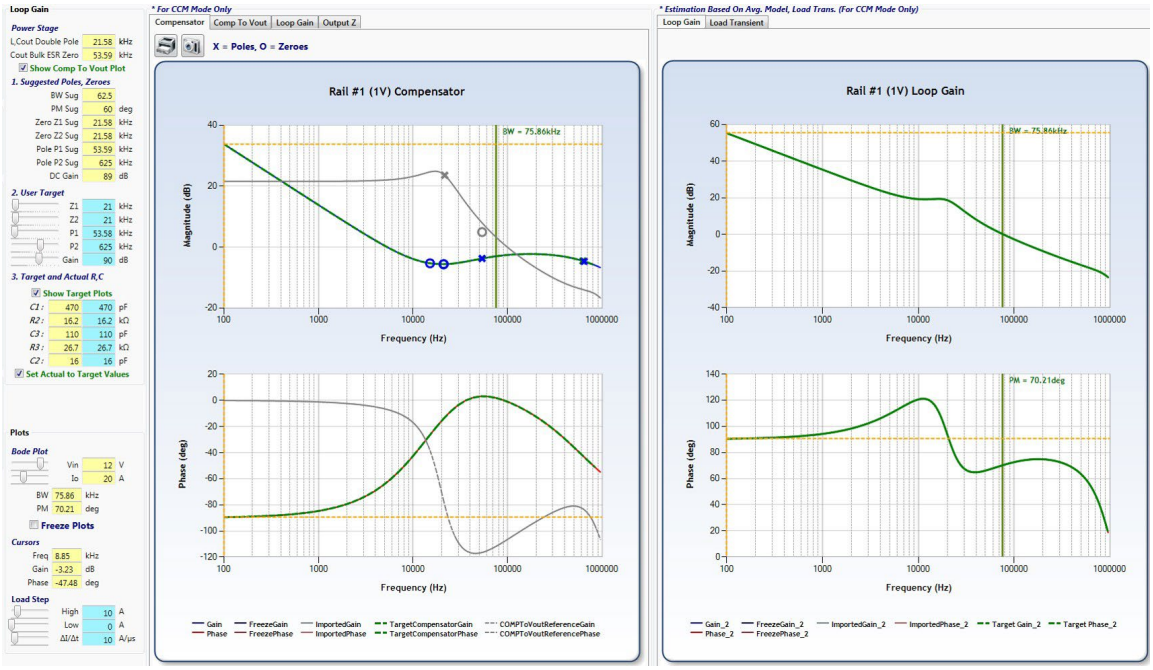


Figure 14. Type III Compensation A(s) Provides 3 Poles and 2 Zeros to Achieve Optimum Total Loop Gain $T_V(s)$

To simplify and automate the switching mode supply design, the LTpowerCAD design tool has been developed. This tool makes loop compensation design a much simpler task. LTpowerCAD is a free-download design tool available at www.linear.com/LTpowerCAD. It helps users to select a power solution, design power stage components, and optimize supply efficiency and loop compensation. As shown in the Figure 15 example, for a given Linear Technology® voltage mode controller such as the LTC3861, its loop parameters are modeled in the design tool. For a given power stage, users can place the pole and zero locations (frequencies), then follow the program guide to put in real R/C values and check the overall loop gain and load transient performance in real time. After that, the design can also be exported to an LTspice® simulation circuit for a real time simulation.



(a) LTpowerCAD Power Stage Design Page



(b) LTpowerCAD Loop Compensation and Load Transient Design Page

Figure 15. LTpowerCAD Design Tool Eases the Type III Loop Design for Voltage Mode Converters (Free-download from www.linear.com/LTpowerCAD)

ADDING A CURRENT LOOP FOR CURRENT MODE CONTROL

The single loop voltage mode control has some limitations. It requires a fairly complicated Type III compensation network. The loop performance can vary significantly with output capacitor parameters and parasitics, especially the capacitor ESR and PCB trace impedance. A reliable supply also requires fast overcurrent protection, which requires a fast current sensing method and fast protection comparator. For high current solutions which require paralleling of many phases, an additional current sharing network/ loop is required.

Adding an inner current sensing path and feedback loop to the voltage-mode converter makes it a current mode-controlled converter. Figures 16 and 17 show the typical peak current-mode buck converter and how it works. The internal clock turns on the topside control FET. After that, as soon as the sensed peak inductor current signal reaches the amplifier ITH pin voltage V_C, the top FET is turned off. Conceptually, the current loop makes the inductor a controlled current source. Therefore, the power stage with closed current loop becomes a 1st-order system, instead of a 2nd-order system with L/C resonance. As a result, the phase lag caused by the power stage poles decreases from 180 degrees to about 90 degrees. Less phase delay makes it much easier to compensate the outer voltage loop. This also makes the power supply less sensitive to output capacitor or inductance variation, as shown in Figure 18.

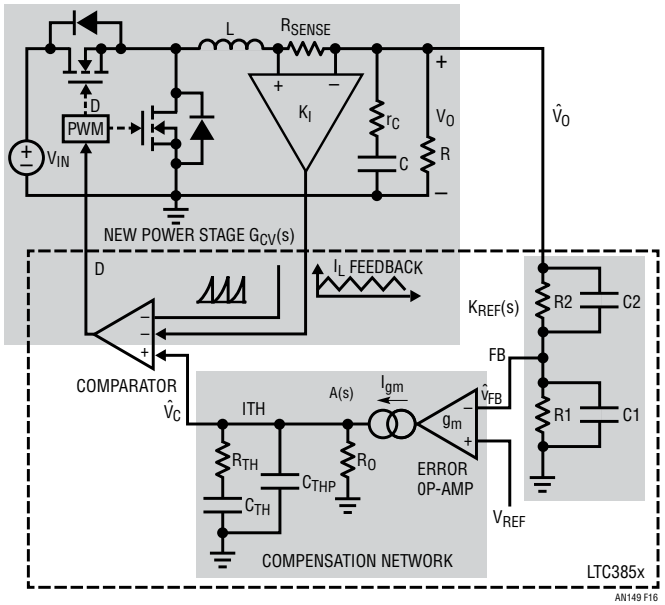


Figure 16. Block Diagram of Current-Mode Converter with an Inner Current Loop and Outer Voltage Feedback Loop

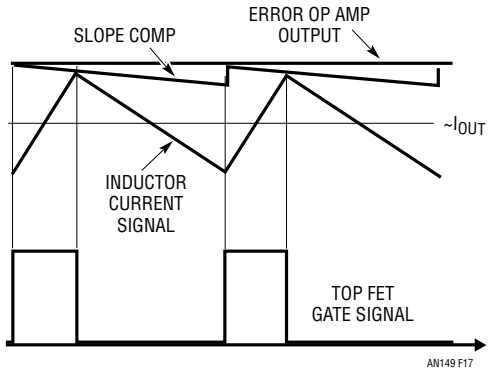


Figure 17. Peak Current Mode Control Signal Waveforms

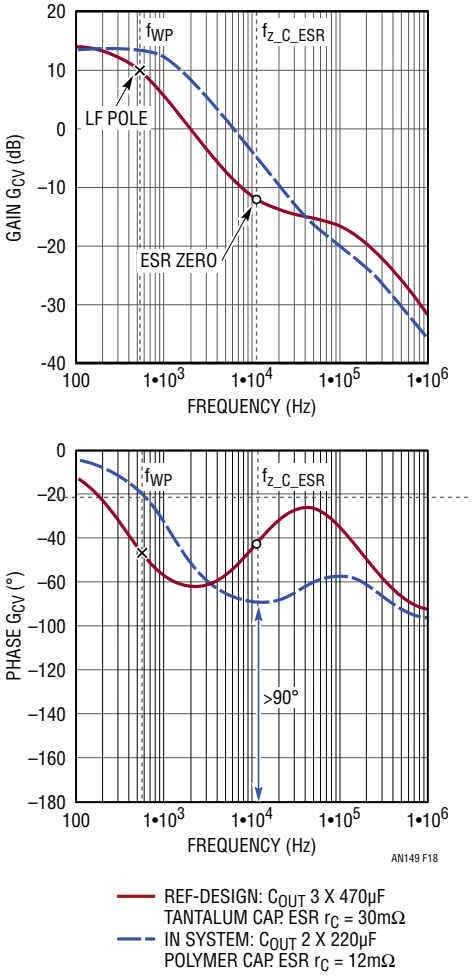


Figure 18. New Power Stage Transfer Function $G_{CV}(s)$ with Closed Current Loop

The inductor current signal can be sensed directly with an additional R_{SENSE}, or indirectly via the inductor winding DCR or FET $R_{DS(ON)}$. All provide several other important benefits from current mode control. As shown in Figure 17, since the inductor current is sensed and limited by the amplifier output voltage in a cycle-by-cycle fashion, the

system has a more accurate and faster current limit under overload or inductor current saturation. The inrush inductor current is also tightly controlled during power-up or input voltage transients. When multiple converters/phases are paralleled, with current mode control, it is very easy to share current among supplies by tying the amplifier ITH pins together to implement a reliable PolyPhase® design. Typical current mode controllers include Linear Technology's LTC3851A, LTC3833 and LTC3855, etc.

Peak vs. Valley Current Mode Control Methods

The current mode control method shown in Figures 16 and 17 is peak inductor current mode control. The converter operates with a fixed switching frequency f_{SW}, making it easy for clock synchronization and phase interleaving, especially for paralleled converters. However, if the load step-up transient occurs just after the control FET gate is turned off, the converter has to wait the FET off-time T_{OFF} until the next clock cycle to respond to the transient. This T_{OFF} delay is usually not a problem, but it matters for a really fast transient system. Besides, the control FET minimum on-time (T_{ON_min}) cannot be really small since the current comparator needs noise blanking time to avoid false triggering. This limits the maximum switching frequency f_{SW} for high V_{IN}/V_{OUT} step-down ratio applications. In addition, peak current mode control also requires certain slope compensation to keep the current loop stable when the duty-cycle is over 50%. This is not a problem for Linear Technology's controllers which usually have built-in adaptive slope compensation to ensure current loop stability over the full duty-cycle range. The LTC3851A and LTC3855 are typical peak current mode controllers.

Valley current mode controllers generate a controlled FET on-time and wait till the inductor valley current reaches its valley limit (V_{ITH}) to turn on the control FET again. Therefore, the supply can respond to load step-up transients during the control FET T_{OFF}. Besides, since the on-time is fixed, the control FET T_{ON_min} can be smaller than with peak current mode control to allow higher f_{SW} for high step-down ratio applications. Valley current mode control also does not need additional slope compensation for current loop stability. However, since the switching period T_S is allowed to vary, the switching node waveform may look more jittery on the scope with valley current mode control. The LTC3833 and LTC3838 are typical valley current mode controllers.

MODELING NEW POWER STAGE WITH CLOSED CURRENT LOOP

Figure 19 shows a simplified 1st order model of the buck converter power stage with inner current loop by just treating the inductor as a current source controlled by amplifier ITH pin voltage υ_C. A similar method can be used for other topologies with inductor current mode control. How good is this simple model? Figure 20 shows the comparison of transfer function $G_{CV}(s) = v_{OUT}/v_C$ between the 1st order model and a more complicated but accurate model. It is for a current mode buck converter running at 500kHz switching frequency. In this example, the 1st order model is accurate up to 10kHz, ~1/50 of the switching frequency f_{SW}. After that, the phase plot of the 1st order model is no longer accurate. So this simplified model is only good for a design with low bandwidth.

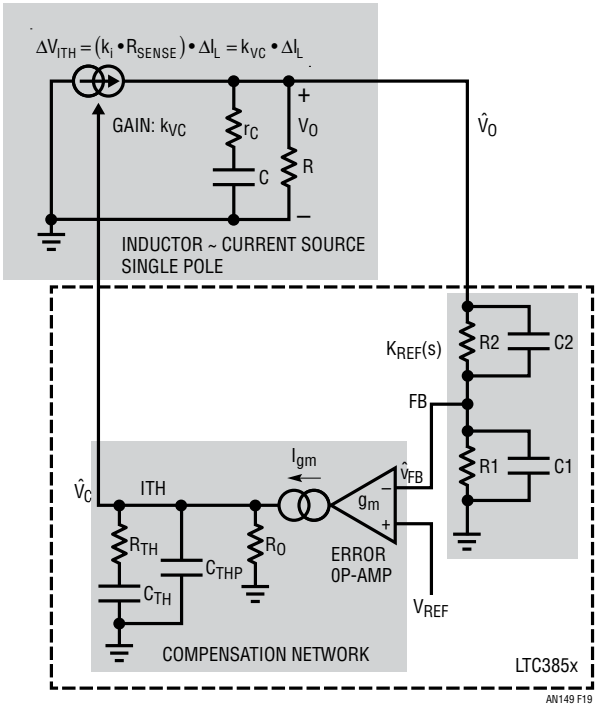


Figure 19. A Simple, 1st Order Model for a Current Mode Buck Converter

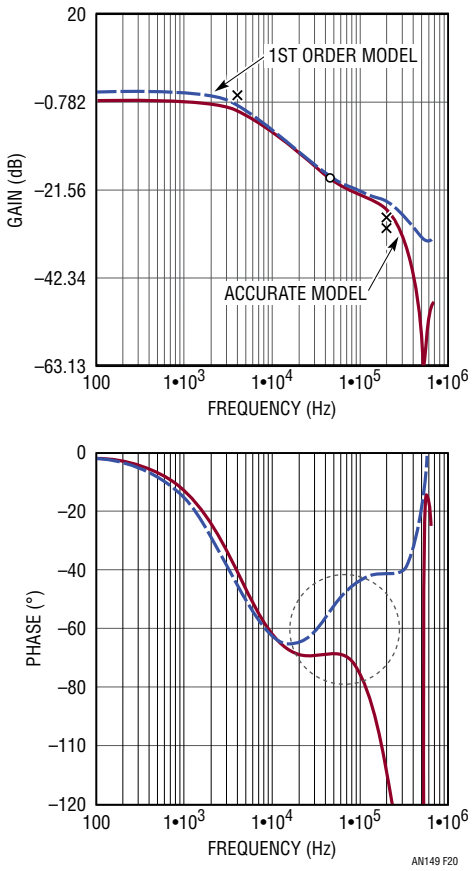


Figure 20. $G_{CV}(s)$ Comparison Between the 1st Order Model and Accurate Model for a Current Mode Buck

In fact, it is quite complicated to develop an accurate small signal model for current mode converters for the full frequency range. R. Ridley's current mode model [3] is the most popular one used by the power supply industry for both peak current mode and valley current mode controls. Most recently, Jian Li developed a more intuitive circuit model [4] for current mode control, which can also be used for other current mode control methods. To make it easy, the LTpowerCAD design tool implements these accurate models, so even an inexperienced user can easily design a current mode power supply, without much knowledge of Ridley or Jian Li's models.

LOOP COMPENSATION DESIGN OF A CURRENT MODE CONVERTER

In Figures 16 and 21, the power stage $G_{cv}(s)$ with closed current loop is determined by the selection of power stage components, which are mainly decided by the DC specifications/performances of the power supply. The outer voltage loop gain $T(s) = G_{CV}(s) \bullet A(s) \bullet K_{REF}(s)$ is therefore determined by the voltage feedback stage $K_{ref}(s)$ and compensation stage A(s). The designs of these two stages will largely decide the supply stability and transient response.

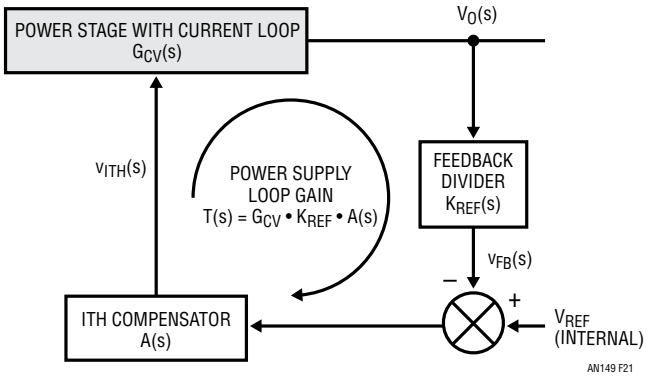


Figure 21. Control Block Diagram for Feedback Loop Design

In general, the performance of the closed voltage loop T(s) is evaluated by two important values: the loop bandwidth and the loop stability margin. The loop bandwidth is quantified by the crossover frequency f_C, at which the loop gain T(s) equals one (0dB). The loop stability margin is typically quantified by the phase margin or gain margin. The loop phase margin ϕ_m is defined as the difference between the overall T(s) phase delay and –180° at the crossover frequency. A 45-degree or 60-degree minimum phase margin is usually needed to ensure stability. For current mode control, to attenuate switching noise in the current loop, the loop gain margin is defined as the attenuation at ½ • f_{SW}. In general, a minimum 8dB attenuation (–8dB loop gain) at ½ • f_{SW} is desired.

Select Desired Voltage-Loop Crossover Frequency f_C

Higher bandwidth helps obtain fast transient response. However, increasing the bandwidth usually reduces the stability margin and makes the control loop more sensitive to switching noise. An optimum design usually achieves a good trade-off between the bandwidth (transient response) and stability margin. In fact, current mode control also introduces a pair of double-poles ϖ_n by the sampling effect of the current signal at 1/2 • f_{SW} [3]. These double poles introduce an undesirable phase delay around ½ • f_{SW}. In general, to obtain sufficient phase margin and PCB noise

attenuation, the crossover frequency is selected to be less than 1/10–1/6 of the phase switching frequency f_{SW}.

$$f_C \le \frac{f_{SW}}{6} \quad (8)$$

Design of the Feedback Divider Network $K_{ref}(s)$ with R1, R2, C1 and C2

In Figure 16, the DC gain K_{REF} of $K_{ref}(s)$ is the ratio between the internal reference voltage V_{REF} and the desired DC output voltage V_o. Resistors R1 and R2 are used to set the desired output DC voltage.

$$R_1 = \frac{K_{REF} \bullet R_2}{1 - K_{REF}} \quad (9)$$

where

$$K_{REF} = \frac{V_{REF}}{V_o} \quad (10)$$

The optional capacitor C2 can be added to improve the dynamic response of the feedback loop. Conceptually, at high frequency, C2 provides a low impedance feed-forward path for the output voltage AC signal and therefore, speeds up transient responses. But C2 may also bring undesirable switching noise into the control loop. Therefore, an optional C1 filter capacitor may be added to attenuate the switching noise. As shown in Equation 11, the overall resistor divider transfer function $K_{REF}(s)$ with C1 and C2 has one zero and one pole. Figure 22 shows the bode plot of $K_{REF}(s)$. By designing $f_{z\_ref} < f_{p\_ref}$, C1 and C2 together with R1 and R2 introduce a phase boost in a frequency band centered at f_{CENTER}, which is given in equation (14). If f_{CENTER} is placed at the targeted crossover frequency f_C, $K_{ref}(s)$ provides phase lead to the voltage loop and increases the phase margin. On the other hand, Figure 22 also shows that C1 and C2 increase the divider gain at high frequency. This is undesirable because a gain increase at high frequency makes the control loop more sensitive to switching noise. The increase in high-frequency gain by C1 and C2 is given by Equation 15.

$$K_{REF}(s) = \frac{v_{FB}}{v_o} = K_{REF} \bullet \frac{1 + \frac{s}{2\pi \bullet f_{z\_ref}}}{1 + \frac{s}{2\pi \bullet f_{p\_ref}}} \quad (11)$$

where:

$$f_{z\_ref} = \frac{1}{2\pi \bullet R_2 \bullet C_2} \quad (12)$$

and

$$f_{p\_ref} = \frac{1}{K_{REF}} \bullet \frac{1}{2\pi \bullet R_2 \bullet (C_1 + C_2)} \quad (13)$$

$$f_{CENTER} = \sqrt{f_{z\_ref} \bullet f_{p\_ref}} \quad (14)$$

$$= \frac{1}{2\pi \bullet R_2} \bullet \sqrt{\frac{1}{K_{REF} \bullet C_2 \bullet (C_1 + C_2)}} = f_C$$

$$\Delta Gain_{HF(dB)} = 20 \bullet \log\left(\frac{C_2}{C_1 + C_2} \bullet \frac{1}{K_{REF}}\right) \quad (15)$$

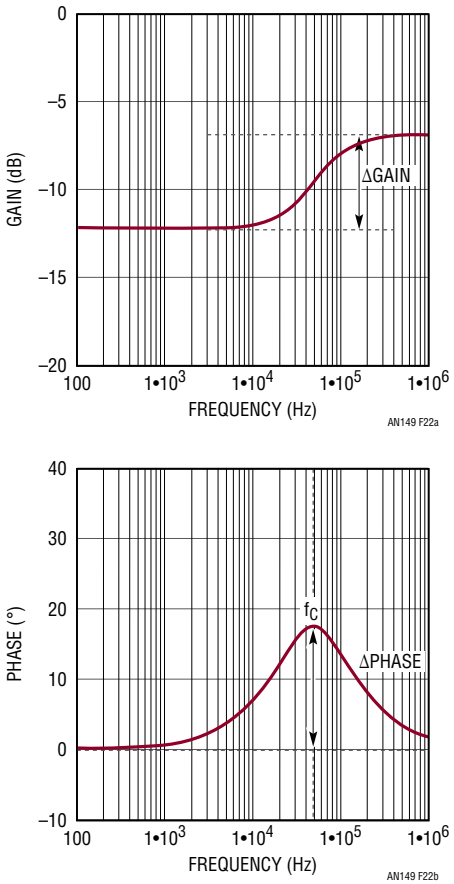


Figure 22. Transfer Function Bode Plot of Resistor Divider Gain $K_{REF}(s)$

For a given C1 and C2, the increased phase φ_{REF} from the divider network can be calculated by Equation 16. Further, the maximum possible phase boost for a given output voltage is given by Equation 17, for C2 >> C1. As shown, the maximum phase boost φ_{REF_max} is determined by the divider ratio $K_{REF} = V_{REF}/V_O$. Since V_{REF} is fixed for a given controller, higher phase boost can be achieved with higher output voltage V_O.

$$\varphi_{REF} = 2 \bullet \tan^{-1}\left(\sqrt{\frac{C_2}{C_1 + C_2} \bullet \frac{1}{K_{REF}}}\right) - 90 \qquad (16)$$

$$\varphi_{REF} = 2 \bullet \tan^{-1}\left(\sqrt{\frac{1}{K_{REF}}}\right) - 90 \qquad (17)$$

The selections of φ_{REF}, C1 and C2 are a trade-off between desired phase boost and undesired high frequency gain increase. The overall loop gain needs to be checked later for optimized values.

Design Type II Compensation Network of Voltage-Loop ITH Error Amplifier

The ITH compensation A(s) is most critical to the loop compensation design because it determines the DC gain, crossover frequency (bandwidth) and the phase/gain margins of the supply voltage loop. For a current source output, g_m transconductance-type amplifier, its transfer function A(s) is given by Equation 18:

$$A(s) = \frac{v_{ith}(s)}{v_{FB}(s)} = g_m \bullet Z_{ith}(s) \qquad (18)$$

where, g_m is the gain of the transconductance error amplifier. $Z_{ith}(s)$ is the impedance of the compensation network at the amplifier output ITH pin.

From the control block diagram in Fig.21, the voltage loop regulation error can be quantified by:

$$\frac{Error}{V_o} = \frac{V_{REF} - V_{FB}}{V_{REF}} = \frac{1}{\left[A(s) \bullet G_{CV}(s)\right]_{S=j2\pi f}} \qquad (19)$$

Therefore, to minimize the DC regulation error, a large DC gain of A(s) is very desirable. To maximize the DC gain of A(s), a capacitor C_{th} is first placed at the amplifier output ITH pin to form an integrator. In this case, the A(s) transfer gain is:

$$A(s) = \frac{v_{ith}(s)}{v_{FB}(s)} = \frac{g_m}{C_{th}} \bullet \frac{1}{s} \qquad (20)$$

Figure 23 shows the schematic diagram of A(s) and its Bode plot. As shown, capacitor C_{th} creates an integration term in A(s) with an infinitely high DC gain. Unfortunately, in addition to the original –180 degrees of negative feedback, C_{th} adds another –90 degrees phase lag. Including the –90 degree phase of the 1st-order system power stage $G_{CV}(s)$, the total voltage loop phase is close to –360 degrees at the crossover frequency f_C and the loop is close to being unstable.

In reality, the output impedance of the current source g_m amplifier is not an infinite value. In Figure 24, R_o is the internal output resistance of the gm amplifier ITH pin. Linear Technology controllers' R_o is usually high, in the 500kΩ – 1MΩ range. Therefore, the single capacitor A(s) transfer function becomes Equation (21). It has a low frequency pole fpo determined by $R_O \bullet C_{th}$. So the DC gain of A(s) is actually $g_m \bullet R_O$. As shown in Figure 24, A(s) still has –90 degree phase lag at the expected crossover frequency f_{C_exp}.

$$A(s) = \frac{v_{ith}(s)}{v_{FB}(s)} = g_m \bullet R_o \bullet \frac{1}{1 + s/s_{po}} \qquad (21)$$

where,

$$s_{po} = \frac{1}{R_o \bullet C_{th}} \qquad (22)$$

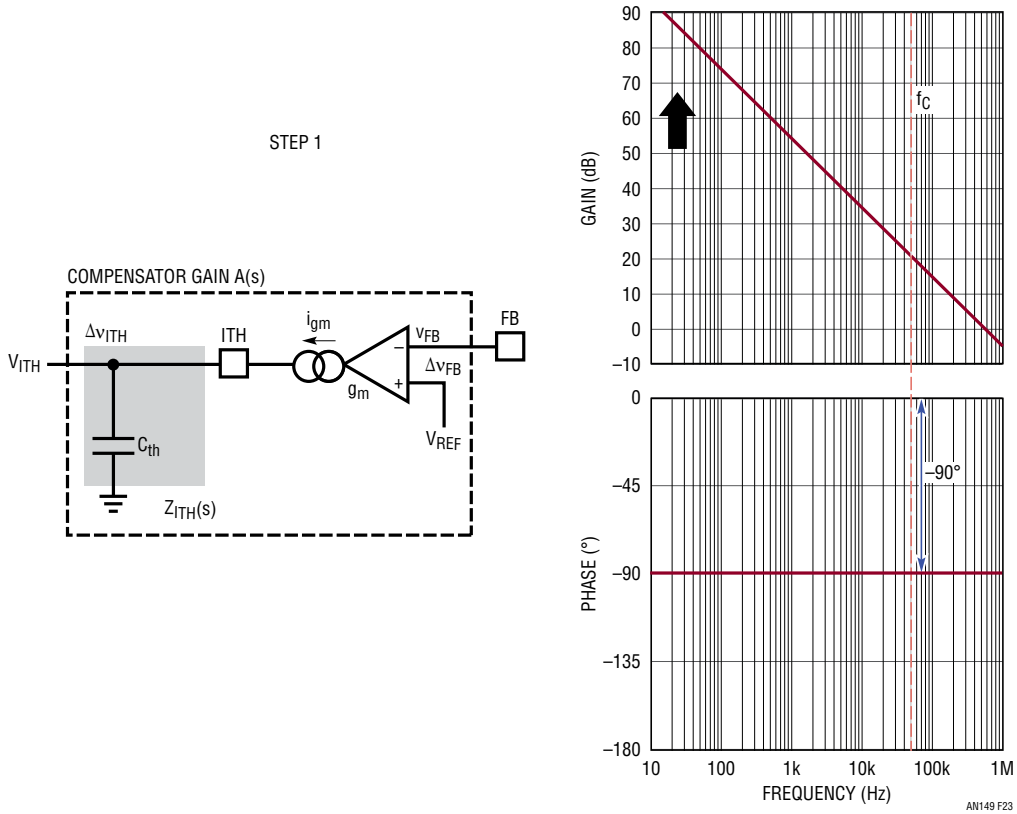


Figure 23. Step 1: Simple Capacitor Compensation Network A(s) and Its Bode Plot

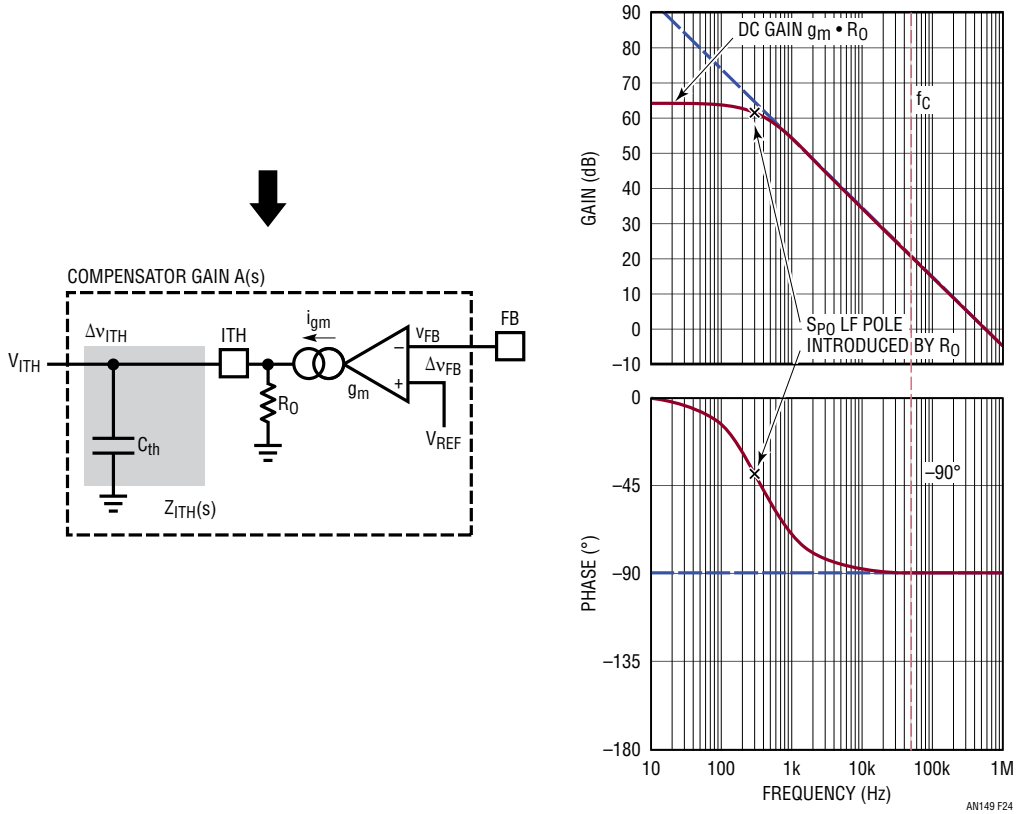


Figure 24. One-Pole A(s) That Includes g_m Amplifier Output Impedance R_O

To increase the phase at f_C, a resistor R_{th} is added in series with C_{th} to create a zero, as shown in Equation 23 and Figure 25. The zero contributes up to +90 degree phase lead. As shown in Figure 25, if the zero s_{thz} is placed before the crossover frequency f_C, A(s)'s phase at f_C can be significantly increased. As a result, it increases the phase margin of the voltage loop.

$$A(s) = \frac{v_{ith}(s)}{v_{FB}(s)} = g_m \bullet R_o \bullet \frac{1 + s/s_{thz}}{1 + s/s_{po}} \quad (23)$$

where,

$$s_{thz} = \frac{1}{R_{th} \bullet C_{th}} \quad (24)$$

Unfortunately, there is a penalty of adding the zero s_{thz}—the gain of A(s) is significantly increased at high frequency beyond f_C. So the switching noise is more likely to come into the control loop with less A(s) attenuation at the switching frequency. To compensate this gain increase and attenuate PCB noise, it is necessary to add another small ceramic capacitor C_{thp} from the ITH pin to IC signal ground, as shown in Figure 26. Typically, choose $C_{thp} << C_{th}$. In the PCB layout, filter capacitor C_{thp} should be placed as close to the ITH pin as possible. By adding C_{thp}, the final compensation transfer function A(s) is given in Equation 25 and Equation 26 and its Bode plot is shown in Figure 26. C_{thp} introduces a high-frequency pole s_{thp}, which should be located between the crossover frequency f_C and the switching frequency f_S. C_{thp} reduces A(s) gain at f_S, but

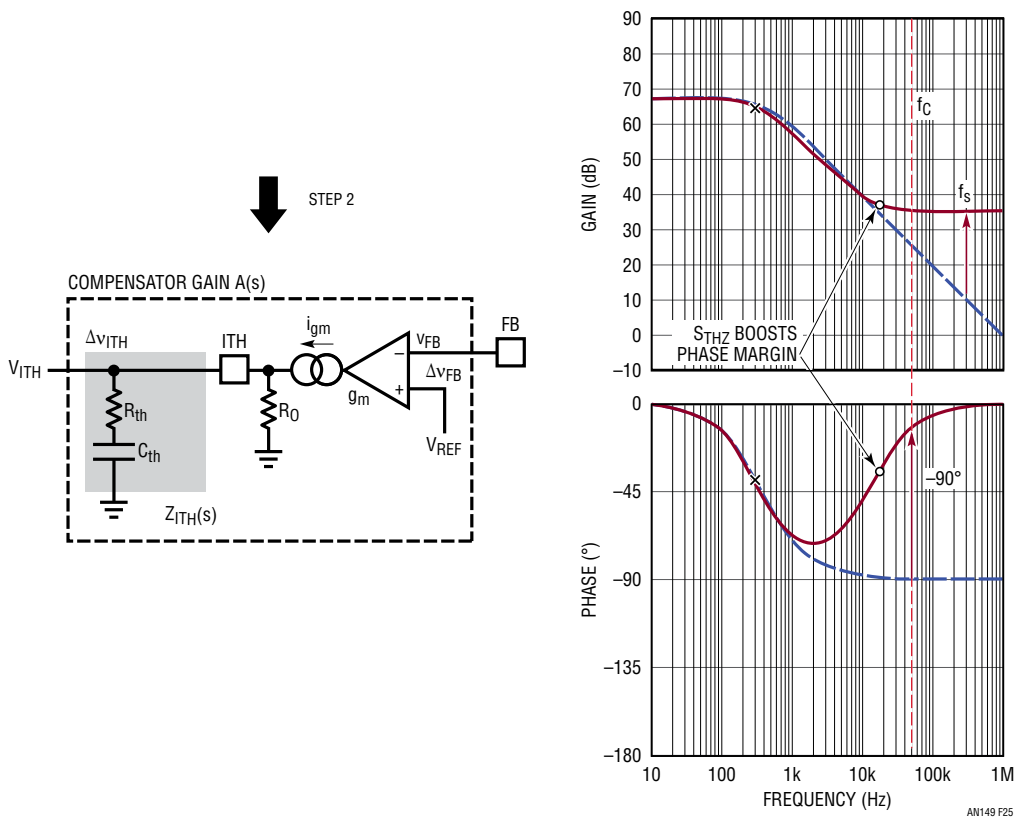


Figure 25 Step 2: Adding R_{TH} Zero to Boost Phase — One-Pole, One-Zero Compensation A(s)

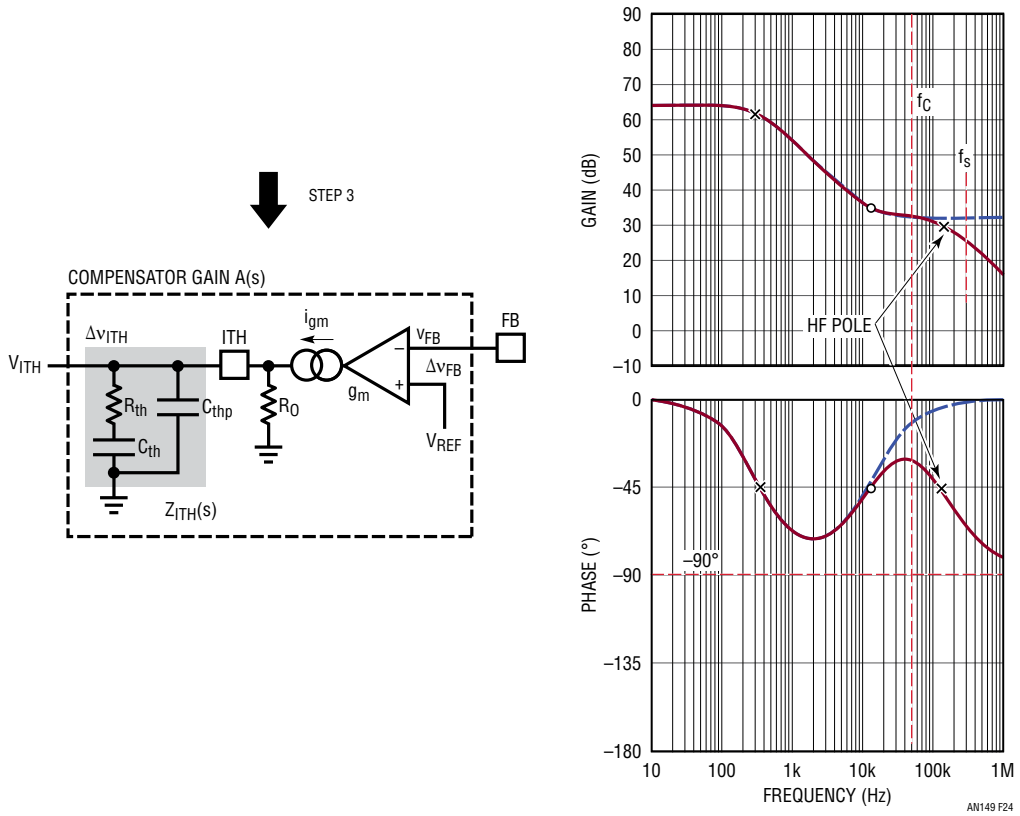


Figure 26. Step 3: Adding High Frequency Decoupling C_{thp} - Two-Pole, One-Zero Compensation A(S)

may also decrease the phase at f_C. The location of s_{thp} is a trade-off between the phase margin and supply PCB noise immunity.

$$A(s) = \frac{v_{ith}(s)}{v_{FB}(s)} = g_m \bullet R_o \bullet \frac{1 + \frac{s}{s_{thz}}}{\left(1 + \frac{s}{s_{po}}\right) \bullet \left(1 + \frac{s}{s_{thp}}\right)} \quad (25)$$

where,

$$s_{thp} = \frac{1}{R_{th} \bullet \frac{C_{th} \bullet C_{thp}}{C_{th} + C_{thp}}} \approx \frac{1}{R_{th} \bullet C_{thp}} \text{ if } C_{thp} << C_{th} \quad (26)$$

Since the current mode power stage is a quasi-single-pole system, the two-pole and one-zero compensation network in Figure 26 is generally sufficient to provide the needed phase margin.

This two-pole, one-zero compensation network on the amplifier ITH pin is also called a Type II compensation network. In summary, there are two capacitors C_{TH} and C_{THP}, and one resistor R_{TH}. This R/C network together with the amplifier output resistance R_o, generates a typical transfer function shown in Figure 27, with one zero at f_{z1} and two poles at f_{po} and f_{p2}.

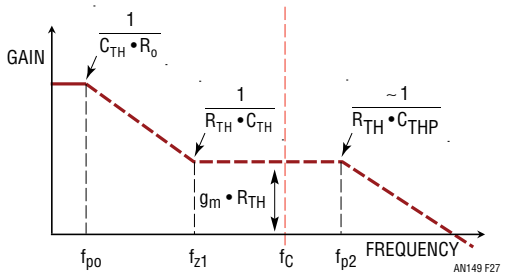


Figure 27. Conceptual Plot of Type II Compensation Network Transfer Function

Compensation R/C Values vs. Load Step Transient Response

The previous section explained the frequency domain behavior of the Type II compensation network. In a closed-loop supply design, one important performance parameter is the supply's output voltage undershoot (or overshoot) during a load step-up (or load step-down) transient, which is usually directly impacted by loop compensation design.

1) C_{TH}'s effects on a load step transient. The C_{TH} affects the location of low frequency pole f_{po} and zero f_{z1}. As shown in Figure 28, a smaller C_{TH} can increase the low-to-mid frequency gain of transfer function A(s). As a result, it can reduce the load transient response settling time without much impact on the V_{OUT} undershoot (or overshoot) amplitude. On the other hand, a smaller C_{TH} means higher f_{z1} frequency. This may reduce the phase boost by f_{z1} at the targeted crossover frequency f_C.

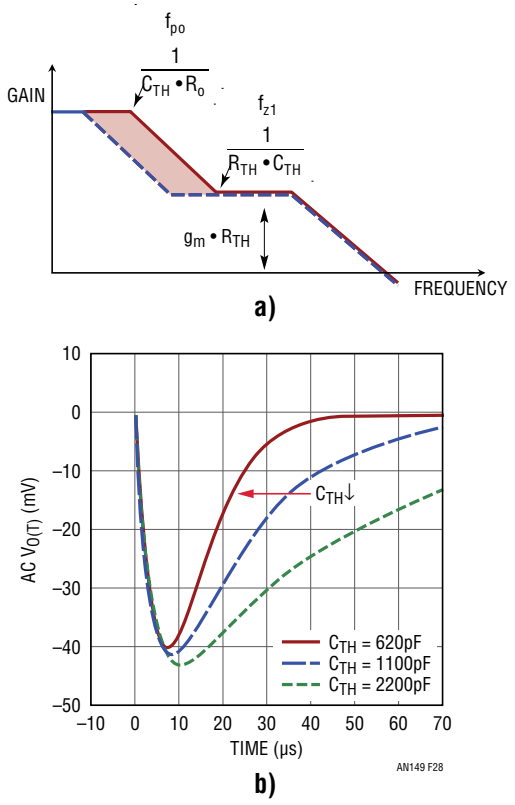


Figure 28. C_{TH}'s Effects on Transfer Function and Load Transient

2) R_{TH}'s effects on load step transient. Figure 29 shows that the R_{TH} affects the location of zero f_{z1} and pole f_{p2}. More importantly, a larger R_{TH} increases the A(s) gain between f_{z1} and f_{p2}. As a result, a larger R_{TH} directly increases the supply bandwidth f_c and reduces the V_{OUT} undershoot/overshoot at load transient. However, if R_{TH} is too large, the supply bandwidth f_c can be too high with insufficient phase margin.

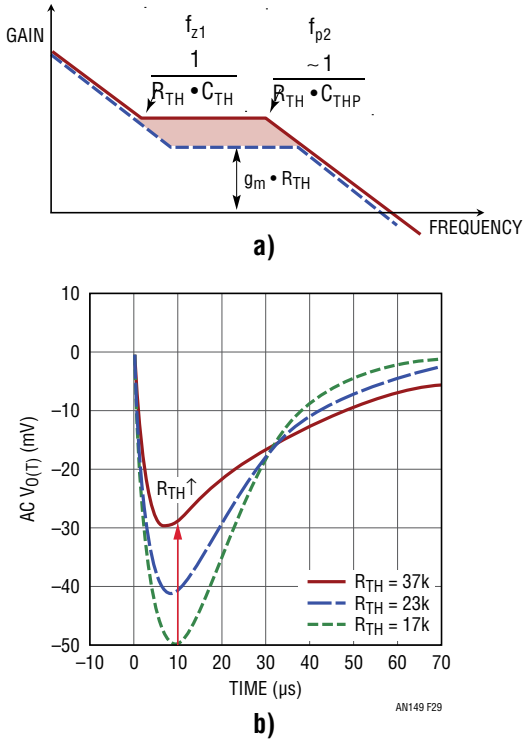


Figure 29. R_{TH}'s Effects on Transfer Function and Load Transient

3) C_{THP}'s effects on load step transient. Figure 30 shows that C_{THP} affects the location of pole f_{p2}. C_{THP} is used as a decoupling capacitor to reduce switching noise on the ITH pin to minimize switching jitter. If the supply bandwidth $f_c > f_{p2}$, C_{THP} does not impact load transient response much. If C_{THP} is overdesigned so that f_{p2} is close to f_c, it can reduce the bandwidth and phase margin, resulting in increased transient undershoot/overshoot.

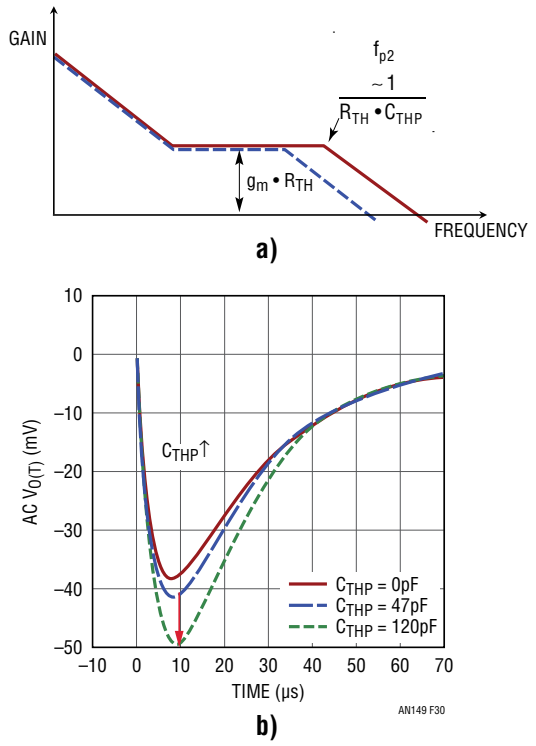


Figure 30. C_{THP}'s Effects on Transfer Function and Load Transient

DESIGN A CURRENT MODE SUPPLY WITH THE LTpowerCAD DESIGN TOOL

With the LTpowerCAD design tool, users can easily design and optimize loop compensation and load transient performance of Linear Technology's current mode supplies. Many Linear products have been accurately modeled with their loop parameters. First, users need to design the power stage, in which they need to design the current sensing network and ensure a sufficient AC sensing signal to the IC. After that, on the loop design page, they can adjust the loop compensation R/C values by simply moving the sliding bars and observing the overall loop bandwidth, phase margin and corresponding load transient performance. For a buck converter, users usually need to design a bandwidth below 1/6 f_{SW}, have at least 45 degrees (or 60 degrees) of phase margin and have at least 8dB total loop gain attenuation at ½ f_{SW}. For a boost converter, because of the right-half-plane zero (RHPZ), users need to design the supply bandwidth below 1/10 of the worst case RHPZ frequency. The LTpowerCAD design file can be exported to LTspice® for real-time simulation to check detailed supply dynamic performance, such as load transient, power-up/down, overcurrent protection, etc.

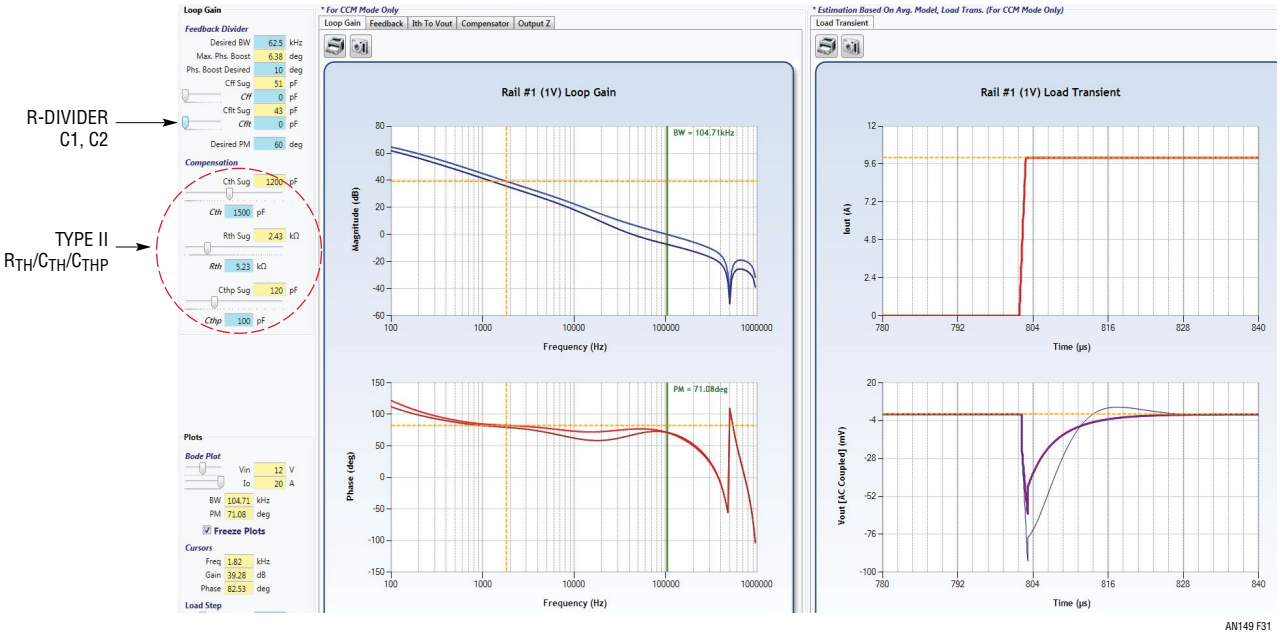


Figure 31. LTpowerCAD Design Tool Eases Loop Compensation Design and Transient Optimization

MEASURE THE SUPPLY LOOP GAIN

The LTpowerCAD and LTspice programs are not intended to replace final bench loop gain measurement of the real power supply. It is always necessary to make a measurement before releasing the design for final production. Though the models of power supplies are theoretically correct, they cannot take full account of circuit parasitics and component nonlinearity, such as the ESR variations of output capacitors, the nonlinearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. That's why, sometimes, the theoretical model and measurement can diverge considerably. If this happens, a load transient test can be used to further confirm the loop stability.

Figure 32 shows the typical supply loop gain measurement setup of a nonisolated power supply using a frequency analyzer system. To measure the loop gain, a 50Ω to 100Ω resistor is inserted into the voltage feedback loop and a 50mV isolated AC signal is applied on this resistor. Channel 2 is connected to the output voltage and Channel 1 is connected to the other side of this resistor. The loop gain is calculated as Ch2/Ch1 by the frequency analyzer system. Figure 33 shows the measured and LTpowerCAD calculated loop Bode plot of a typical LTC3851A current mode supply. They have good matching in the critical frequency range from 1kHz to 100kHz.

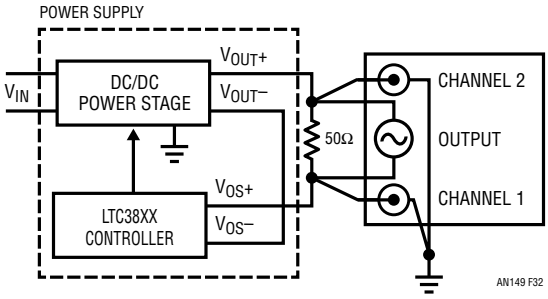


Figure 32. Test Setup of the Power Supply Loop Gain Measurement

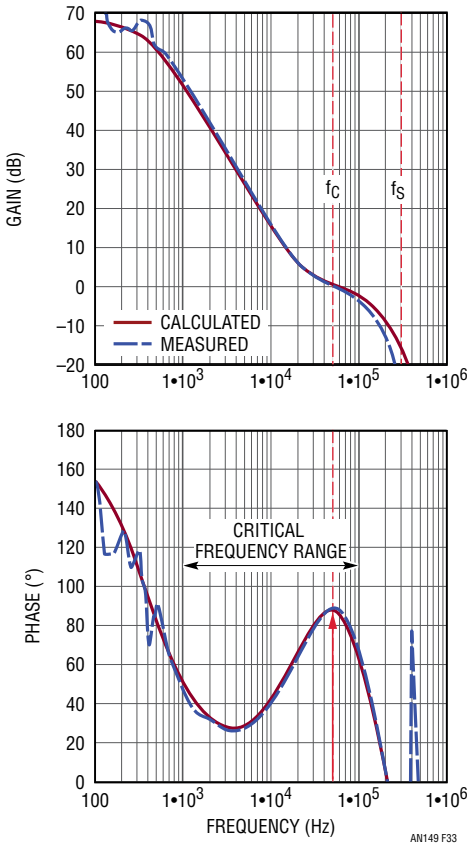


Figure 33. Measured and LTpowerCAD Modeled Loop Gain of a Current Mode Buck Converter

OTHER REASONS THAT CAUSE INSTABILITY

Operating Conditions:

If the supply switching or output voltage waveform looks unstable or jittery on the oscilloscope, first, users need to make sure the supply is operated in a steady state condition, without load or input voltage transients. For very small or very large duty cycle applications, if pulse-skipping operation happens, check whether the minimum on-time or off-time limitation has been reached. For supplies that require an external synchronization signal, make sure the signal is clean and within the linear range given by controller data sheet. Sometimes it is also necessary to adjust the phase-locked-loop (PLL) filter network.

Current Sensing Signal and Noise:

To minimize the sensing resistor power loss, in a current mode supply, the maximum current sensing voltage is typically very low. For example, LTC3851A may have 50mV maximum sensing voltage. It is possible for PCB noise to disturb the current sensing loop and cause an unstable switching behavior. To debug whether the problem is indeed a loop compensation problem, a large 0.1µF capacitor can be placed from ITH pin to IC ground. If the supply is still unstable with this capacitor, the next step is to review the design. In general, the inductor and current sensing network should be designed to have at least 10mV to 15mV peak-to-peak AC inductor current signal on the IC current sensing pin. Besides, the current sensing traces can be rerouted with a pair of twisted jumper wires to check if it solves the problem.

There are some important considerations for PCB layout [6]. In general, Kelvin sensing is usually required with a pair of closely routed current sensing traces back to $SENSE^+$ and $SENSE^-$ pins. If a PCB via is used in the $SENSE^-$ net, make sure this via does not contact other V_{OUT} planes. The filter capacitor across $SENSE^+$ and $SENSE^-$ should be placed as close to the IC pins as possible with a direct trace connection. Sometimes, filter resistors are needed and these resistors must be close to the IC too.

Control Chip Component Placement and Layout:

Placement and layout of components around the control IC are also critical [6]. All the ceramic decoupling capacitors should be close to their pins, if possible. It is especially important for the ITH pin capacitor C_{thp} to be as close to the ITH and IC signal ground pins as possible. The control IC should have a separate signal ground (SGND) island from the power supply power ground (PGND). The switching nodes, such as SW, BOOST, TG and BG, should be kept away from sensitive small signal nodes, such as current sensing, feedback and ITH compensation traces.

SUMMARY

Loop compensation design is often viewed as a challenging task for switching mode power supplies. For applications with fast transient requirements, it is very important to design the supply with high bandwidth and sufficient stability margin. This is typically a time consuming process. This article explains the key concepts to help system engineers understand this task. The LTpowerCAD design tool can be used to make supply loop design and optimization a much simpler task.

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