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Synchronous Step-Down DC-DC Controller Survives 150V Input Surges

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The LTC3895 is a high-voltage non-isolated synchronous step-down switching regulator controller that drives external N-channel MOSFETs. Its 4V to 140V (150V absolute max.) input voltage range allows it to operate from a high-input voltage source or from an input that has high voltage surges. The LTC3895 continues to operate at up to 100% duty cycle during input voltage dips down to 4V, making it suited for transportation, industrial control, robotic and datacom applications (*Fig.*1).

The LTC3895 implements a protection feature that inhibits switching when the input voltage rises above a programmable operating range. By using a resistor divider from the input supply to ground, the OVLO (overvoltage lockout) pin serves as a precise input supply voltage monitor. Switching is disabled when the OVLO pin rises above 1.2V, which can be configured to limit switching to a specific range of input supply voltage. With switching disabled, the LTC3895 can safely sustain input voltages up to the absolute maximum rating of 150V. Input supply overvoltage events trigger a soft-start reset, which results in a graceful recovery from an input supply transient.

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An overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{FB} pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

A PGOOD pin connects to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} pin voltage is not within $\pm 10\%$ of the 0.8V reference voltage. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the V_{FB} pin voltage is within the $\pm 10\%$ requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V.

The LTC3895 uses a constant frequency, current-mode step-down architecture. During normal operation, the external top MOSFET is turned on when the clock sets an RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets

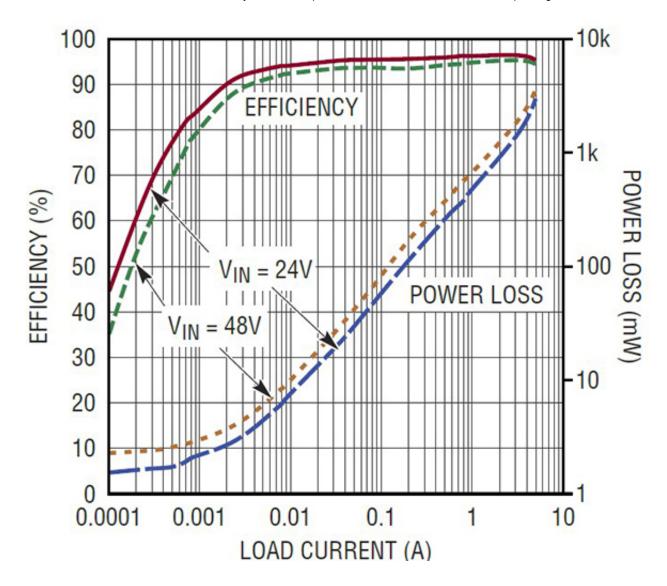
the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT} , to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by a current comparator, or the beginning of the next clock cycle.

Its $40\mu A$ no-load quiescent current extends operating run time in battery-powered systems. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The LTC3895 operates with a selectable fixed frequency between 50kHz and 900kHz and is synchronizable to an external clock from 75kHz to 850kHz. The designer can select from forced continuous operation, pulse-skipping or low ripple Burst Mode operation during light loads. Its current-mode architecture provides easy loop compensation, fast transient response, and excellent line regulation. Current sensing is accomplished by measuring the voltage drop across the output inductor (DCR) for highest efficiency or by using an optional sense resistor. An 80ns minimum on-time allows for high step-down ratios at high switching frequency. Current foldback limits MOSFET heat dissipation during overload conditions. Additional features include an integrated bootstrap diode, adjustable input overvoltage lockout, and soft-start.

To support the external power MOSFETs, you can program the gate drive output voltage from 5V to 10V, which allows use of logic or standard-level FETs. An integrated switch in the top-gate driver eliminates the need for an external bootstrap diode. An internal charge pump allows 100% duty cycle operation.



The output voltage can be set from 0.8V to 6oV using external resistors or pin-programmed for a fixed 5V or 3.3V. Output currents can be up to 2oA with efficiencies as high as 96%. *Figure 2* is a plot of efficiency and power losses vs. load current. This IC draws only 40µA in sleep mode with the output voltage in regulation, ideal for always-on systems. An internal charge pump allows for 100% duty cycle operation in dropout, a useful feature when powered from a battery during discharge. To prevent high on-chip power dissipation in high input voltage applications, the LTC3895 includes an NDRV pin that drives the gate of an optional external N-channel MOSFET acting as a low dropout linear regulator to supply IC power. The EXTV_{CC} pin permits the LTC3895 to be powered from the output of the switching regulator or other available source, reducing power dissipation and improving efficiency.

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} supply voltage can be programmed from 5V to 10V by setting the DRVSET pin. Two separate LDOs can provide power from V_{IN} to DRV_{CC}. The internal V_{IN} LDO uses an internal P-channel pass device between the V_{IN} and DRV_{CC} pins. To prevent high on-chip power dissipation in high-input voltage applications, the LTC3895 also includes an NDRV LDO that utilizes the NDRV pin to supply power to DRV_{CC} by driving the gate of an external N-channel MOSFET acting as a linear regulator with its source connected to DRV_{CC} and drain connected to V_{IN} . The NDRV LDO includes an internal charge pump that allows NDRV to be driven above V_{IN} for low dropout performance.

When the EXTV $_{CC}$ pin is tied to a voltage below its switchover voltage (4.7V or 7.7V depending on the DRVUV pin), the V_{IN} and NDRV LDOs are enabled and one of them supplies power from V_{IN} to DRV $_{CC}$. The V_{IN} LDO has a slightly lower regulation point than the NDRV LDO. If the NDRV LDO is being used with an external N-channel MOSFET, the gate of the MOSFET tied to the NDRV pin is driven such that DRV $_{CC}$ regulates above the V_{IN} LDO

regulation point, causing all DRV_{CC} current to flow through the external N-channel MOSFET, bypassing the internal $V_{\rm IN}$ LDO pass device. If the NDRV LDO is not being used, all DRVCC current flows through the internal P-channel pass device between the $V_{\rm IN}$ and DRV_{CC} pins.

If EXTV_{CC} is taken above its switchover voltage, the V_{IN} and NDRV LDOs are turned off and an EXTV_{CC} LDO is turned on. Once enabled, the EXTV_{CC} LDO supplies power from EXTV_{CC} to DRV_{CC}. Using the EXTV_{CC} pin allows the DRV_{CC} power to be derived from a high efficiency external source such as the LTC3895 switching regulator output.

The INTV_{CC} supply powers most of the other internal circuits in the LTC3895. The INTV_{CC} LDO regulates to a fixed value of 5V and its power is derived from the DRV_CC supply.

The LTC3895 can be shut down using the RUN pin. Connecting the RUN pin below 1.12V shuts down the main control loop. Connecting the RUN pin below 0.7V disables the controller and most internal circuits, including the DRV $_{CC}$ and INTV $_{CC}$ LDOs. In this state, the LTC3895 draws only 10 μ A of quiescent current.

The LTC3895 is available in a TSSOP-38 thermally enhanced package with several pins removed for high voltage spacing. Two operating junction temperature grades are available with extended and industrial versions from -40 to 125°C and a high temp automotive version from -40°C to 150°C.

Looking for parts? Go to Source ESB.

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