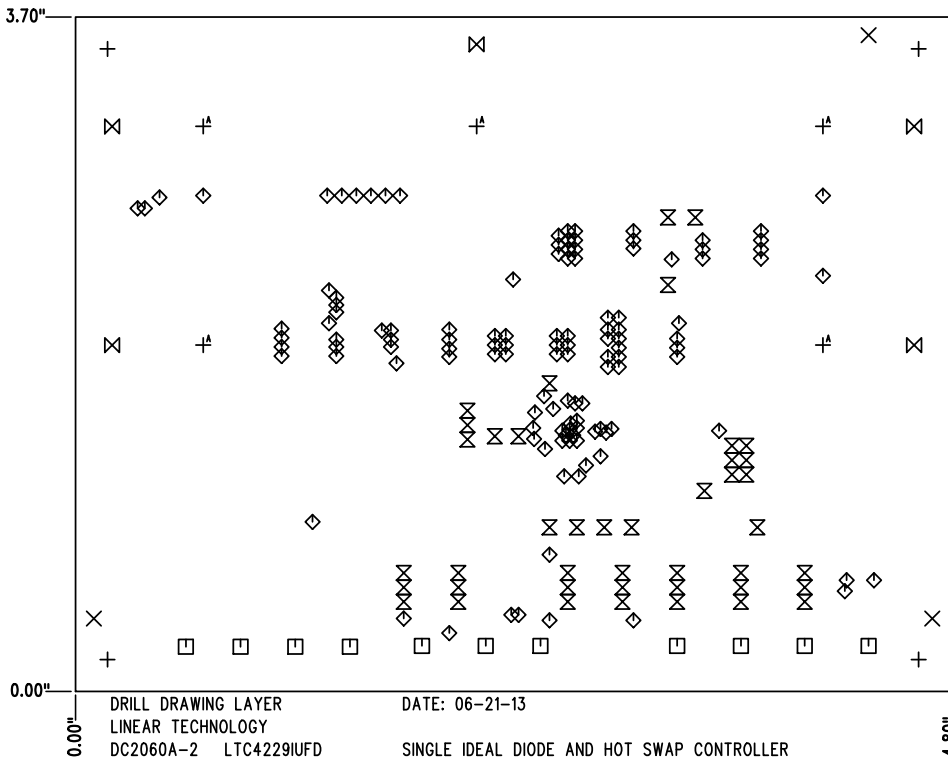


SHOWN FROM TOP SIDE



DRILL DRAWING LAYER
LINEAR TECHNOLOGY
DC2060A-2 LTC4229IUF

DATE: 06-21-13

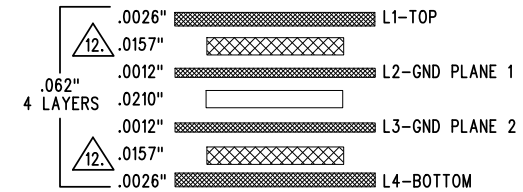
SINGLE IDEAL DIODE AND HOT SWAP CONTROLLER

SIZE	QTY	SYM	PLATED	TOL
0.19	4	+	NO	+/-0.003"
0.07	3	X	NO	+/-0.003"
0.064	11	□	YES	+/-0.003"
0.012	122	◇	YES	+/-0.003"
0.035	42	⊗	YES	+/-0.003"
0.094	5	⊗ ^A	YES	+/-0.003"
0.215	5	⊗ ^A	YES	+/-0.003"

REVISION HISTORY

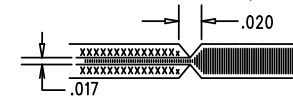
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	2	2ND PROTOTYPE	VLADIMIR O.	06-21-13

LAYER STRUCTURE



NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



<div>UNLESS OTHERWISE SPECIFIED</div> <div>DIMENSIONS ARE IN INCHES</div> <div>TOLERANCES:</div> <div>0.XX" = ±0.01"</div> <div>0.XXX" = ±0.005"</div> <div>INTERPRET DIM AND TOL PER ASME Y14.5M-1994</div> <div>THIRD ANGLE PROJECTION</div> <div></div>	APPROVALS		<div> LINEAR TECHNOLOGY</div> <div>1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.linear.com LTC CONFIDENTIAL- FOR CUSTOMER USE ONLY</div>	
	PCB DES.	KIM T.		
	APP ENG.	VLADIMIR O.		
	TITLE: FABRICATION DRAWING			
	SINGLE IDEAL DIODE AND HOT SWAP CONTROLLER			
SIZE		IC NO.	LTC4229IUF	REV
N/A		DEMO CIRCUIT 2060A		2
SCALE = NONE		FILENAME: DC2060A-2.PCB		SHT 1 OF 1