Power over Ethernet Consortium
Clause # 33 PSE Conformance Test Suite v 1.8 Report

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Report Rev. 2.0

Enclosed are the results from the Clause # 33 PSE Conformance testing performed on:

Device Under Test (DUT):	LTC4259ACGW DC837B
Port Tested:	Port 1
Hardware Version:	Not Available
DUT PHY Chip:	Not Available
Power Chipset:	LTC4259ACGW DC837B

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/CL33_PSE/PSE_Test_Suite_v1.8.pdf

During Clause 33 conformance testing, no issues were uncovered.

Review Completed 10/18/2005

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Testing Completed 10/19/2005

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Result Key

The following table contains possible results and their meanings:

Result	Interpretation
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with Comments	The DUT was observed to exhibit conformant behavior however an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Informative	Results are for informative purposes only and are not judged on a pass of fail basis.
Refer to Comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.
Not Applicable	The DUT does not support the technology required to perform these tests.
Not Available	Due to testing station or time limitations, the tests could not be performed.
Borderline	The observed values of the specified parameters are valid at one extreme, and invalid at the other.
Not Tested	Not tested due to the time constraints of the test period.

Test Setup

Testing Equipment	
Real-time DSO	TEKTRONIX, TDS 3014
Current Probe and Amplifier	TEKTRONIX, TPS305 and TPSA300
Digital Multimeter	HEWLETT-PACKARD, 34401A
Digital Power Supply	AGILENT TECHNOLOGIES, E3641A
UNH-IOL Developed Test Board	PoE Test Board Version 1.0

Basic Testing Configuration

The basic testing configuration is defined in the UNH Interoperability Laboratory PSE Parametric Test Suite v1.8

GROUP 1: PARAMETRIC TESTING

Test # and Label	Part(s)	Result(s)
33.1.1 - Open Circuit Voltage	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the open circuit voltage at the PI of the PSE during detection mode is below the conformance limits. a. The open circuit voltage (V_{oc}) should not exceed 30 Volts.		
Comments on Test Results		
a. Open Circuit Voltage = 15.2 V		

Test # and Label	Part(s)	Result(s)
33.1.2 - Detection Circuit	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify the Thevenin equivalent detection circuit of the PSE detection source. a. The DUT loaded circuit voltage should be less than half the open circuit PI voltage or reject current into $V_{detect+}$. The open circuit voltage should not exceed 30V.		
Comments on Test Results		
a. Open circuit voltage = 15.2 V The DUT was observed to reject current into Vdetect+ port. This is compliant with the Alternative PSE detection source shown in Figure 33-9. Output Impedance was not calculated (not applicable due to diode configuration).		

Test # and Label	Part(s)	Result(s)
33.1.3 - BackDrive Current	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the detection circuit of the PSE can withstand maximum backdrive current over the range of V_{Port}. a. The DUT should not be affected by backdrive current		
Comments on Test Results		
a. The DUT was observed to properly ignore the backdrive current.		

Test # and Label	Part(s)	Result(s)
33.1.4 – Detector Circuit Output Current	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the short circuit output current of the PSE during PD detection is within the conformance limits.

a. The output short circuit current should not exceed 5 mA.

Comments on Test Results

a. The observed short circuit output current was 0.34 mA.

Test # and Label	Part(s)	Result(s)
33.1.5 – Detector Circuit Output Voltage	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify the voltage output of the PSE's detection circuit conforms to the specified limits.

a. The loaded circuit voltage should be between 2.8 and 10V.
b. The voltage difference between any consecutive detection probe voltages should be at least 1V.
c. The slew rate of the probe voltages should be no greater than 0.1V/µs.

Comments on Test Results

a. Probe Voltage1 = 6.82 V
   Probe Voltage2 = 4.04 V
b. Detection probe voltage difference = 2.78 V
c. Maximum slew rate of the probe voltages = 0.07 V/µs

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.6 – PD Detection Timing	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE probes its PI with valid detection pulses and completes an entire detection sequence within the proper time period.

a. The total pulse width of the detection pulse should not be greater than 500ms.
b. The detection probe voltages should have a duration of at least 2 ms.

Comments on Test Results

a. Probe Voltage1 pulse width = 94 ms
   Probe Voltage2 pulse width = 90 ms
b. Duration of the detection probe voltages > 2 ms

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.7 – Turn On Rise Time	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that when the PSE turns on power, the response times of the PSE are within the conformance limits.

a. The measured slew rate should not exceed 3.04V/µs.

Comments on Test Results

a. The observed slew rate was 1.35 V/µs

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.8 – PD Signature Detection Limits	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT will properly detect a PD's Signature impedance.

a. The minimum accepted input resistance should be between 15 kΩ and 19 kΩ.
b. The maximum accepted input resistance should be between 26.5kΩ and 33 kΩ.
c. The DUT must detect a proper signature if the input capacitance is less than 150nF.
d. The DUT must detect an improper signature if the input capacitance is greater than 10µF.

Comments on Test Results

a. 16.4 kΩ ≤ $R_{accept(min)}$ ≤ 16.5 kΩ
b. 29.7 kΩ ≤ $R_{accept(max)}$ ≤ 29.8 kΩ
c. The DUT was observed to accept capacitances less than 150nF.
d. The DUT was observed to reject improper capacitances above 10µF.

Test # and Label	Part(s)	Result(s)
33.1.9 – PD Classification	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that a DUT supporting Classification properly performs PD class detection.

a. During classification the PSE should supply a voltage between 15.5 and 20.5 V.
b. The DUT should accurately classify the PD.
c. The DUT should classify the PD as Class 0 if the current drawn is equal to or greater than 51mA.
d. The DUT should not supply a current greater than 100 mA.

Comments on Test Results

a. V_{Class}= 17.46 V
b. The DUT was observed to accurately classify the PD.
c. The DUT was observed to accurately classify overload currents as Class 0.
d. The DUT was observed to supply a maximum current of 58 mA.

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.10 – Classification Timing	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that a PSE capable of classifying a PD completes classification within the proper time period after successfully completing the detection of a PD.

a. The DUT should complete classification between 10ms and 75ms after PD detection.

Comments on Test Results

a. T_{pdc} = 32ms

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.11 - PD MPS Dropout Current Limits (I_{MIN} measurement)	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that PSE correctly monitors the PD Maintain Power Signature for DC disconnect.

a. The DUT may remove power if the current drawn is between 5 mA and 10 mA ($I_{MIN2\ (max)}$) for 400 ms.
b. The DUT must remove power if the current drawn is less than 5 mA ($I_{MIN1\ (max)}$) for 400 ms.

Comments on Test Results

a. 8.0 mA ≤ $I_{MIN2\ (max)}$ ≤ 8.1 mA
b. The DUT removes power when current draw is less than 5mA.

Test # and Label	Part(s)	Result(s)
33.1.12 – Range of T_{MPDO} Timer	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that PSE correctly monitors the PD Maintain Power Signature

a. *DC disconnect:* 300ms ≤ T_{MPDO} ≤ 400ms
b. *AC disconnect:* 300ms ≤ T_{MPDO} ≤ 400ms

Comments on Test Results

a. *DC disconnect:* 344 ms ≤ T_{MPDO} ≤ 346 ms
b. *AC disconnect:* 330 ms ≤ T_{MPDO} ≤ 333 ms

Test # and Label	Part(s)	Result(s)
33.1.13 – Power Feed Ripple and Noise	**a**	**Informative**
	b	**Informative**
	c	**Informative**
	d	**Informative**

Expected Results and Procedural Comments

Purpose: To verify that the power feeding ripple and noise are within the conformance limits.

The peak-to-peak values of ripple and noise transmitted on the line by the DUT, in both the common mode and pair-to-pair, should not exceed:
a. 0.5 V_{pp} between 0-500 Hz
b. 0.2 V_{pp} between 500 Hz -150 kHz
c. 0.15 V_{pp} between 150-500 kHz
d. 0.1 V_{pp} between 500 kHz-1 MHz

Comments on Test Results

Total Ripple and Noise = 0.014 V_{pp}

Note: This test is currently under development. Individual frequency range information is not currently available.

Test # and Label	Part(s)	Result(s)
33.1.14 – Load Regulation	**a**	**Not Available**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE performs load regulation while supplying power to the PI.

a. Voltage transients should not exceed 3.5 V/µs.
b. The DUT output voltage should be between 44 and 57 V for all values of I_{Port}.

Comments on Test Results

a. This test is currently under development.
b. V_{Port} (max)= 48.3 V
   V_{Port} (min)= 47.3 V

Test # and Label	Part(s)	Result(s)
33.1.15 – Power Turn On Timing	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT supplies power onto the link segment within the acceptable turn on time after it has successfully detected a PD.

a. The DUT should start supplying power within T_{pon} (400ms) after detection.

Comments on Test Results

a. T_{pon} = 265 ms

Test # and Label	Part(s)	Result(s)
33.1.16 – Apply Power	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE applies power on the same pairs as those used for detection after completing a valid detection.

a. The PSE should perform a valid detection sequence before powering the PD.
b. The PSE should supply power on the same pairs as that it performed detection for the PD.

Comments on Test Results

a. The DUT performed a valid detection sequence before supplying power onto the link segment.
b. The DUT applied power on the same pairs as those it detected on.

Test # and Label	Part(s)	Result(s)
33.1.17 – Overload Current Detection Range	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE removes power if the Iport exceeds the specified limits.

a. If the DUT supports classification, then the value of I_{CUT} should be between P_class/44 to 400mA, otherwise I_{CUT} is between15.4/Vport and 400mA (inclusive).
b. The voltage at the PI of the DUT should be between 44 to 57V (inclusive).

Comments on Test Results

a. I_{CUT} = 361 mA
b. V_{Port} (min) = 47.3 V

Test # and Label	Part(s)	Result(s)
33.1.18 – Overload Time Limits	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE removes power if the Iport exceeds I_{CUT} for greater than overload time interval.

a. The overload time limit (T_{ovld}) should be between 50ms and 75ms (inclusive).

Comments on Test Results

a. T_{ovld} = 60 ms

Test # and Label	Part(s)	Result(s)
33.1.19 – Inrush Current	**a**	**PASS**
	b	**Not Available**

Expected Results and Procedural Comments

Purpose To verify that the PSE will start removing power from the PI within T_{LIM} when it detects a short circuit condition.

a. The inrush current at the PI of the DUT should be between 400 to 450mA (inclusive).
b. The inrush current at the PI of the DUT should be at least 60mA.

Comments on Test Results

a. I_{INRUSH} = 430 mA
b. This test is currently under development.

Test # and Label	Part(s)	Result(s)
33.1.20 – Short Circuit Time Limit	**a**	**PASS**

Expected Results and Procedural Comments

Purpose To verify that when the PSE detects a short circuit condition it starts removing power from the PI within T_{LIM} and must be done removing power within the conformant time limit.

a. The short circuit time limit (T_{LIM}) should be between 50ms and 75ms (inclusive).

Comments on Test Results

a. T_{LIM} = 56 ms

Test # and Label	Part(s)	Result(s)
33.1.21 – PD MPS Time for Validity	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE waits for at least the minimum MPS validity time when it monitors the DC MPS component.

a. The DUT should not remove power from a PD that provides a valid DC MPS signature for at least T_{MPS} every T_{MPS}+T_{MPDO}.

Comments on Test Results

a. The DUT was observed to remain powering when a valid DC MPS signature was presented for at least T_{MPS} every T_{MPS}+T_{MPDO}.

Test # and Label	Part(s)	Result(s)
33.1.22 – AC MPS Signal Parameters	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PI probing AC signals fall within the conformance limits.

a. The PI probing AC voltage (V_open) should be between 1.9V to 10% of Vport (V_{pp}).
b. The AC probing signal frequency should not be greater than 500 Hz.
c. The AC probing signal slew rate should not be greater than 0.1V/µs.

Comments on Test Results

a. V_open = 4.4 V
b. AC probing signal frequency= 104 Hz
c. Slew rate =0.0006 V/µs

Test # and Label	Part(s)	Result(s)
33.1.23 – AC Disconnect Detection Voltages	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PI probing AC voltages during AC disconnect detection fall within the conformance limits.

a. The AC ripple voltage (V_{CLOSE}) should be less than 0.5Vpp.
b. The measured V_{Port} (Vp) should not exceed 60V.

Comments on Test Results

a. V_{CLOSE} = 0.014 Vpp
b. Vp= 51.6 V

Test # and Label	Part(s)	Result(s)
33.1.24 – AC MPS Signature	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE that implements AC MPS component correctly monitors the PD Maintain Power Signature.

a. The DUT should supply power to the PD for signature impedance less than 27KΩ.
b. The measured impedance (Z_{ac2}) should be between 27KΩ and 1980KΩ (inclusive).

Comments on Test Results

a. The DUT remained powering for maintain power signatures less than 27kΩ.
b. 290 kΩ ≤ Z_{ac2} ≤ 300 kΩ

Test # and Label	Part(s)	Result(s)
33.1.25 – New Detection Cycle	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that if the PSE is unable to supply power within T_{pon} then, it initiates and successfully completes a new detection cycle before powering on. a. The DUT should complete a full detection cycle before applying power onto the link segment.		
Comments on Test Results		
a. The DUT was observed to successfully complete a new detection cycle before applying power onto the link segment.		

Test # and Label	Part(s)	Result(s)
33.1.26 – Alternative B Backoff Cycle	**a**	**PASS**
	b	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that if a PSE implementing Alternative B fails to detect a valid detection signature at its PI, it will wait for the appropriate period of time before beginning a new detection cycle and applies a voltage on to the PI that falls within the defined limits. a. The DUT should not apply a voltage greater than 2.8 V_{dc} to the PI. b. The value for T_{dbo} should be at least 2 sec.		
Comments on Test Results		
a. The DUT was observed to not apply a voltage greater than 2.8 V_{dc} to the PI. b. The DUT was observed to wait for 2.7 seconds before resuming detection. General Note: The DUT was wired for alternative A during testing of this feature.		

Test # and Label	Part(s)	Result(s)
33.1.27 – PSE Current Unbalance	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the current unbalance between the two conductors of the power pairs of the PSE over the current load range is within the permissible range. a. The current unbalance between the two conductors per power pair should not be greater than 10.5mA.		
Comments on Test Results		
a. The DUT was observed to have a current unbalance less than 6.0 mA for minimum and maximum I_{port}.		

Test # and Label	Part(s)	Result(s)
33.1.28 – Error Delay Timing	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE waits for at least the minimum conformant time before attempting subsequent detection after it removes power due to detection of error condition.

a. The DUT should wait for at least 750ms after detecting a short circuit condition and removing power before resuming detection
b. The DUT should wait for at least 750ms after detecting an overload condition and removing power before resuming detection

Comments on Test Results

a. The DUT was observed to wait 2.2 sec after a short circuit event before resuming signature detection.
b. The DUT was observed to wait 1.6 sec after an overload event before resuming signature detection.

Test # and Label	Part(s)	Result(s)
33.1.29 – Turn Off Time Limits	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE disconnects power within T_{Off} through a test resistor.

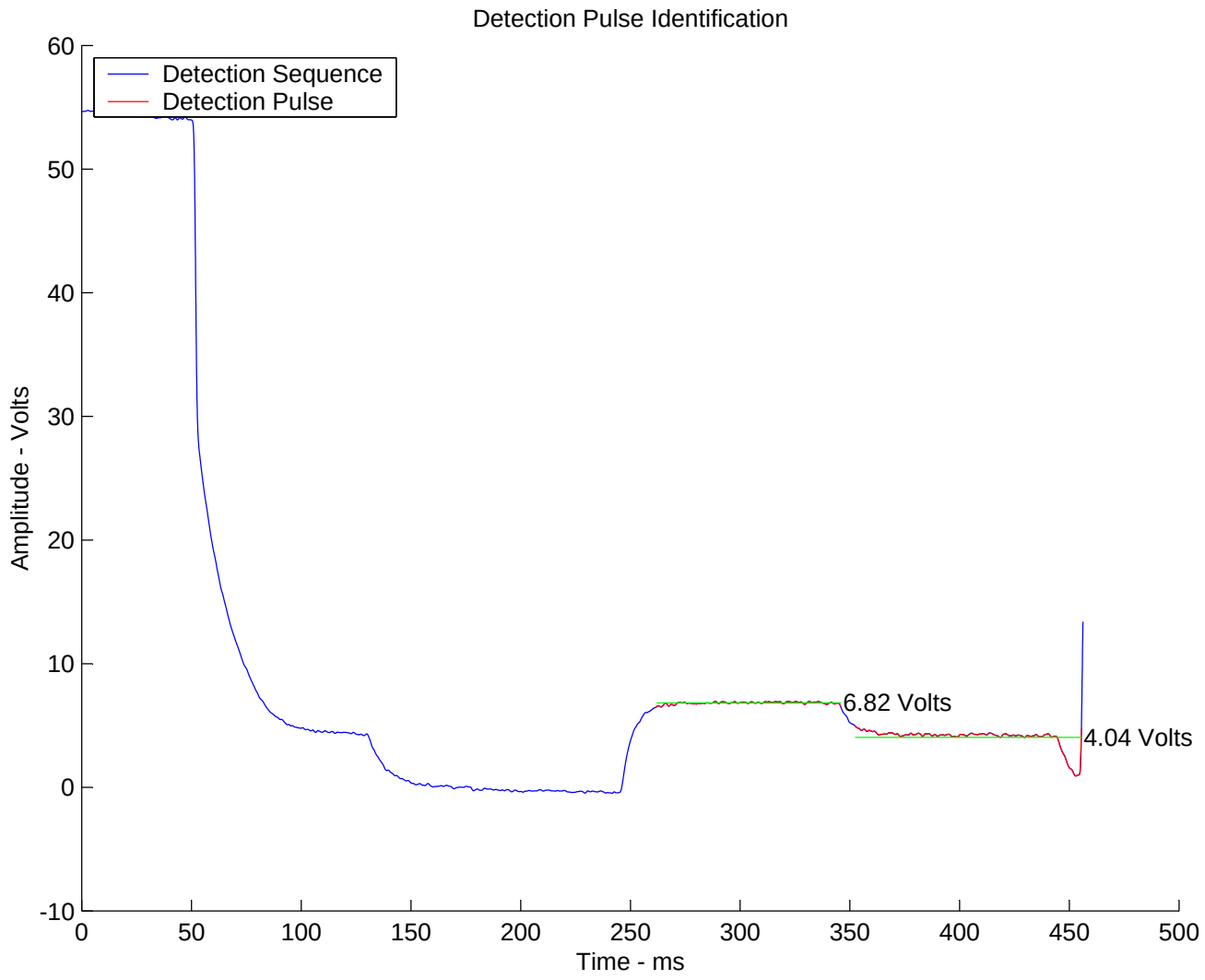
a. The DUT should remove power in times less than 500ms through a test resistor of 320kΩ.

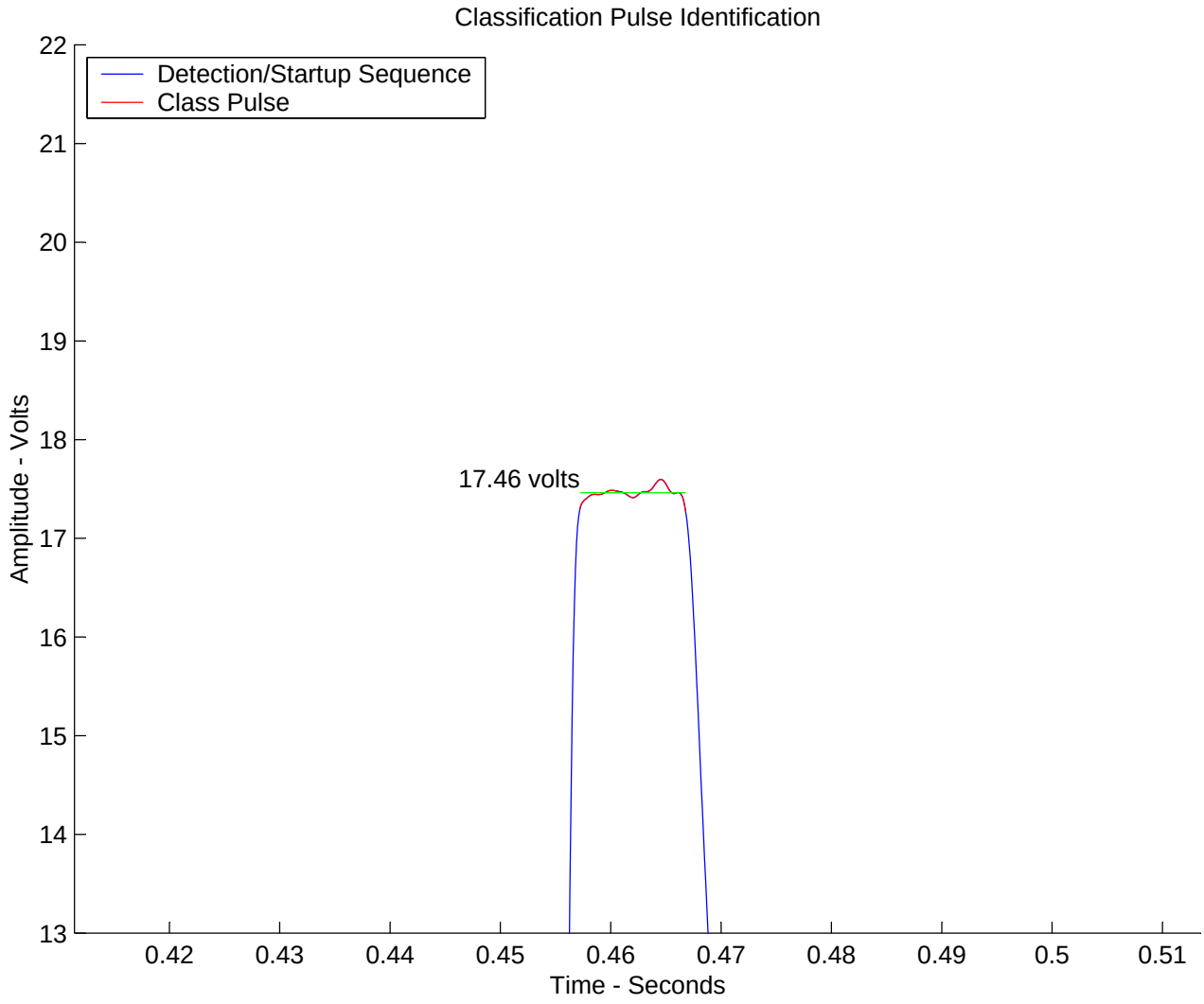
Comments on Test Results

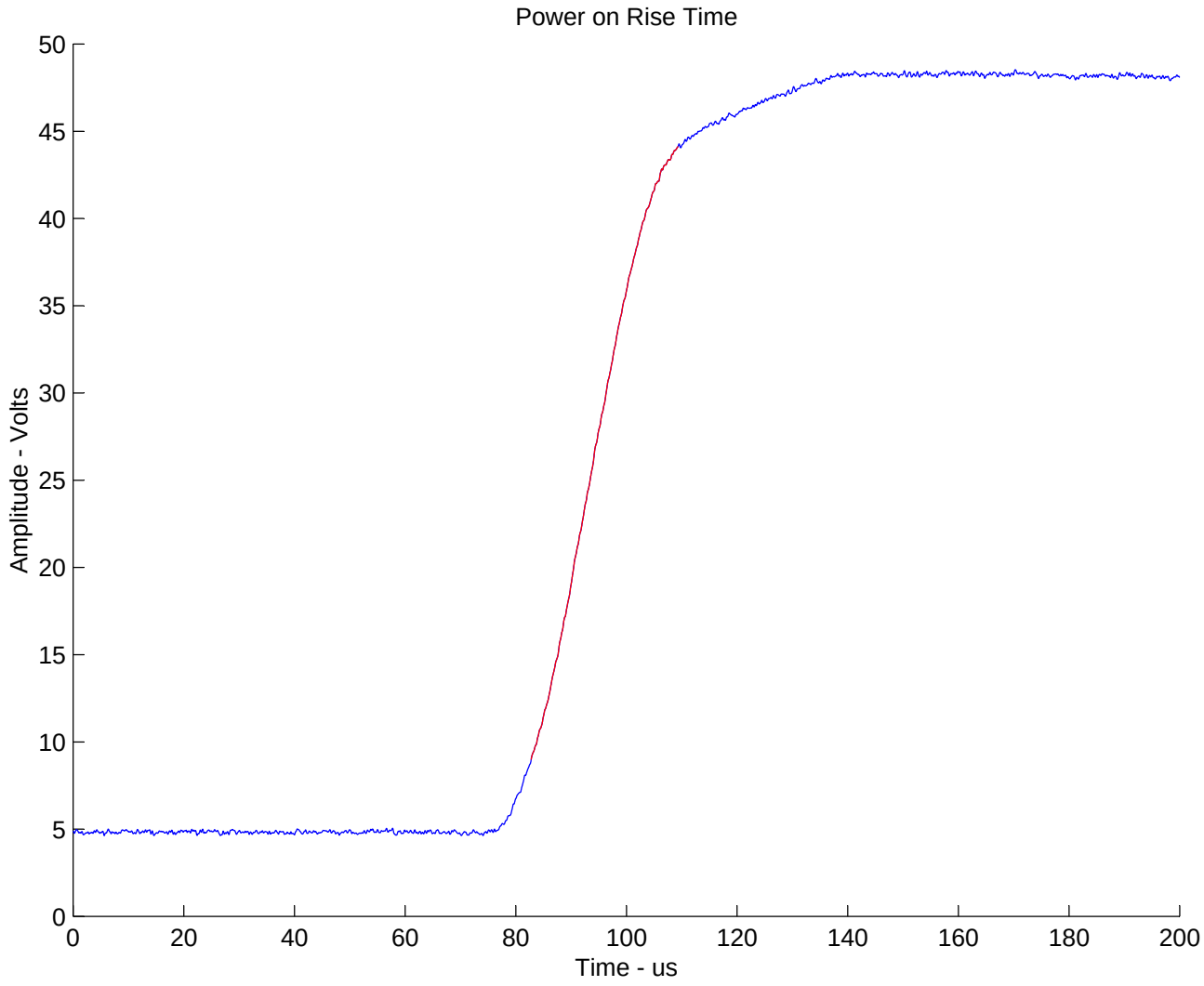
a. The DUT was observed to remove power in less than 426 ms.

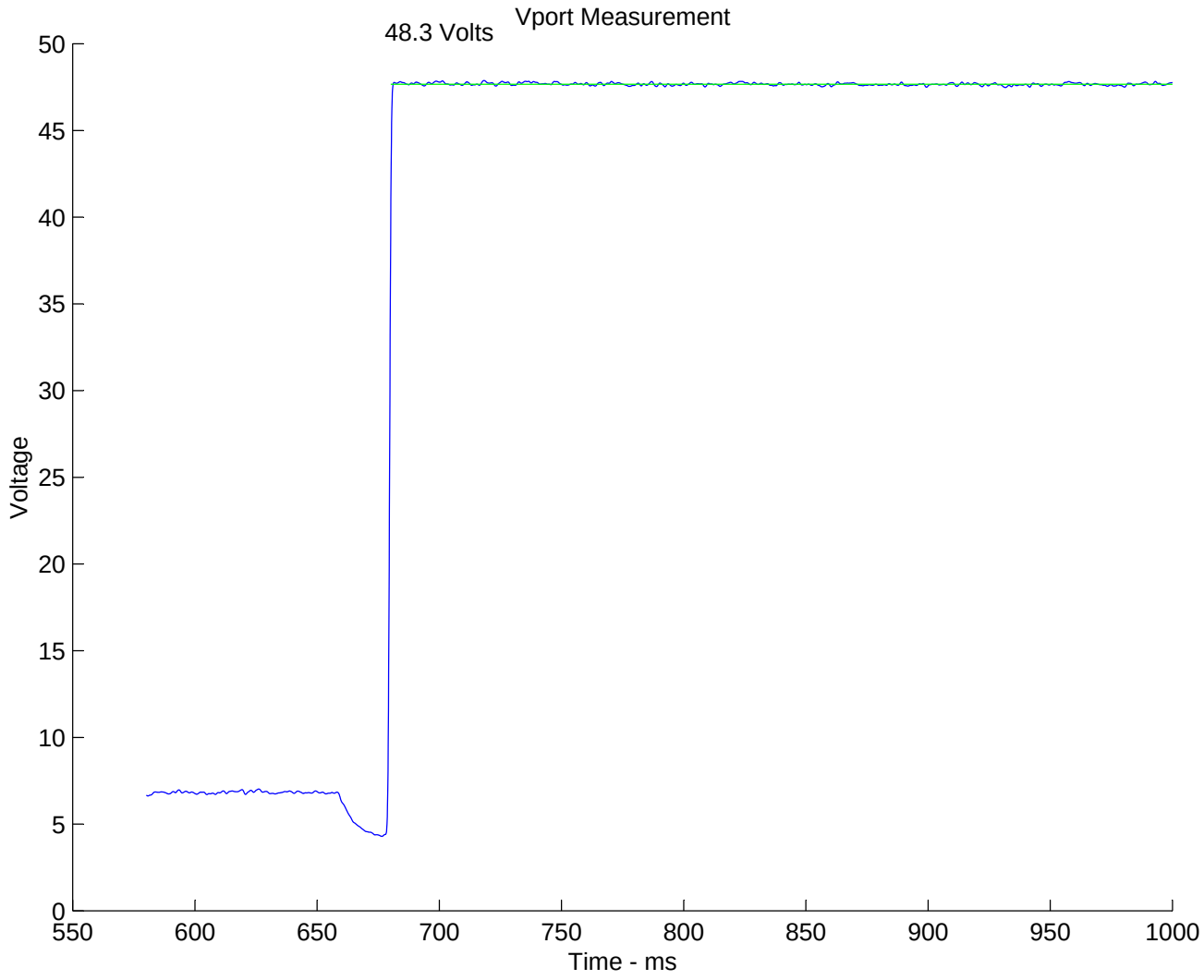
Annex A: Figures

Attached are the figures illustrating the Detection Pulse Sequence, Classification Pulse (Optional), Turn on Rise Time and V_{PORT}. These were captured with the real time DSO and post processed using custom Matlab scripts.


Detection Pulse Identification
Detection Sequence
Detection Pulse
6.82 Volts
4.04 Volts
Amplitude - Volts
Time - ms
60
50
40
30
20
10
0
-10
0
50
100
150
200
250
300
350
400
450
500


Classification Pulse Identification
Detection/Startup Sequence
Class Pulse
17.46 volts
Amplitude - Volts
Time - Seconds
22
21
20
19
18
17
16
15
14
13
0.42
0.43
0.44
0.45
0.46
0.47
0.48
0.49
0.5
0.51


Power on Rise Time
Amplitude - Volts
Time - us
0
5
10
15
20
25
30
35
40
45
50
0
20
40
60
80
100
120
140
160
180
200


Vport Measurement
48.3 Volts
Voltage
Time - ms
0
5
10
15
20
25
30
35
40
45
50
550
600
650
700
750
800
850
900
950
1000