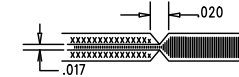


SIZE	QTY	SYM	PLATED	TOL
70	2	+	NO	+/-0.0
15	79	X	YES	+/-0.0
187	4	□	NO	+/-0.0
33	100	◇	YES	+/-0.0
205	2	⊗	YES	+/-0.0
94	16	⊗	YES	+/-0.0
35	72	⊕ ^B	YES	+/-0.0
130	2	⊕ ^C	NO	+/-0.0
35.04	20	⊕ ^D	YES	+/-0.0
62	4	⊕ ^E	YES	+/-0.0
62	2	⊕ ^F	NO	+/-0.0

REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	2	PRODUCTION	DILIAN R.	05-05-11

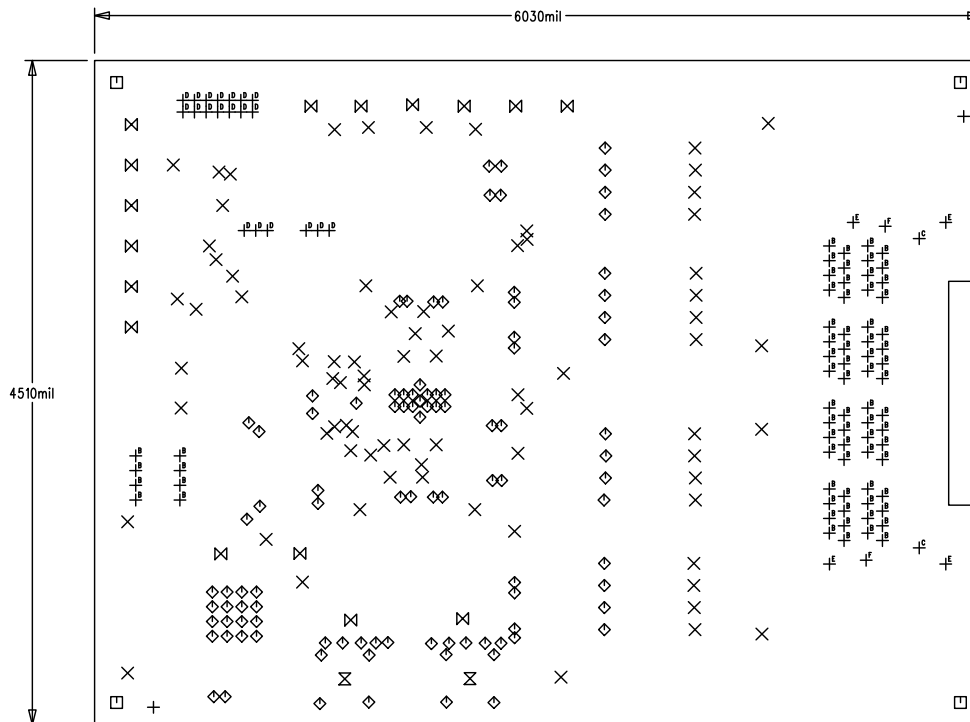
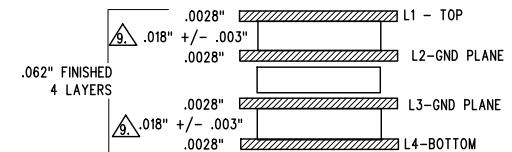
NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -EPOXY FIBERGLASS, NEMA GRADE FR-4
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 2 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



9. CONTROLLED DIELECTRIC FOR LAYERS 1-2 AND LAYERS 3-4

LAYERING STRUCTURE



LAYER 1 : TOP LAYER

DRILL DRAWING LAYER

LINEAR TECHNOLOGY DATE: 05-09-11
DC1815A-2 LTC4266AIUHF
QUAD PORT LTPoE++ PSE CONTROLLER

UNLESS OTHERWISE SPECIFIED		APPROVALS			
DIMENSIONS ARE IN INCHES		PCB DES.	J.K.		
TOLERANCES:		APP ENG.	DILIAN R.	TITLE: FABRICATION DRAWING	
0.XX" = ±0.01"				QUAD PORT LTPoE++ TM PSE CONTROLLER	
0.XXX" = ±0.005"				SIZE N/A	
INTERPRET DIM AND TOL PER ASME Y14.5M-1994				IC NO. LTC4266AIUHF FAMILY	
THIRD ANGLE PROJECTION				DEMO CIRCUIT 1815A	
		SCALE = NONE		FILENAME: DC1815A-2.PCB	SHT 1 OF 1

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