Product Errata

LTC4302-1/LTC4302-2 LTC4305, LTC4306, I²C Filter SDAIN Short Pulse Misprocessing Issue

October 5, 2011

Date Codes for New LTC4302-1/LTC4302-2, LTC4305, LTC4306 Silicon with Fixed Input I²C Filter Circuitry

This note applies to LTC4302-1/LTC4302-2, LTC4305 and LTC4306 units with date codes prior to 1144. Parts with date code 1144 and later have been fixed.

Description of the Issue

Short pulses on the SDAIN pin of the LTC®4302-1/LTC4302-2, LTC4305, LTC4306 may cause the I²C interface of the LTC4302-1/LTC4302-2, LTC4305, LTC4306 to misprocess I²C commands it receives. These SDA short pulses occur during the SCL low period immediately preceding or immediately following an Acknowledge Bit, depending upon the relative hold times of the LTC4302-1/ LTC4302-2, LTC4305, LTC4306 and the I²C master. For a typical unit, the pulse width causing the errors is 240ns ±3ns. Manufacturing process variations cause the mean value of the pulse width to vary from 150ns to 340ns from unit to unit, but for any single unit, the time window in which the problem occurs is very narrow, approximately ±3ns.

The misprocessed SDAIN logic states may result in the LTC4302-1/LTC4302-2, LTC4305, LTC4306 failing to write its registers correctly when commanded to do so by the I²C master. Figures 1 and 2 and the following text illustrate the problem using the LTC4306. The same SCLIN and SDAIN waveforms shown in the figures can cause similar problems in the LTC4302-1/LTC4302-2 and LTC4305. Figure 1 shows a successful write operation to connect the input SDAIN, SCLIN bus to downstream channel 4. The SDAIN short pulse is 500ns wide—wider than the maximum 340ns pulse width that can ever cause a misprocessing issue. SDAIN short pulses narrower than 150ns also never cause an issue.

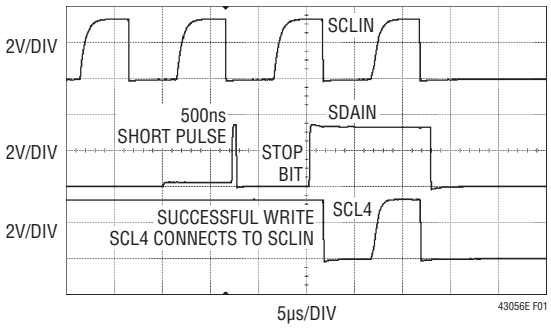

Figure 1. A 500ns Wide Logic High Short Pulse on SDAIN Causes No Issues with the LTC4306. After the Stop Bit, Which Completes the Command to Connect to Channel 4, SCL4 Follows SCLIN as It Should

Figure 2 shows a failed write operation to connect to downstream channel 4, where SCL4 remains high after the Stop Bit. The SDAIN short pulse width that caused the problem for this particular unit was 240ns. Pulse widths narrower than 237ns and wider than 243ns resulted in successful write operations.

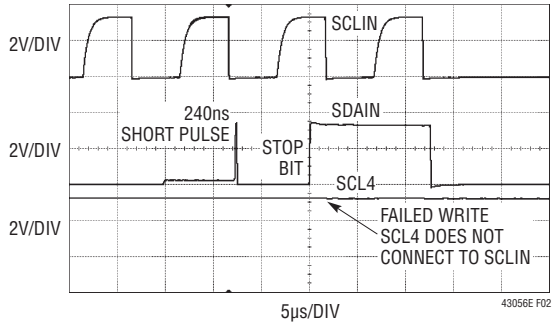

Figure 2. A 240ns Wide Logic High Short Pulse on SDAIN Causes a Failed Write Operation to Occur with the LTC4306. After the Stop Bit, Which Completes the Command to Connect to Channel 4, SCL4 Fails to Connect to SCLIN and Remains High. For the Unit Under Test, if the Short Pulse Width Is Narrowed to Less Than 237ns or Widened to Greater Than 243ns, the Write Operation Is Successful

Because the ±3ns window causing the problem is so small, random variations in the system over time can cause the problem to be intermittent. For this reason, a Write Operation to a single LTC4302-1/ LTC4302-2, LTC4305, LTC4306 may fail sometimes but pass at other times. The best way

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to fix this issue is to ensure that the SDAIN short pulse never occurs. Adding capacitance to SDAIN to prevent the short pulse from rising above 1V is a good solution. This and other solutions are discussed in the next section.

Possible Workarounds

Linear Technology Corporation recommends the following fixes in applications where the problem occurs:

- Observe the SDAIN short pulses before and after the 9th clock of each byte when the master is communicating with the LTC4302-1/LTC4302-2, LTC4305, LTC4306. Add capacitance to the SDAIN line to prevent SDAIN from ever rising above 1V during a short pulse. Adding the same capacitance to SCLIN is also recommended to optimize timing on the I^2C bus.
- For new mux designs not requiring pin compatibility with the LTC4305, LTC4306 and not requiring channel selectability by I^2C software, users may choose the LTC4312 and LTC4314 2-Channel and 4-Channel Pin Selectable I^2C Muxes with Bus Buffers. Channel selection is done out-of-band via ENABLE channel select pins. The LTC4312 and LTC4314 do not contain I^2C interface circuitry and therefore do not have any issues with SDAIN short pulses.
- For new single bus buffer designs not requiring pin compatibility with the LTC4302-1/LTC4302-2 and not requiring control by I^2C software, users may choose the LTC4300A-1, LTC4303 or LTC4307 I^2C bus buffers. These buffers do not contain I^2C interface circuitry and therefore do not have any issues with SDAIN short pulses.
- For a given unit, the time window in which the problem occurs is quite narrow – on the order of a few nanoseconds. Due to the narrow time window coupled with random cycle-to-cycle variations, a write operation that fails on the first attempt will often succeed on subsequent attempts. While less than optimal and not guaranteed to work in all cases, adding a software loop to write a register, read back the register contents to confirm the new data, and retry the write if the previous write failed, often fixes the problem.

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