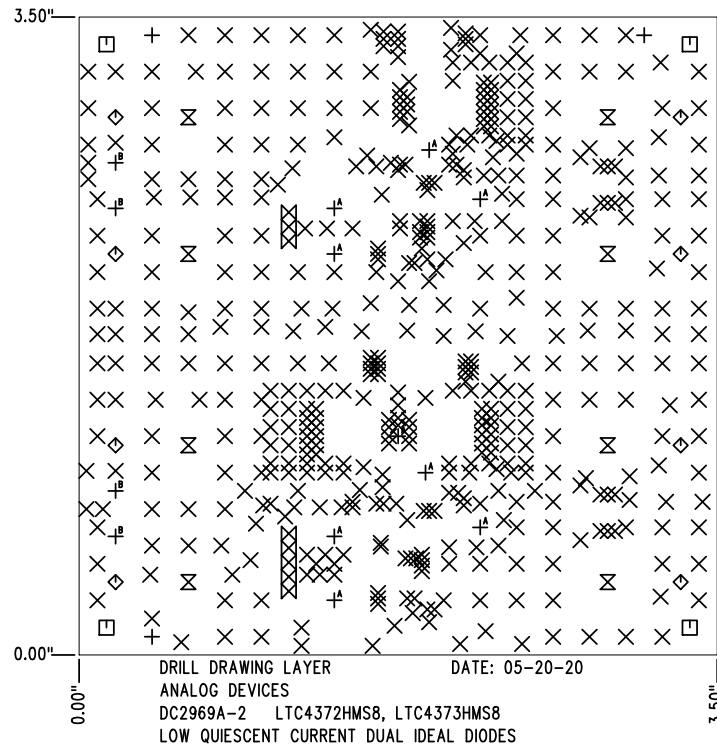


SHOWN FROM TOP SIDE

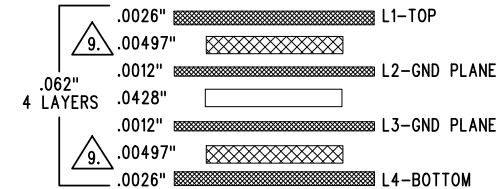


SIZE	QTY	SYM	PLATED	TOL
0.07	3	+	NO	+/-0.003"
0.012	504	X	YES	+/-0.003"
0.187	4	□	NO	+/-0.003"
0.094	8	◇	YES	+/-0.003"
0.207	8	⊗	YES	+/-0.003"
0.035	8	⊗	YES	+/-0.003"
0.025	9	+	YES	+/-0.003"
0.064	4	+	YES	+/-0.003"

REVISION HISTORY

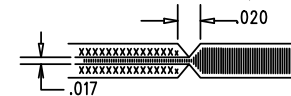
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	2	2ND PROTOTYPE	PINKESH S.	05-20-20

LAYER STRUCTURE



NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



9. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT ADI.

<p>UNLESS OTHERWISE SPECIFIED</p> <p>DIMENSIONS ARE IN INCHES</p> <p>TOLERANCES:</p> <p>0.XX" = ±0.01"</p> <p>0.XXX" = ±0.005"</p> <p>INTERPRET DIM AND TOL PER ASME Y14.5M-1994</p> <p>THIRD ANGLE PROJECTION</p>	APPROVALS		<p>ANALOG DEVICES POWER BY LINEAR</p> <p>2555 AUGUSTINE DRIVE SANTA CLARA, CA 95054 www.analog.com</p>
	PCB DES.	KIM T.	
	APP ENG.	PINKESH S.	
	TITLE: FABRICATION DRAWING		<p>LOW QUIESCENT CURRENT DUAL IDEAL DIODES</p>
	SIZE	IC NO. LTC4372HMS8, LTC4373HMS8	
	N/A	DEMO CIRCUIT 2969A	
SCALE = NONE	FILENAME:	DC2969A-2.PCB	SHT 1 OF 1