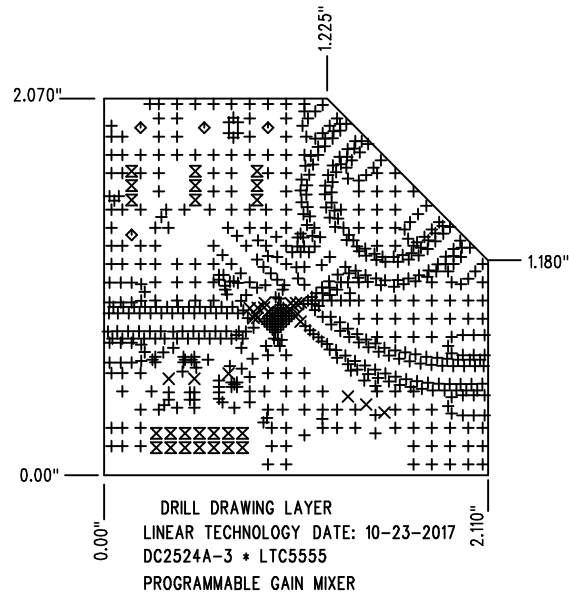
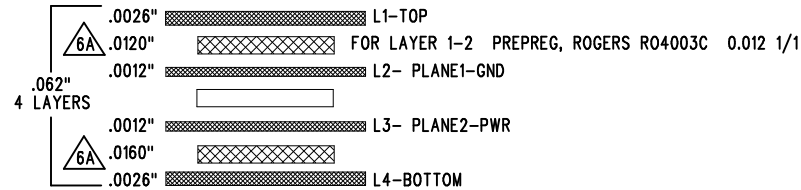


## LAYER STRUCTURE



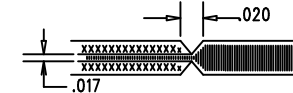
SIZE	QTY	SYM	PLATED	TOL
0.006	645	+	YES	+/-0.003
0.004	21	X	YES	+/-0.003
0.066	4	◇	YES	+/-0.003
0.035	23	⊗	YES	+/-0.003

## NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: FOR LAYER 1-2 PREPREG, ROGERS R04003C  
FOR LAYER 2-3-4 - ISOLA FR-370HR OR EQUIVALENT  
-FINISHED THICKNESS TO BE 0.062" +/- .005"  
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.  
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.  
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.  
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.  
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.  
-GOLD IMMERSION BOTH SIDES.  
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- CONTROLLED 50 OHM +/-5% IMPEDANCE FOR LAYER 1-2  
TRACE WIDTH 23.5 MILS, GAP 20 MILS

6A SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.  
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- PERFORM SCORING PER ITEM "A".



10. LTC DESIGNED IMPEDANCE TEST COUPON REQUIRED!

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: 0.XX" = ±0.01" 0.XXX" = ±0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION	APPROVALS		<b>LINEAR TECHNOLOGY</b> 1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.linear.com LTC CONFIDENTIAL - FOR CUSTOMER USE ONLY	
	PCB DES.	AK		TITLE: FABRICATION DRAWING <b>PROGRAMMABLE GAIN MIXER</b>
	APP ENG.	WESTON S.		
	SCALE = NONE	SIZE N/A IC NO. LTC5555UFD <b>DEMO CIRCUIT 2524A</b>	REV 3 FILENAME: DC2524A-3 SHT 1 OF 1	