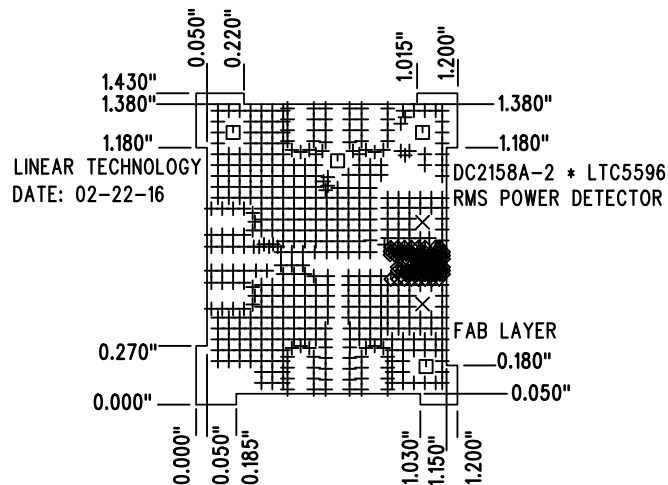
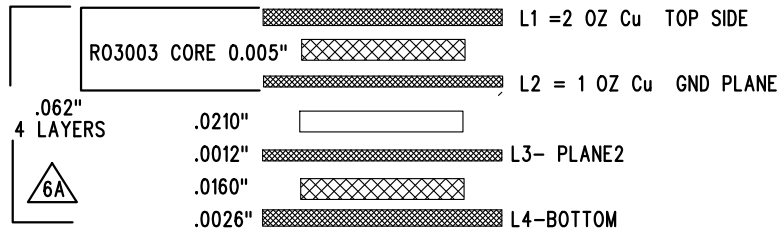


## LAYER STRUCTURE



SIZE	QTY	SYM	PLATED	TOL
0.006	449	+	YES	+/-0.003
0.082	2	X	YES	+/-0.003
0.066	4	□	YES	+/-0.003
0.004	90	◇	YES	+/-0.003

REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	2	2ND PROTO	ANDY M.	02-22-16

### NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.

### BETWEEN LAYER 1 AND 2 R03003 SERIES ROGERS PREPREG 5mills

- FINISHED THICKNESS TO BE 0.062" +/- .005"
- TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
- FLAMMABILITY RATING: 94 V-0 MINIMUM.

- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN. 0.00" ARE PRIMARY DATUMS.

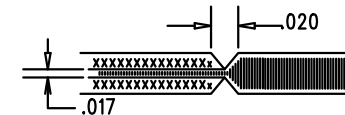
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.  
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.  
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER

- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.  
-GOLD IMMERSION BOTH SIDES.  
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.

- CONTROLLED 50 OHM +/-5% IMPEDANCE FOR LAYER 1-2 TRACE WIDTH 10 MILS IN A COPLANAR WAVEGUIDE STRUCTURE.

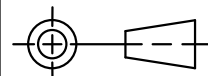
6A SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING



### UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES  
TOLERANCES:  
0.XX" = ±0.01"  
0.XXX" = ±0.005"  
INTERPRET DIM AND TOL  
PER ASME Y14.5M-1994  
THIRD ANGLE PROJECTION



### APPROVALS

PCB DES. AK  
APP ENG. ANDY M.

SCALE = NONE

**LINEAR TECHNOLOGY**

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FOR CUSTOMER USE ONLY

TITLE: FABRICATION DRAWING

RMS POWER DETECTOR

SIZE N/A IC NO. LTC5596  
DEMO CIRCUIT 2158A REV 2

FILENAME: DC2158A-2.PCB

SHT 1 OF 1