PCA SCH, MOTHERBOARD, CAMANCHE, MOTE VERSION

Content:

1. Title Page
2. Eterna
3. Memory
4. Connectors, LED & Power

Notes:

1. Associcated Documents

BOM
700-0216-0101 REV2

ASY DWG
705-0216-0001 REV1

PCB FAB
600-0216-0001 REV1

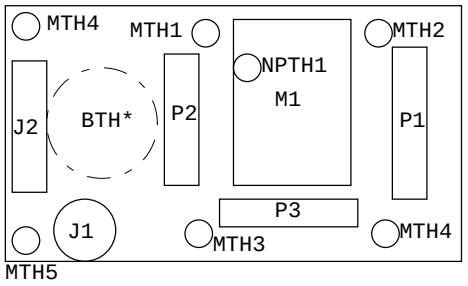
2. Assembly Options

1. External Memory or not
2. Russian or Canadian or uModule Oski based
3. PA_EXT_SET R value

Revision History:

Rev	Description	ECO	Author
01	Initial release	1212	Ric Peregrino
02	Change R6 to 0 ohm, FLASH_P_ENn no mem Load PB1, not PB2, adjust M1 PN	1262	Ric Peregrino

Parts placement, not to scale



LINEAR TECHNOLOGY

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CUSTOMER NOTICE

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.

THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND IS SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

CONTRACT NO.

APPROVALS

DRAWN:

CHECKED:

APPROVED:

ENGINEER:

DESIGNER:

dust networks™ A Linear Technology Company

1630 McCarthy Blvd. Milpitas, CA 95035

Phone: (408)432-1900 Fax: (408)434-0507

TITLE: DC9018A-B

PCA SCH, MOTHERBOARD, CAMANCHE

SIZE B

DWG NO. 710-0216-0101

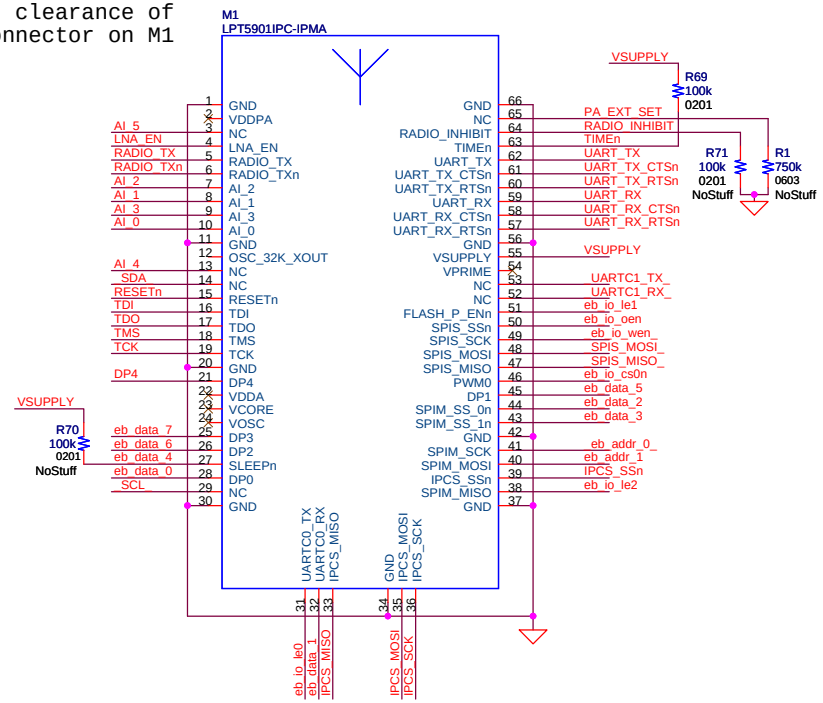
REV 02

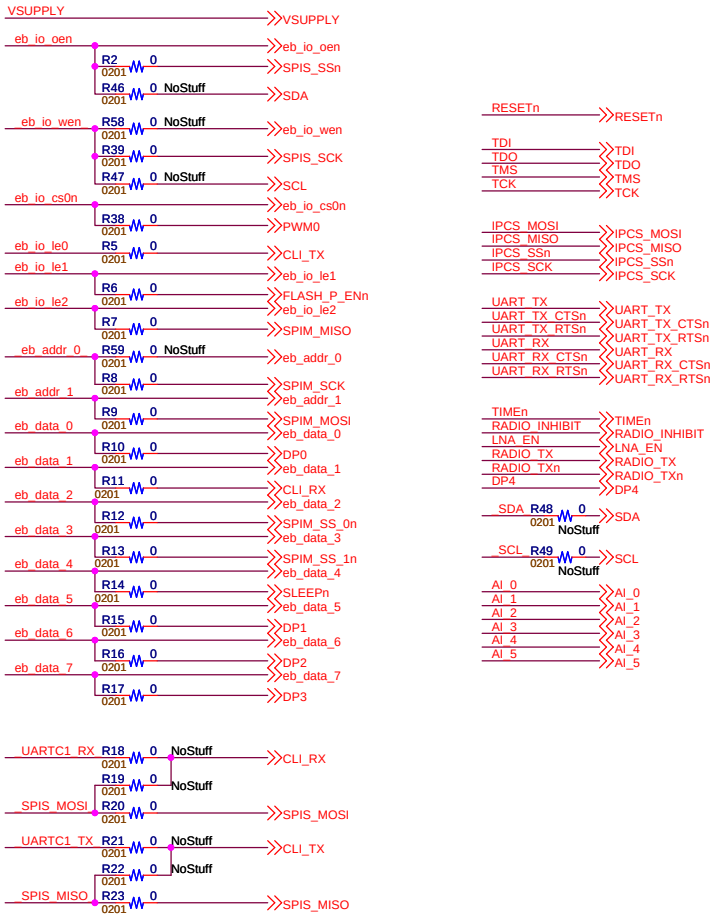
DATE: Friday, June 14, 2013

SHEET 1 OF 4

Place all R's on this page
as close as possible to M1

NPTH1, for clearance of
antenna connector on M1





LINEAR TECHNOLOGY

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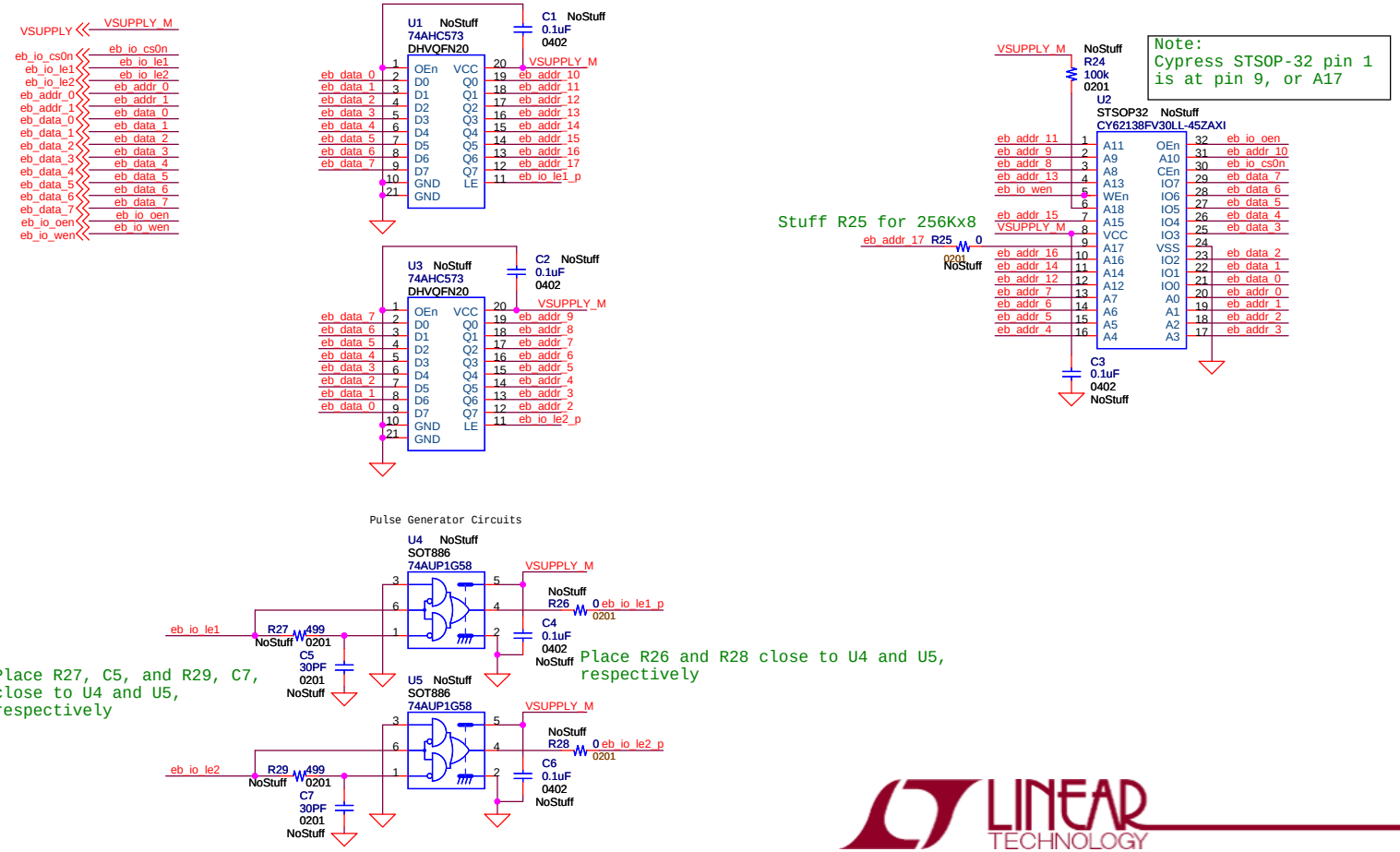
25 mil traces for VSUPPLY_M



A

A

Pulse Generator Circuits

Place R27, C5, and R29, C7, close to U4 and U5, respectively

Place R26 and R28 close to U4 and U5, respectively

LINEAR TECHNOLOGY

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PCA SCH, MOTHERBOARD, CAMANCHE

SIZE	DWG NO.	REV
B	710-0216-0101	02

DATE: Tuesday, May 14, 2013 SHEET 3 OF 4

CONNECTORS, VISUAL INDICATORS, POWER

P1 100MIL_RA 250-0406 HDR16X2PTH100RARP
P2 100MIL HDR12X2PTH100RP
P3 100MIL HDR7X2PTH100RP
REVERSE PINOUT FOOTPRINT
KEY

(*) (3x) ANNOTATE TOP SILK WITH SIGNAL NAMES (SEE SEPARATE INSTRUCTIONS FOR DETAILS)

(*) (3x) PLACE HEADERS ON BOTTOM (SEE SEPARATE INSTRUCTIONS FOR DETAILS)

(#) ANNOTATE SILK WITH : "AI_0", "AI_1", "AI_2", "AI_3", "AI_4", and "AI_5" as shown

(+++) ANNOTATE SILK WITH NOTE SHOWING ON/OFF:
JP4 3 2 1
1-2 |ON |
2-3 |OFF|

(+++) ANNOTATE SILK WITH: "LED ENABLE", "EHORBAT", "I/O 1" & "I/O 2" RESP.

(**) SPLIT LED PAIRS AND PLACE ONE ON TOP AND ONE ON BOTTOM OF PCB.

(**) ANNOTATE SILK ON BOTH TOP AND BOTTOM WITH: "STATUS 0", "STATUS 1" & "INDICATOR 0".

(++) ANNOTATE WITH: "POWER" NEAR SWITCH "; AND "ON" NEAR PIN1 & "OFF" NEAR PIN 3

(+) ANNOTATE SILK WITH : "MOTE RESET"

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