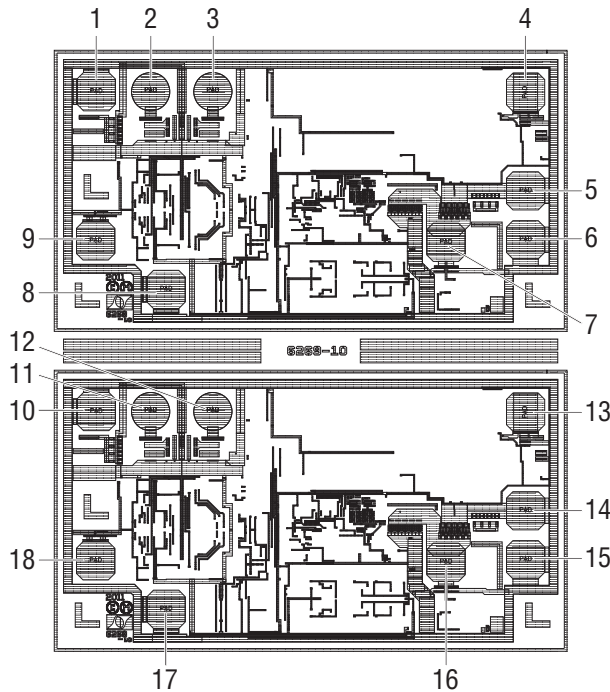


LTC6269-10

4GHz Ultra-Low Bias Current FET Input Op Amp


PAD FUNCTION

- | | |
|---------------------|----------------------|
| 1. V ⁻ A | 10. V ⁻ B |
| 2. +INA | 11. +INB |
| 3. -INA | 12. -INB |
| 4. SHDNA | 13. SHDNB |
| 5. V ⁺ A | 14. V ⁺ B |
| 6. V ⁺ A | 15. V ⁺ B |
| 7. OUTA | 16. OUTB |
| 8. V ⁻ A | 17. V ⁻ B |
| 9. SHDNA | 18. SHDNB |

50mils × 58mils,
 28mils thick.
 Backside metal: None
 Backside potential: V⁻

DIE CROSS REFERENCE

LTC® Finished Part Number	Order Part Number
LTC®6269-10	LTC6269-10 DICE/DWF

Please refer to LTC standard product data sheet for other applicable product information.
 *DWF = DICE in wafer form.

Pins 1 and 8 are connected internally
 Pins 5 and 6 are connected internally
 Pins 4 and 9 are connected internally
 Pins 10 and 17 are connected internally
 Pins 14 and 15 are connected internally
 Pins 13 and 18 are connected internally

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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage V ⁺ to V ⁻	5.5V	Input Current (SHDN)	±1mA
Input Voltage	V ⁻ - 0.2V to V ⁺ + 0.2V	Output Current (I _{OUT}) (Notes 4, 5)	135mA
Input Current (+IN, -IN) (Note 2)	±1mA		

DICE/DWF ELECTRICAL TEST LIMITS

Specifications are at T_A = 25°C, V_{SUPPLY} = 5.0V (V⁺ = 5V, V⁻ = 0V, V_{CM} = mid-supply), R_L = 1kΩ, V_{SHDN} is unconnected.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V _{OS}	Input Offset Voltage	V _{CM} = 2.75V	-0.7	0.7	mV
		V _{CM} = 4.0V	-1.0	1.0	mV
I _B	Input Bias Current (Notes 3, 4)	V _{CM} = 2.75V	-20	20	fA
		V _{CM} = 4.0V	-20	20	fA
I _{OS}	Input Offset Current (Notes 3, 4)	V _{CM} = 2.75V	-40	40	fA
CMRR	Common Mode Rejection Ratio	V _{CM} = 0.5V to 3.2V (PNP Side)	72		dB
		V _{CM} = -0.1V to 4.5V	64		dB
IVR	Input Voltage Range	Guaranteed by CMRR	-0.1	4.5	V
PSRR	Power Supply Rejection Ratio	V _{CM} = 1.0V, V _{SUPPLY} Ranges from 3.1V to 5.25V	78		dB
			Supply Voltage Range	3.1	5.25

DICE/DWF SPECIFICATION

LTC6269-10

DICE/DWF ELECTRICAL TEST LIMITS

Specifications are at $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = 5.0\text{V}$ ($V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = \text{mid-supply}$), $R_L = 1\text{k}\Omega$, V_{SHDN} is unconnected.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS	
A_V	Open Loop Voltage Gain	$V_{\text{OUT}} = 0.5\text{V to } 4.5\text{V}$	$R_{\text{LOAD}} = 10\text{k}$	125		V/mV
			$R_{\text{LOAD}} = 100$	10		V/mV
I_{SC}	Output Short Circuit Current (Note 5)		60		mA	
I_S	Supply Current Per Amplifier		15	18	mA	
	Supply Current in Shutdown (Per Amplifier)			0.85	mA	
I_{SHDN}	Shutdown Pin Current	$V_{\text{SHDN}} = 0.75\text{V}$	-12	12	μA	
		$V_{\text{SHDN}} = 1.50\text{V}$	-12	12	μA	
V_{IL}	SHDN Input Low Voltage	Disable		0.75	V	
V_{IH}	SHDN Input High Voltage	Enable. If SHDN is Unconnected, Amp is Enabled	1.5		V	
I_{LEAK}	Output Leakage Current in Shutdown	$V_{\text{SHDN}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$		400	nA	
		$V_{\text{SHDN}} = 0\text{V}$, $V_{\text{OUT}} = 5\text{V}$		400	nA	

DICE/DWF ELECTRICAL TEST LIMITS

Specifications are at $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = 3.3\text{V}$ ($V^+ = 3.3\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = \text{mid-supply}$), $R_L = 1\text{k}\Omega$, V_{SHDN} is unconnected.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS	
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = 1.0\text{V}$	-0.7	0.7	mV	
		$V_{\text{CM}} = 2.3\text{V}$	-1.0	1.0	mV	
I_B	Input Bias Current (Notes 3, 4)	$V_{\text{CM}} = 1.0\text{V}$	-20	20	fA	
		$V_{\text{CM}} = 2.3\text{V}$	-20	20	fA	
I_{OS}	Input Offset Current (Notes 3, 4)	$V_{\text{CM}} = 1.0\text{V}$	-40	40	fA	
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = 0.5\text{V to } 1.2\text{V}$ (PNP Side)	63		dB	
		$V_{\text{CM}} = -0.1\text{V to } 2.8\text{V}$ (Full Range)	60		dB	
IVR	Input Voltage Range	Guaranteed by CMRR	-0.1	2.8	V	
A_V	Open Loop Voltage Gain	$V_{\text{OUT}} = 0.5\text{V to } 2.8\text{V}$	$R_{\text{LOAD}} = 10\text{k}$	80		V/mV
			$R_{\text{LOAD}} = 100$	10		V/mV
I_{SC}	Output Short Circuit Current (Note 5)		50		mA	
I_S	Supply Current per Amplifier		14.5	17.5	mA	
	Supply Current in Shutdown (Per Amplifier)			0.6	mA	
I_{SHDN}	Shutdown Pin Current	$V_{\text{SHDN}} = 0.75\text{V}$	-12	12	μA	
		$V_{\text{SHDN}} = 1.5\text{V}$	-12	12	μA	
V_{IL}	SHDN Input Low Voltage	Disable		0.75	V	
V_{IH}	SHDN Input High Voltage	Enable. If SHDN is Unconnected, Amp Is Enabled	1.5		V	

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by two series connected ESD protection diodes to each power supply. The input current should be limited to less than 1mA. The input voltage should not exceed 200mV beyond the power supply.

Note 3: The input bias current is the average of the currents into the positive and negative input pins.

Note 4: This parameter is specified by design and/or characterization and is not tested in production.

Note 5: The LTC6269-10 is capable of producing peak output currents in excess of 135mA. Current density limitations within the IC require the continuous current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 135mA (Absolute Maximum).

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 16-33-626910