LTC6431-15
50Ω Gain Block IF Amplifier

DESCRIPTION

Demonstration circuit 1774A-C features the LTC®6431-15 gain block amplifier. The LTC6431-15 has a power gain of 15.5dB and it is part of the LTC643X-YY amplifier series.

DC1774A-C is part of the DC1774A demo boards family supporting the LTC643X-YY family. The demo board DC1774A-C is optimized for a frequency range from 100MHz to 1200MHz. It incorporates a minimum of passive support components to configure the amplifier for various applications. The LTC6431-15 provides 50Ω single-ended input and output impedance so that it can be easily evaluated with most RF test equipment.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, V_{CC} = 5V

SYMBOL	PARAMETER	CONDITIONS	VALUE/UNIT
Power Supply			
V_{CC}	Operating Supply Range	All V_{CC} Pins Plus +OUT	4.75V to 5.25V
I_{CC}	Current Consumption	Total Current	90mA

FREQUENCY (MHz)	POWER GAIN S21 (dB)	OUTPUT THIRD-ORDER INTERCEPT POINT [1] OIP3 (dBm)	OUTPUT THIRD-ORDER INTERMODULATION [1] OIM3 (dBc)	SECOND HARMONIC DISTORTION [2] HD2 (dBc)	THIRD HARMONIC DISTORTION [2] HD3 (dBc)	OUTPUT 1dB COMPRESSION POINT P1dB (dBm)	NOISE FIGURE [3] NF (dB)
100	15.1	46.6	–89.2	–58.0	–88.0	20.0	3.8
200	15.4	46.7	–89.5	–58.0	–88.0	20.0	3.5
240	15.6	46.7	–89.3	–59.0	–88.0	20.3	3.4
300	15.5	46.6	–89.3	–60.0	–86.0	20.1	3.5
400	15.5	46.1	–88.3	–57.0	–87.0	20.3	3.5
500	15.4	45.3	–86.6	–55.6	–77.0	20.3	3.6
600	15.3	43.5	–83.1	–53.6	–69.0	20.4	3.7
700	15.2	42.2	–80.4	–51.9	–69.0	20.2	3.8
800	15.0	41.1	–78.1	–49.2	–65.0	20.1	4.0
900	14.8	39.5	–74.9	–46.7	–63.0	19.7	4.2
1000	14.7	38.7	–73.3	–45.0	–59	19.3	4.2
1100	14.5	38.0	–71.9	–40.8	–56.8	18.8	4.4
1200	14.3	38.0	–71.9	–38.4	–54.2	18.6	4.6

Notes: All figures are referenced to J7 (Input Port) and J10 (Output Port).

1. Two-tone test condition: Output power level = +2dBm/tone; Tone spacing = 1MHz.
2. Single-tone test condition: Output power level = +6dBm.
3. Small signal noise figure.

QUICK START PROCEDURE

Demo circuit 1774A-C can be set up to evaluate the performance of the LTC6431-15. Refer to Figures 7 and 8, for proper equipment connections and follow the procedure below:

Single-Tone Measurement:

Connect all test equipment as suggested in Figure 7

1. The power labels of +5V and GND directly correspond to the power supply. Typical current consumption of the LTC6431-15 is about 90mA.
2. Apply an input signal to J7. A low-distortion, low noise signal source with an external high order lowpass filter will yield the best performance. (i.e. the input signal is –10dBm. The Input is impedance matched to 50Ω).
3. Observe the output via J10. (The measured power at the analyzer should be about +5dBm. The output is impedance matched to 50Ω), suitable for the input of a network or spectrum analyzer.

Two-Tone Measurement:

Connect all test equipment as suggested in Figure 8.

1. The power labels of +5V and GND directly correspond to the power supply. Typical current consumption of the LTC6431-15 is about 90mA.
2. Apply two independent signals f1 and f2 from SG1 and SG2 at 240MHz and 241MHz respectively.
3. Monitor the output tone level on the spectrum analyzer. Adjust signal generator levels such that output power measures +2dBm/tone at the amplifier output J10, after correcting for external cable losses and attenuators.
4. Change the spectrum analyzer's center frequency and observe the two IM3 tones at 1MHz below and above the input frequencies. (i.e. the frequencies of IM3_LOW and IM3_HIGH are 239MHz and 242MHz, respectively. The measurement levels should be approximately –90dBc; +47dBm is a typical performance of OIP3 at 240MHz). For this setup, the Rohde and Schwarz FSEM30 spectrum analyzer was used. This SA has a typical +20dBm third-order intercept point (TOI). So, the SA input attenuation is set to 20dB with an external 20dB attenuation pad, resulting in an attenuation total of 40dB. The system as described can measure OIP3 up to +50dBm.

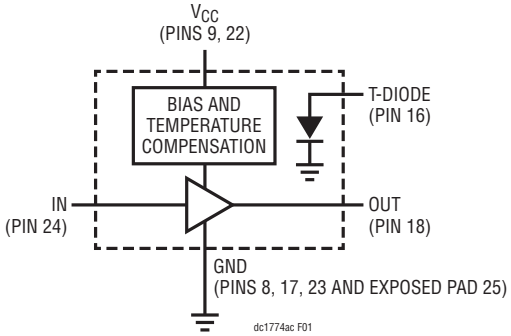


Figure 1. LTC6431-15 Device Block Diagram

QUICK START PROCEDURE

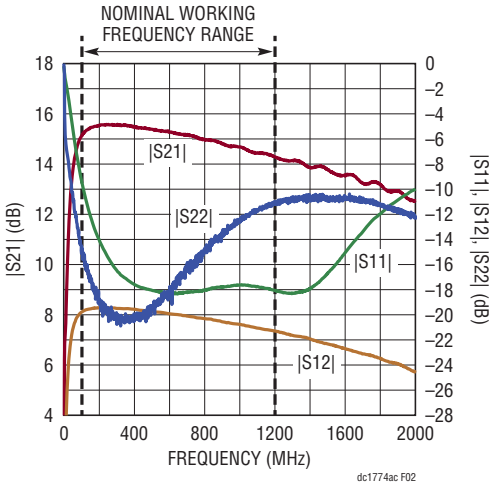


Figure 2. Demo Board S-Parameters

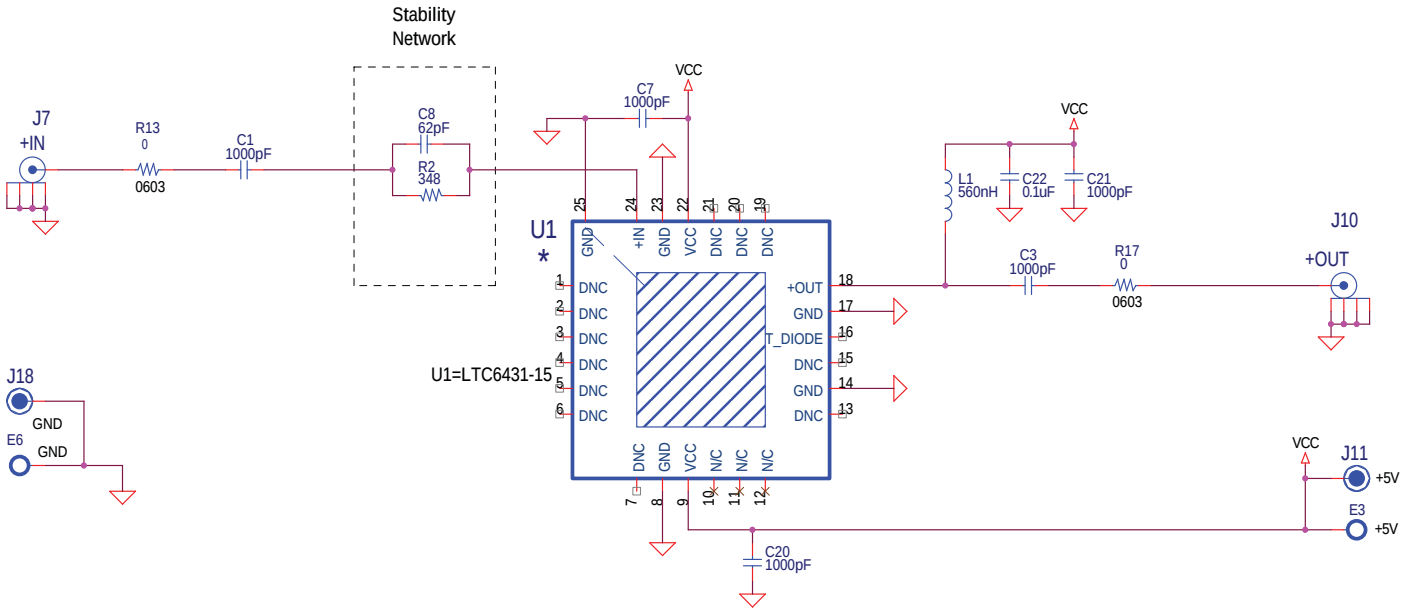


Figure 3. Demo Board DC1774A-C Schematic

OPERATION

The demo circuit 1774A-C is a high linearity fixed gain amplifier. It is designed for ease of use. Both the input and output are internally matched to 50Ω single-ended source and load impedance which is compatible with most test equipment input and output. Figure 2 is shown demo board's S-parameters.

Figure 3 shows the demo circuit's schematic. It requires a minimum of passive supporting components. The input and output DC blocking capacitors (C1 and C3) are required because this device is internally biased for optimal operation. The frequency appropriate choke (L1) and the decoupling capacitors (C21 and C22) provide bias to the RF output node. Only a single 5V supply is necessary for the V_{CC} pins on the device.

An optional parallel 62pF (C8) and 348Ω (R2) input network has been added to insure low frequency stability.

Table 2 shows the function of each input and output on the board.

Table 2. DC1774A-C Board I/O Descriptions

CONNECTOR	FUNCTION
J7 (IN+)	Single-Ended Input. Impedance Matched to 50Ω. Drive from a 50Ω Network Analyzer or Signal Source.
J10 (OUT+)	Single-Ended Output. Impedance Matched to 50Ω. Drive from a 50Ω Network Analyzer or Spectrum Analyzer.
E3 or J11 (V_{CC})	Positive Supply Voltage Source.
E6 or J18 (GND)	Negative Supply Ground.

ADDITIONAL INFORMATION

The particular element values shown in the demo board schematic are chosen for wide bandwidth operation. Depending on the desired frequency, performance may be improved by properly selecting one of the supporting components.

As with any RF device, minimizing ground inductance is critical. Care should be taken with the board layout because of these exposed pad packages. The maximum number of minimum diameter vias holes should be placed underneath the exposed pad. This will ensure good RF ground and low thermal impedance. Maximizing the copper ground plane will also improve heat spreading and low inductance. It is a good idea to cover the via holes with solder mask on the back side of the PCB to prevent solder from wicking away from the critical PCB to exposed pad interface.

The DC1774A-C is a wide bandwidth demo board but it is not intended for operation down to DC. The lower frequency cutoff is limited by on-chip matching elements.

The Schematic Diagram section shows the PCB's schematic of the amplifier family LTC643X-YY. Hence, the board can be modified for multiple demo board versions. For example, both DC1774A-A and DC1774A-B demo boards have a differential amplifier at U1; therefore, the board is using transformers to transform from differential to single-ended input and output. Likewise, the DC1774A-C is a single-ended demo board; consequently, it uses the LTC6431-15 for single-ended input and output.

Setup and Testing Signal Sources

The LTC6431-15 is an amplifier with high linearity performance; therefore, output intermodulation products are very low. For this reason, it drives most test equipment and test setups to their limits. Consequently, accurate measurement of the third-order intercept point for a low distortion IC such as the LTC6431-15 requires certain precautions to be observed in the test setup and testing procedure.

Setup Signal Source

Figure 8 shows a proposed IP3 test setup. This setup has low phase noise, good reverse isolation, high dynamic range, sufficient harmonic filtering and wideband impedance matching. The setup is outlined below:

a. High performance signal generator 1 and 2, the HP8644A, were used to characterize the LTC6431-15. These generators have low harmonic distortion and very low phase noise.

ADDITIONAL INFORMATION

b. High linearity amplifier which will help with the generator's isolation. It also prevents the two signal generators from cross talking with each other and provides higher output power.

c. A lowpass filter to suppress the harmonic contents from interfering with the test signal.

d. The signal combiner from mini circuit, ADP-2-9, combines the two isolated input signals. This combiner has a typical isolation of 27dB. For better VSWR and isolation, use the H-9 signal combiner from MA/COM. The H-9 combiner has > 40dB isolation and a wider frequency range, with about 3dB insertion loss. Even passive devices (i.e. combiners) with magnetic elements can contribute non-linearity to the signal chain.

e. The Attenuator pads, on all three ports of the signal combiner, will support further isolation of the two input signal sources. They will reduce reflection and promote maximum power transfer with wideband impedance matching.

Testing Signal Source

The testing signal should be evaluated and optimized before it is used for measurements. The following outlines the necessary steps to achieve optimization.

a. Apply two independent signals f1 and f2 from signal generator 1 and signal generator 2 at 240MHz and 241MHz with the amplitude = –20dBm for each output tone.

b. Connect the combined signal sources output directly to the spectrum analyzer. (without the DUT).

c. Slowly adjust the amplitude from signal generators so that the output power level is +2dBm for each tone (i.e. The default two tone testing power level for LTC6431-15).

d. Adjust the spectrum analyzer for maximum possible resolution of the intermodulation products amplitude in dBc relative to the main tone power (i.e. adjust frequency span and resolution bandwidth to display the noise floor. The wider span frequency will take a longer time to sweep).

e. Insert a small attenuator pad (3dB or 6dB at the signal combiner inputs) into the setup and observe if the setup limits the intermodulation products level. (i.e. for a good IP3 test setup with sufficient port-to-port isolation, when measuring the intermodulation products, their amplitude level (in dBc), will not be changed when a small attenuation pad insert into the setup). Figure 4 shows the setup at the optimum input Attenuation.

f. Optimize the dynamic range of the spectrum analyzer by adjusting input attenuation. First increase the spectrum analyzer input attenuation (normally in steps of 10dB). If the IMD product levels decrease when the input attenuation is increased, then, the input power level is too high for the spectrum analyzer to make a valid measurement. Figure 5 is depicted the signal overloaded. (i.e. these also mean that you are overloading the spectrum analyzer and it is producing its own IMD products).

If the IMD (dBc) readings are constant, then, a sufficient amount of attenuation has been added. Adding too much attenuation will raise the noise floor and bury the intended IMD signal as shown in Figure 6. Therefore, select just enough attenuation to achieve a stable and valid measurement.

In order to achieve good measurement result, the test system must have lower distortion than the DUT Intermodulation. For example, to yield a +47dBm OIP3, the measured Intermodulation products must be about –90dBc than the test system must have better Intermodulation products than –90dBc.

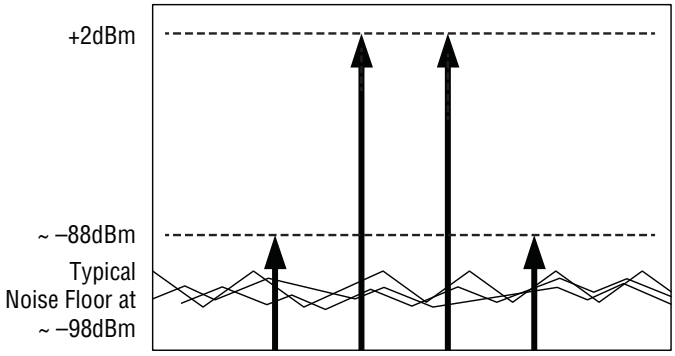


Figure 4. Optimum Input Attenuation

ADDITIONAL INFORMATION

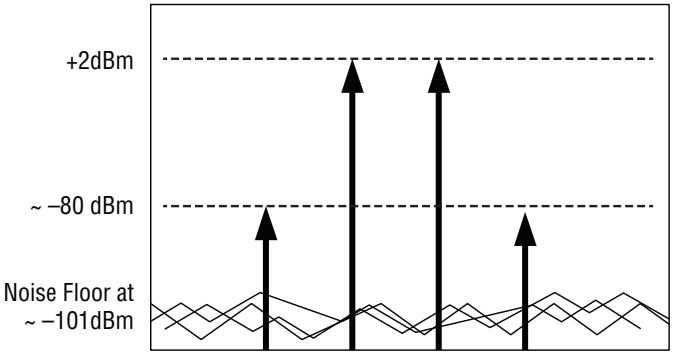


Figure 5. Not Enough Input Attenuation

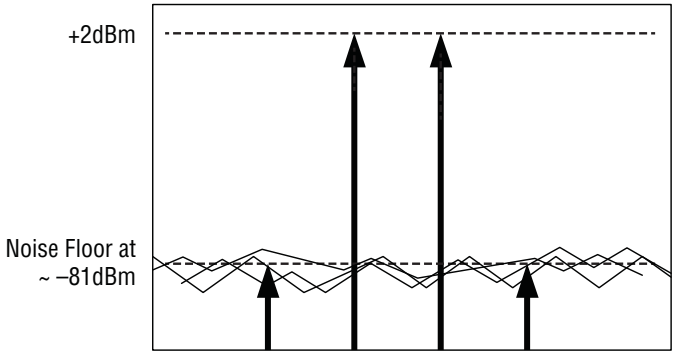


Figure 6. IMD Buried in the Noise Floor

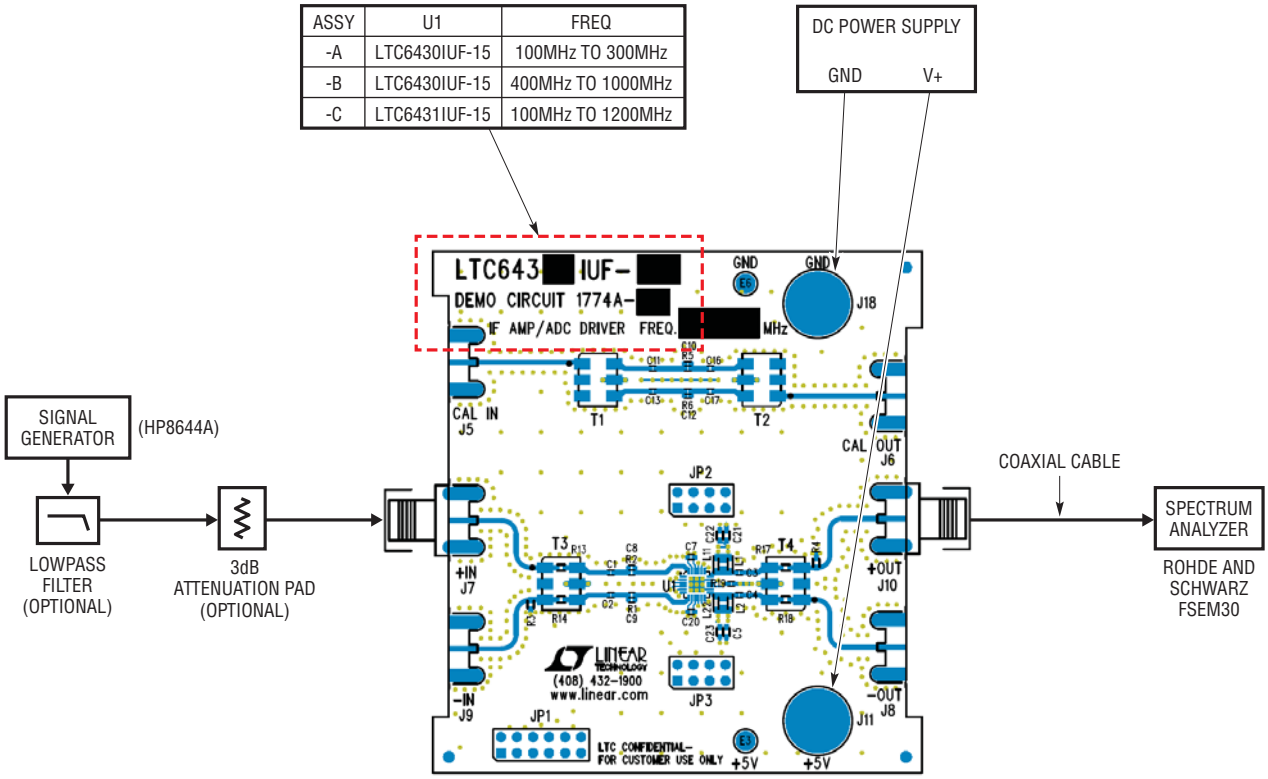


Figure 7. Proper Equipment Setup for Gain and Single-Tone Measurement

ADDITIONAL INFORMATION

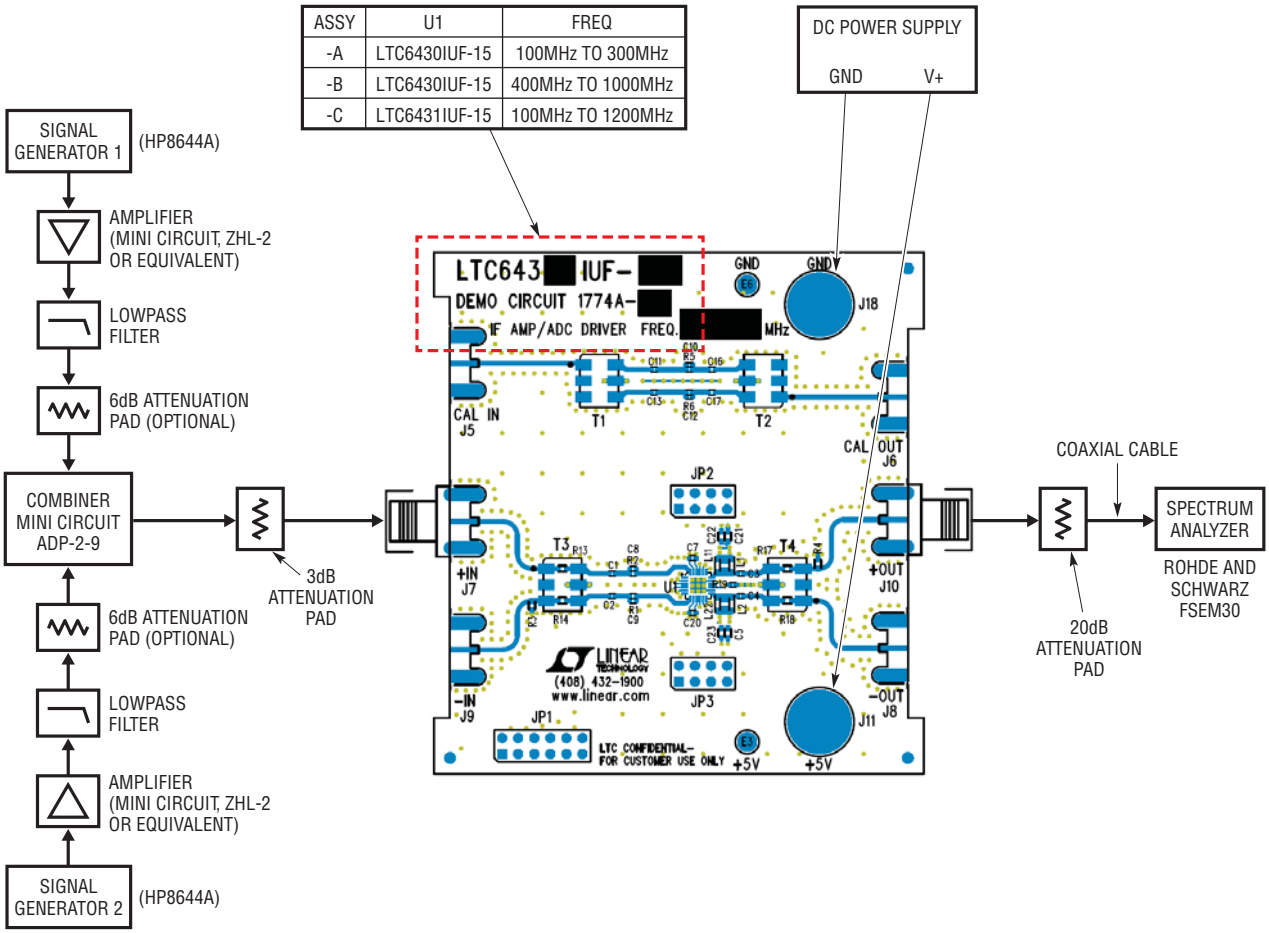
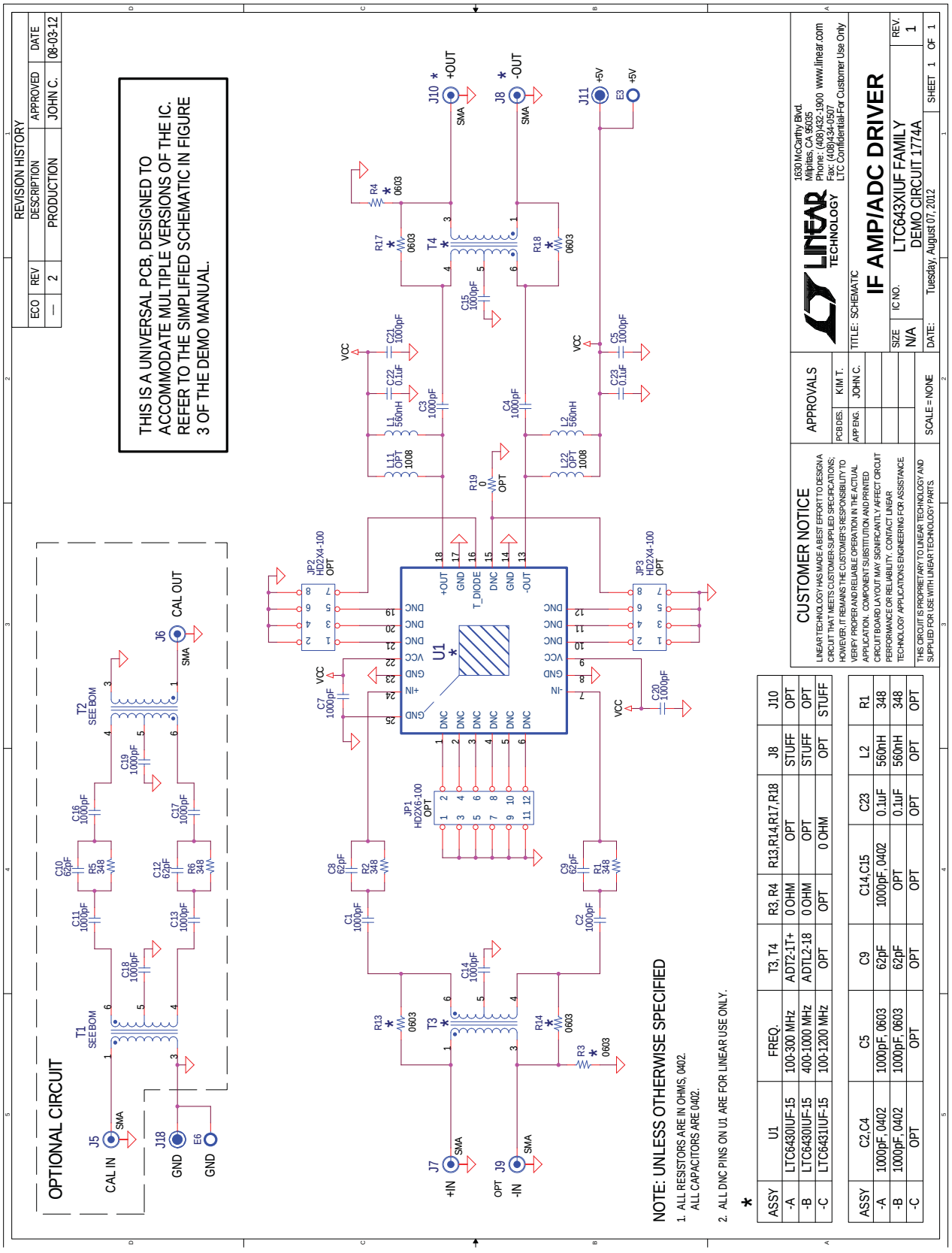


Figure 8. Proper Equipment Setup for IP3 Measurement

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1774A2 Required Circuit Components				
1	4	C1, C3, C7, C20	CAP., X7R, 1000pF, 50V 5%, 0402	AVX, 04025C102JAT2A
2	1	C21	CAP., X7R, 1000pF, 50V 5%, 0603	AVX, 06035C102JAT2A
3	1	C8	CAP., COG, 62pF, 16V 2%, 0402	AVX, 0402YA620GAT2A
4	0	C10, C12	CAP., COG, 62pF, 16V 2%, 0402	OPT
5	0	C11, C13, C16-C19	CAP., X7R, 1000pF, 5%, 0402	OPT
6	1	C22	CAP., X5R, 0.1µF, 10V, 10%, 0603	AVX, 0603ZD104KAT2A
7	2	E3, E6	TESTPOINT, TURRET, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
8	0	JP1	HEADER, 2X6, 0.1"	OPT
9	0	JP2, JP3	HEADER, 2X4, 0.1"	OPT
10	0	J5, J6	CONN., SMA 50Ω EDGE-MOUNTED	OPT
11	1	J7	CONN., SMA 50Ω EDGE-MOUNTED	JOHNSON, 142-0701-851
12	0	J9	CONN., SMA 50Ω EDGE-MOUNTED	OPT
13	2	J11, J18	JACK, BANANA	KEYSTONE, 575-4
14	1	L1	INDUCTOR, CHIP, 560nH, 5%, 0603LS-1608	COILCRAFT, 0603LS-561XJLB
15	0	L11, L22	INDUCTOR, CHIP, 1008LS-2520	OPT
16	1	R2	RES., CHIP, 348Ω, 1%, 0402	YAGEO, RC0402FR-07348RL
17	0	R5, R6	RES., CHIP, 348Ω, 1%, 0402	OPT
18	0	R19	RES., CHIP, 0Ω, 5%, 0402	YAGEO, RC0402JR-070RL
19	2	STENCILS FOR BOTH SIDES		DC1774A-2
DC1774A2-C Required Circuit Components				
1	1	DC1774A-2	GENERAL BOM	
2	0	C2, C4	CAP., X7R, 1000pF, 50V 5%, 0402	AVX, 04025C102JAT2A
3	0	C5	CAP., X7R, 1000pF, 50V 5%, 0603	AVX, 06035C102JAT2A
4	0	C9	CAP., COG, 62pF, 16V 2%, 0402	AVX, 0402YA620GAT2A
5	0	C14, C15	CAP., X7R, 1000pF, 25V 5%, 0402	AVX, 04023C102JAT2A
6	0	C23	CAP., X5R, 0.1µF, 10V, 10%, 0603	AVX, 0603ZD104KAT2A
7	0	L2	INDUCTOR, CHIP, 560nH, 5%, 0603LS-1608	COILCRAFT, 0603LS-561XJLB
8	0	J8	CONN., SMA 50Ω EDGE-MOUNTED	OPT
9	1	J10	CONN., SMA 50Ω EDGE-MOUNTED	JOHNSON, 142-0701-851
10	0	R1	RES., CHIP, 348Ω, 1%, 0402	YAGEO, RC0402FR-07348RL
11	0	R3, R4	RES., CHIP, 0Ω, 1/16W, 5%, 0603	OPT
12	4	R13, R14, R17, R18	RES., CHIP, 0Ω, 1/16W, 5%, 0603	YAGEO, RC0603JR-070RL
13	0	T1, T2	XFMR, MINI-CIRCUITS	OPT
14	0	T3, T4	XFMR, 2:1	OPT
15	1	U1	IC, IF AMP., QFN24UF-4X4	LINEAR TECH., LTC6431IUF-15

SCHEMATIC DIAGRAM



ASSY	U1	FREQ.	T3, T4	R3, R4	R13,R14,R17,R18	J8	J10
-A	LTC6430IUF-15	100-300 MHz	ADT2-1T+	0 OHM	OPT	STUFF	OPT
-B	LTC6430IUF-15	400-1000 MHz	ADTL2-18	0 OHM	OPT	STUFF	OPT
-C	LTC6431IUF-15	100-1200 MHz	OPT	OPT	0 OHM	OPT	STUFF

ASSY	C2,C4	C5	C9	C14,C15	C23	L2	R1
-A	1000pF, 0402	1000pF, 0603	62pF	1000pF, 0402	0.1uF	560nH	348
-B	1000pF, 0402	1000pF, 0603	62pF	OPT	0.1uF	560nH	348
-C	OPT	OPT	OPT	OPT	OPT	OPT	OPT

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