DEMO MANUAL DC2100A

Bi-Directional Cell Balancer Using the LTC3300-1 and the LTC6804-2

DESCRIPTION

Demonstration Circuit DC2100A is a Bi-Directional Cell Balancer using two LTC®3300-1 ICs to achieve active balancing of up to 12 Li-Ion cells. The board uses a single LTC6804-2 Multi-Cell Addressable Battery Stack Monitor IC to measure cell voltages and two LTC3300-1 ICs to provide active cell balancing. The DC2100A-C contains a PIC18F47J53 microcontroller to communicate with the LTC3300-1 and LTC6804-2 ICs, as well as an LTC6820 isoSPI Interface IC for communication with DC2100A-D boards. Up to 7 DC2100A-D boards can be connected to a DC2100A-C to build a stacked system of 8 total boards.*

* Note: The voltage rating of T15 limits the system to a total of 8 total boards.

A graphical user interface (GUI) uses a USB interface to communicate with the DC2100A-C. The GUI controls the LTC3300-1 ICs allowing manual control of the charging/discharging of cells and reporting the voltage of each cell. Cell balancing is achieved through the LTC3300-1 ICs by transferring charge from one or more cells per LTC3300-1 to the stack or from the stack to one or more cells per LTC3300-1.

Design files for this circuit board are available at http://www.linear.com/demo/DC2100A

Source code and documentation for PIC18 and GUI are available at http://www.linear.com/docs/45563

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PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

Cell Voltage Range	3.2V to 4.5V (2.5V to 4.5V)*
Stack Voltage	60V Max
Average Battery Balancing Charge Current (12 Cell)	4.0A (Typ)
Average Battery Balancing Discharge Current (12 Cell)	4.3A (Typ)
Average Battery Balancing Charge Current (6 Cell)	3.4A (Typ)
Average Battery Balancing Discharge Current (6 Cell)	4.0A (Typ)
Balancing Efficiency	90% (Typ)

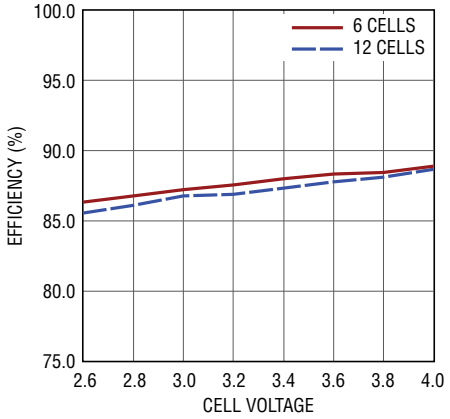
The Cell Voltage Range may be expanded to 2.5V to 4.5V by changing the resistors R_{TONS} to 30.9kΩ and resistors R_{TONP} to 47.5kΩ

DEMO BOARD DESCRIPTION

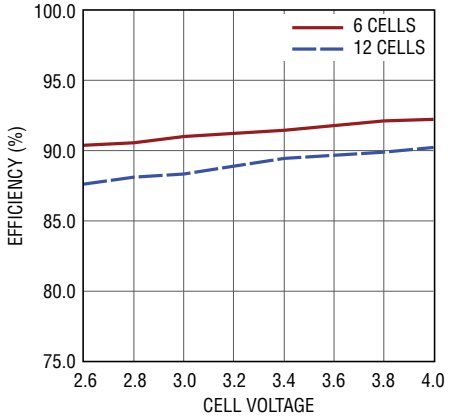
DC2100A-C	12 Cell 4A Active Cell Balancer Controller Board
DC2100A-D	12 Cell 4A Active Cell Balancer Stacked Board

QUICK START PROCEDURE

Discharge Efficiency



Charge Efficiency

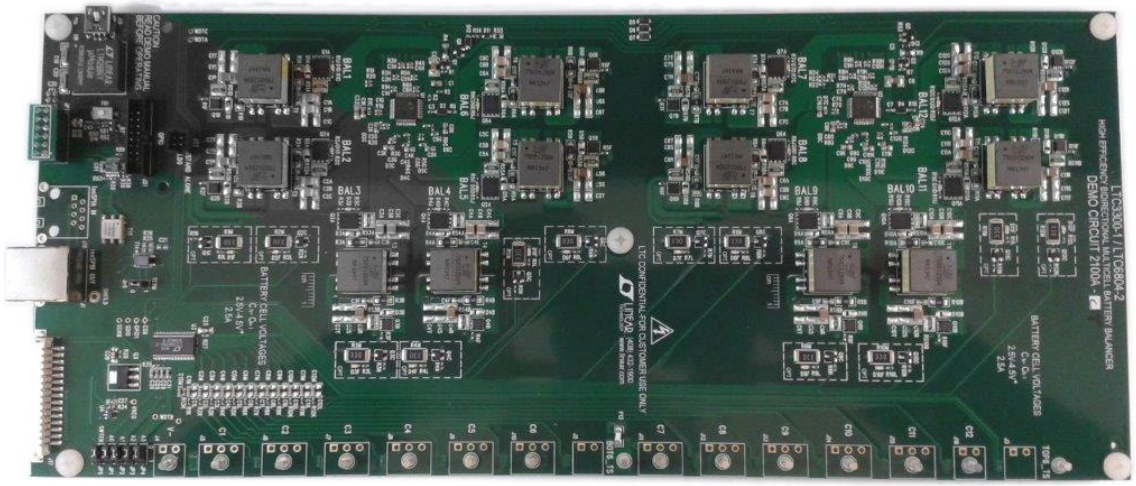


Cell Balancer Efficiency vs Cell Voltage

Thermal Image all Cells Active Balancing

The conditions for the Thermal Plot are:
Cell Voltages at 3.6V, Odd Numbered Cells Discharging, Even Numbered Cells Charging

QUICK START PROCEDURE



DC2100A-C Demo Board Photo

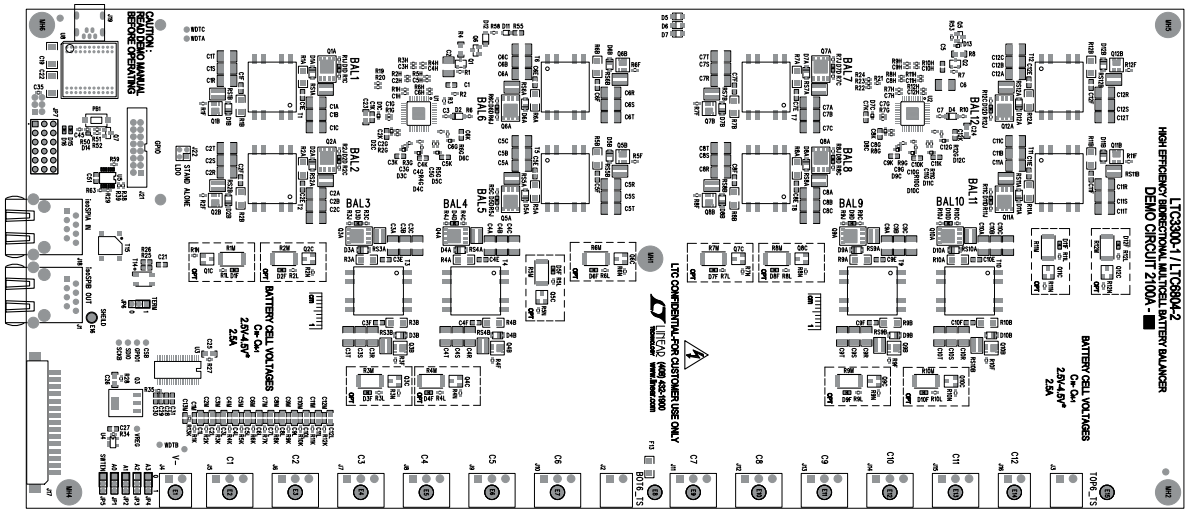


Figure 1. DC2100A-C Demo Board Size Equals 5.5" x 12.8"

OPERATING PRINCIPLE

The DC2100A has a five window GUI, pictured in Figure 28. The Control Panel is the primary window, which displays information about the ICs in the stacked system, the state of the cells on each DC2100A board, and allows manual control of the balancing mode of the LTC3300-1. The Control Panel can spawn three more windows: a Calibration Data window to calibrate cell and balancer characteristics, an Error Log window to display logged errors, and a Graph View window to graphically display characteristics of the stacked system over time. The Graph View window also spawn a Graph View Option window that controls the settings of the Graph View window. The LTC3300-1 Active Balancer is a power stage control IC. The LTC3300-1 does not have a balancer algorithm built into it. The determination of the balancing times and directions are performed at a system level and conveyed to the LTC3300-1 through its SPI interface. The LTC3300-1 only accepts cell charge or discharge commands. Charge is transferred to/from a cell from/to the stack, a series connection of adjacent cells, through a flyback converter that is operating in boundary mode. During discharge of a cell the current in the primary of a coupled inductor transformer with a turns ratio of 1:2, ramps up to 10A at which point the primary switch turns off. The charge in the primary inductor is transferred to the secondary inductor which is connected across the 12 cell sub-stack. This sub-stack current then passes through the series connected cells thus distributing the charge equally across each cell. When charging a cell, the current in the secondary of the coupled inductor transformer ramps up to 5.0A at which point the secondary switch turns off. The charge in the secondary inductor is transferred to the primary inductor which is connected across the cell. The secondary current is drawn from the series connected cells thus removing charge equally across each cell. The efficiency through the fly-back converter is 90%.

QUICK START PROCEDURE

The demonstration circuit is set up per Figure 34 to evaluate the performance of the DC2100A-C Bi-Directional Cell Balancer using the LTC3300-1.

Using short twisted pair leads for any power connections, refer to Figure 34 for the proper measurement and equipment setup. The DC2100A will support a system of 4 to 12 cells (See Figures 34 and 37 to 44).

Recommended Cell Connection Sequence

The recommended cell connection sequence is to connect the V^- connection first followed by connecting cells 1 through cell 12. Disconnection of the cells should follow this sequence in the reverse order with the V^- connection being removed last. Connecting the V^- connection first and removing last is recommended because the V^- connection is the ground reference for the circuitry within the demo board. After connecting the V^-, all other cell connection sequence is less critical as long as the cell circuit capacitances are matched as they are in the demo board. Following the recommended cell connection removes the possibility of excessive voltage on any of the lower cells due to an imbalance in cell circuit capacitance.

A 4 bit board ID code is set by the A0 through A3 jumpers on the DC2100A-C must be set to 0000. The jumpers on the DC2100A-D boards must be set to unique values between 0001 and 1111.

To use the DC2100A, the PC must first have the proper driver and software installed. To do this, download the QuikEval™ software from Linear Technology, at www.linear.com:

http://www.linear.com/designtools/software/quik_eval.jsp

1) Install the QuikEval software by running the executable ltcqev.exe. Follow the instructions to connect the DC2100A.

If you fail to unplug the DC2100A, the DC2100A driver will not install!

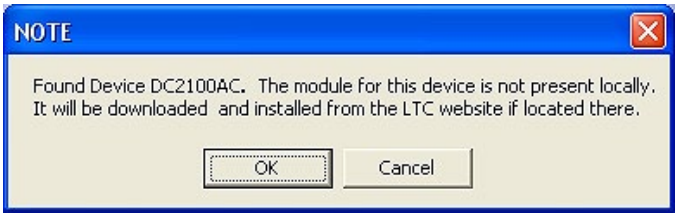
QUICK START PROCEDURE

2) When installation of QuikEval is complete, close the QuikEval program.

3) Reopen QuikEval. If properly installed, QuikEval will show the following message until the DC2100A is connected:

If not properly installed, QuikEval will be unable to connect to the DC2100A. Please retry the software installation, with the DC2100A disconnected.

4) Now connect the DC2100A. The QuikEval software will recognize when the DC2100A demo board has been found, and will offer to download and install the module from the LTC website:



At this point, select OK.

5) The QuikEval software will now download and open the software for the DC2100A.

6) Close QuikEval Software, as it is no longer needed for the DC2100A.

When the DC2100A-C is connected to the PC, the PIC18 will become powered. The powered status will be indicated through Green LED D15 flashing with a 1 second period. When the GUI's launched, it will begin communicating with the PIC18 via USB. Proper USB communication will be indicated through Orange LED D16 lighting during each USB transaction.

When the GUI connects to the DC2100A system, it will display the boards attached in the Control Panel System Tree View. The DC2100A GUI Control Panel is able to display the data and controls for one board at a time. When a board is selected in the System Tree View, all of the Windows will begin to display the data and controls for that board. The Selected Board Indicator in each window will indicate which board is selected. The Board Status LEDs indicate the state of the boards similarly to the LEDs on the DC2100A-C.

The green LED flashes quickly when a board is connected but its cells are not powered, and slowly when a board is connected with powered cells. The amber LED turns on when the GUI is communicating with a board via USB.

When the DC2100A is used with fewer than 12 cells, the board must be configured in the GUI so that the unpopulated

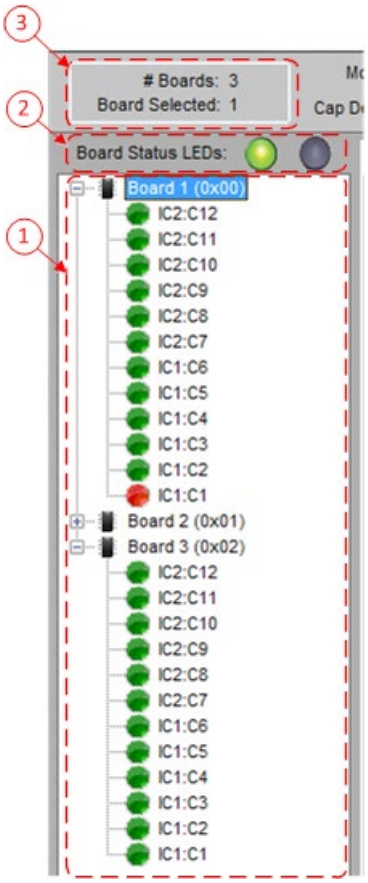


Figure 2. Board Selection in System Tree View

QUICK START PROCEDURE

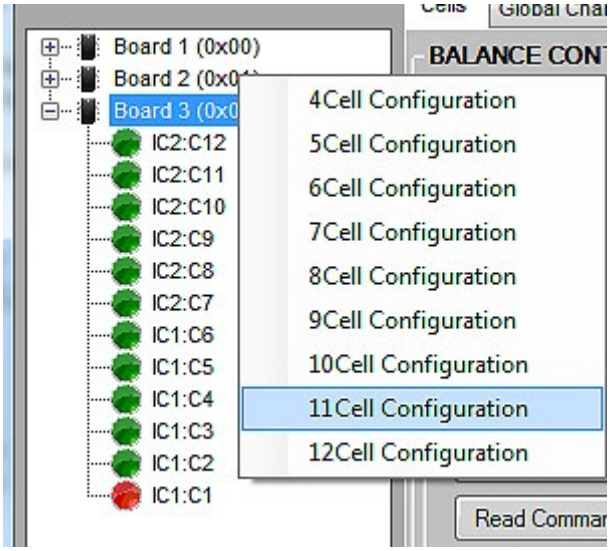


Figure 3. Turning off Cell 1 on Board 3

cells are not interpreted as an undervoltage condition. When a cell is red in the System Tree View, it has been specified as unpopulated. To configure a DC2100A for fewer than 12 cells, right click the board in the System Tree View and select the number of populated cells.

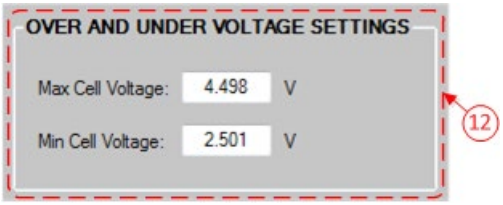


Figure 4. VOV and VUV Text Boxes

The DC2100A GUI periodically checks for OV and UV measured on the cells when balancing. To avoid the program from suspending balancing from a OV and UV measurement during normal operation, the Max Cell Voltage and UV values must be entered in the VOV and Min Cell Voltages text boxes tab shown in Figure 4.

The cell voltages in the Control Panel can be configured to stop updating automatically, and only be updated when the Read Voltages button is clicked (as shown in Figure 5). This provides the ability to freeze the data for a board at any instant in time.

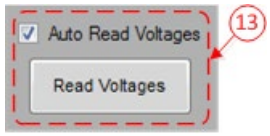


Figure 5. Voltage Display Controls

An alternative method of viewing the data is available by pressing the Graph Data button, to open the Graph View Window. The Graph View Window is detailed in Figure 33, and allows data for each board and the stacked system to be graphed over time. The graph data can be saved and are reloaded later, and the View Options control allows configuration of the Graph Display. The Stack Summary provides graphed data for the entire system, where the Board Summary, Cell Voltages, and Temperatures allow data to be graphed for boards selected in the Tree View. Up to 15 values may be graphed at one time, and the graph is limited to 500 seconds of data.

The Global Channel Monitor tab switches the Control Panel to a grid view in which all of the cell voltages can be viewed at the same time. Disabled cells will be color coded as grey, and cells selected in the System Tree View will be highlighted in blue. Details of the Global Channel Monitor View are provided in Figure 30.

Several controls are available on the Control Panel Cell Tab for issuing balancing commands to the selected board. In the Balance Mode Select Boxes, you can manually select which cells are to be discharged by clicking the cell's DISCHARGE button, which cells are to be charged by clicking the cell's CHARGE button.

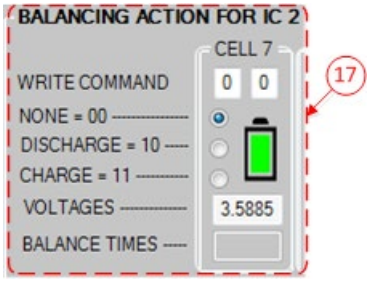


Figure 6. Balance Mode Select Boxes

Note that if a cell is disabled, the balance mode select box will not be selected and the cell pictured will be grey. Balancing and overvoltage conditions are also indicated by color, according to the Cell State Color Key.

QUICK START PROCEDURE

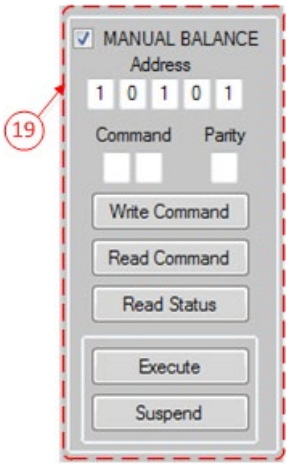


Figure 7. Manual Balance Control

Once the balance modes are selected, they are not immediately written to the LTC3300-1 ICs. Two methods are available for writing the balance modes: Manual and Timed Balance Control. When the Manual Balance method is selected, the Write Command button will cause the GUI to write the balance modes to the selected board.

Once the balance mode commands are written to the LTC3300-1 ICs, balancing will not begin until the Execute button has been pressed to command the balancing to begin. The Execute button will cause all of the attached boards to begin balancing. This allows each board to have its balancing commands set up when selected in the System Tree View, and to then have all of the balancers turned on together. To disable any cell from balancing, the cell's NONE button must be clicked in the Balance Mode Select Box followed by clicking the Write Command button and finally the Execute button. Each time the Execute button is pressed, the Read Command and Read Status registers will be updated for the selected board (see Figure 8).

When the Timed Balance method of balance control is selected, the GUI allows the user to program the balancer to charge or discharge each cell for a specific amount of time. The LTC3300-1 is a power stage control IC. The determination of the balancing times and directions are done at the System level and conveyed to the LTC3300-1 through its SPI communications port. In order to perform a timed balance, the TIMED BALANCE check shown in Figure 9 must be selected to have access to the timed balance controls as shown in the Balance Mode Select Boxes.

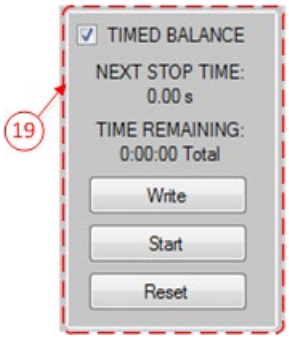


Figure 9. Timed Balance Control

To use the Timed Balance method of balance control, select the DISCHARGE, CHARGE, or NONE button for each cell and then enter the time in seconds into the cells "BALANCE TIME" text box. Press the Write button to write the balance commands and times into the selected board. Select another board from the System Tree View and repeat until the balance settings have been loaded into each DC2100A board. Press the Start button to begin the timed balance

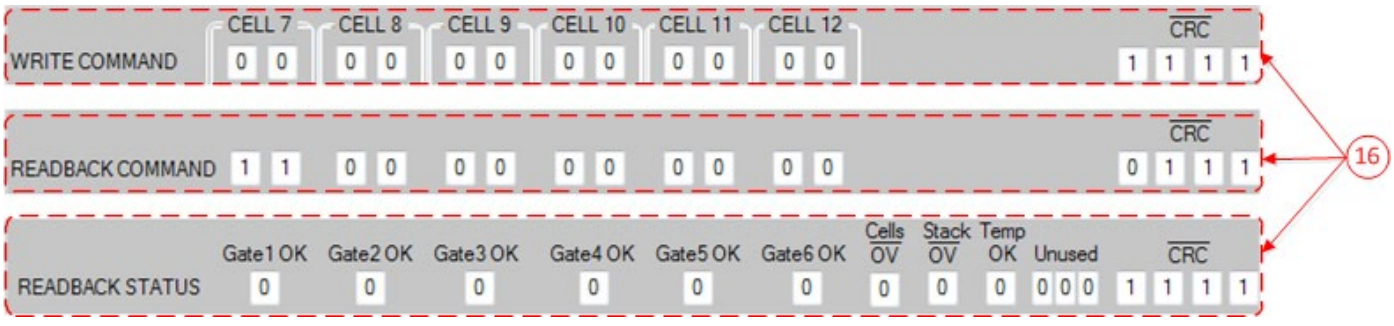


Figure 8. LTC3300-1 Register Display

QUICK START PROCEDURE

for all of the boards in the stacked system. The balance times will then begin to count down as the balancing is performed, and the LTC3300-1 Register Display will be continuously updated. The NEXT STOP TIME field will display the earliest time that one of the cells will complete balancing, and the board on which that cell resides. When the NEXT STOP TIME arrives, the balance mode for that cell will change to NONE and a new cell will display for the NEXT STOP TIME. The TIME REMAINING will display the total time remaining in the timed balancing, after which all of the cells will have NONE for their balancing mode.

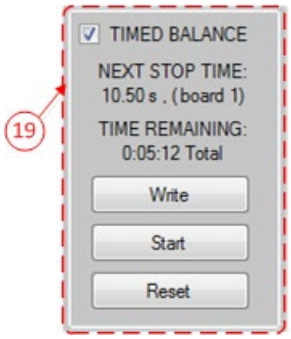


Figure 10. Timed Balancing

While balancing is active, the Start button (see Figure 10) will change to Stop, in case the user wishes to pause the balancing operation. Selecting the Reset button will reset all of the balance timers to 0 and all of the cell balance modes to NONE.

The user can load and store several timed balance profiles in the Board Configuration control (see Figure 11). The Imbalance Cells button in this control will load a pattern of charging and discharging cells. The user can then manually configure the Timed Balance controls to correct for the imbalance created by this button. The user can save their Timed Balance configuration and reload it later. The configuration will also save the over and undervoltage settings, as well as the disabled cell configuration.

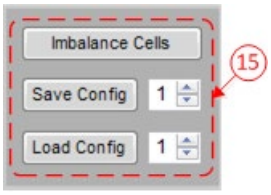


Figure 11. Board Configuration Control

In addition to the Graph View of the data, the DC2100A system can be monitored over a long period of time with the results written to a CSV file. The logging interval and length can be configured, but note that the size of the data files can grow quite large for stacked systems with many boards. The projected memory size will be displayed before the user begins logging by pressing the Start Data Log button. Once the button is pressed, the user will be prompted to enter a data file name and location, and the logging will begin.

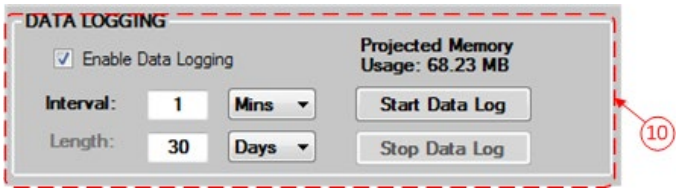


Figure 12. Data Log Control

Although each DC2100A will balance with currents similar to those listed in Table 1, each board was tested upon manufacture and its actual balancing currents are stored within the DC2100A. These currents can be accessed by pressing the Calibration Data button on the Control Panel, which will then launch the Calibration Data window (see Figure 31). In this window the user has the ability to enter new calibration current values, or reset the currents to the

QUICK START PROCEDURE

values from Table 1. It is not recommended to change these, however, from the factory measured settings. The capacity of each cell can also be stored in the DC2100A. The capacity and balance currents will be used in a later release of firmware for the DC2100A-C, which will employ an autonomous balancing algorithm.

The DC2100A GUI installed with the QuikEval software, will always contain the most up to date version of Firmware for the DC2100A. In order to update the firmware, press the Update Firmware button in the Control Panel.

Figure 13. Update Firmware Button

After confirming that the Firmware should be updated, a command line window will be launched in which the PIC18 on the DC2100A is first erased, and then reprogrammed. Do not remove power from the DC2100A while the Firmware is being updated.

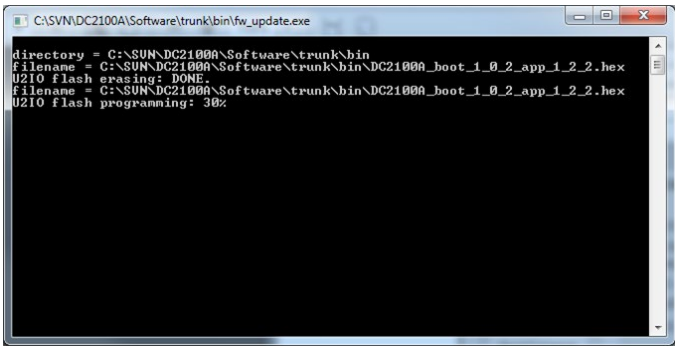


Figure 14. Firmware Update Window

Cell Balancer Efficiency Measurements

Figure 35 shows the proper connections for measuring the efficiency of a cell balancer. The secondary of the cell balancer connects to the top of stack. This connection needs to be to an isolated power source through a current sensing resistor (0.10Ω). Cells 1 through 6 are connected to the BOT6_TS turret with its return path the V- turret while Cells 7 through 12 are connected to the TOP6_TS turret with its return path the C6 turret. These isolated power sources simulate a stack of cells from 3 to 12 cells. The primary side connection of the cell balancers are connected to a string of power sources that simulate the battery stack. Cell 1 power source is a two wire connection that connects the positive node, through a current sensing resistor (0.01Ω), to the C1 turret, and the negative node to the V- turret. Remote sense connections for power sources with remote sensing capabilities should be connected to the C1 and V- respectively. All other connections of the simulated string of cells connect their positive node, through a current sensing resistor (0.01Ω), to respective turrets. Cell voltage measurements should be made across the C(x) and C(x-1) turrets of the respective cells. Stack voltage measurements should be made at the BOT6_TS and TOP6_TS turrets and their return path turret.

To calculate cell balancer efficiency use the expressions below:

Cells 1-6

Charge Mode

$$\text{Efficiency}_1 = \frac{Vm_1 \bullet Vm_2 \bullet 10}{Vm_3 \bullet Vm_4} \bullet 100\%$$

Discharge Mode

$$\text{Efficiency}_1 = \frac{Vm_3 \bullet Vm_4}{Vm_1 \bullet Vm_2 \bullet 10} \bullet 100\%$$

Cells 7-12

Charge Mode

$$\text{Efficiency}_{11} = \frac{Vm_5 \bullet Vm_6 \bullet 10}{Vm_7 \bullet Vm_8} \bullet 100\%$$

Discharge Mode

$$\text{Efficiency}_{11} = \frac{Vm_7 \bullet Vm_8}{Vm_5 \bullet Vm_6 \bullet 10} \bullet 100\%$$

QUICK START PROCEDURE

Cell Balancer Performance Measurements

Table 2 through Table 5 present the typical operational data for a 12 cell and 6 cell balancer in both Discharge and Charge modes. The cell voltages were 3.6V and measurements of Cell Current, Stack Current, Operating Frequency were taken and transfer Efficiency was calculated from the data. Figure 15 through Figure 18 are actual in-circuit waveforms taken on Cell 1 and Cell 7 while operating in both modes. The waveforms present voltage on the primary side and secondary side MOSFET's drain to source voltage and the primary side and secondary side current sense inputs to the LTC3300-1.

Figure 14 through Figure 22 are cell and stack currents taken over a range of cell voltages from 2.6V to 4.0V. The R_{TONP} and R_{TONS} resistors were set for 2.6V cell voltage operation. All cells were set to the cell voltage under test. The slight negative slope in current at higher voltages is due to the increased operating frequency and the circuit delays and dead time becoming a higher percentage of the operating period.

Table 2. Typical 12 Cell Discharge Data

Cell I (A)	Stack I (A)	Frequency (KHz)	Efficiency
4.250	0.311	95.7	87.9%

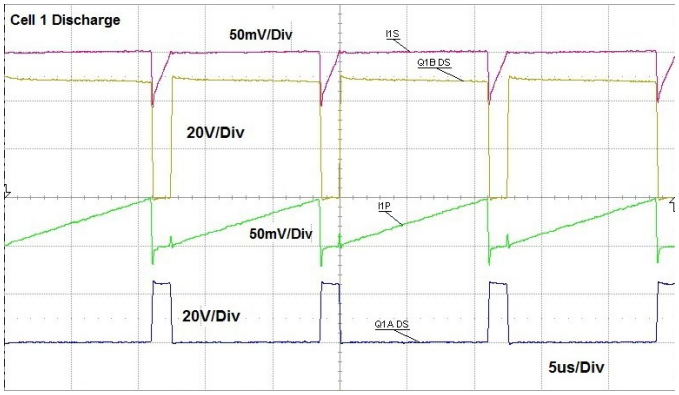


Figure 15. 12 Cell Discharge Waveforms

Table 3. Typical 12 Cell Charge Data

Cell I (A)	Stack I (A)	Frequency (KHz)	Efficiency
3.960	0.367	106.6	89.7%

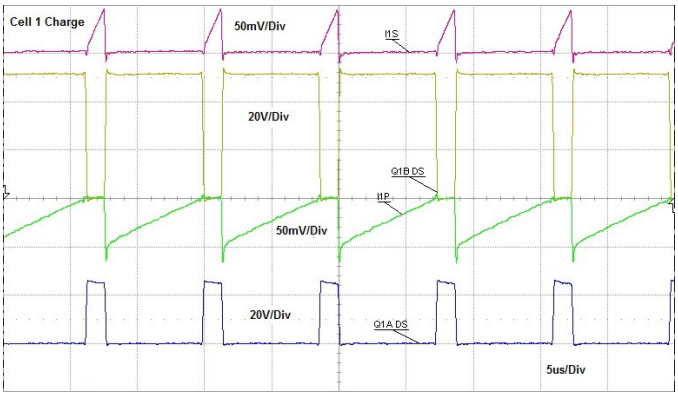


Figure 16. 12 Cell Charge Waveforms

Table 4. Typical 6 Cell Discharge Data

Cell I (A)	Stack I (A)	Frequency (KHz)	Efficiency
4.000	0.577	88.6	88.4%

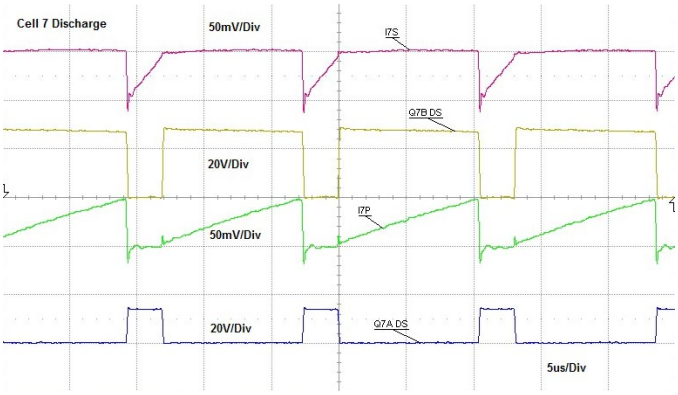


Figure 17. 6 Cell Discharge Waveforms

QUICK START PROCEDURE

Table 5. Typical 6 Cell Charge Data

Cell I (A)	Stack I (A)	Frequency (KHz)	Efficiency
3.430	0.619	91.2	91.8%

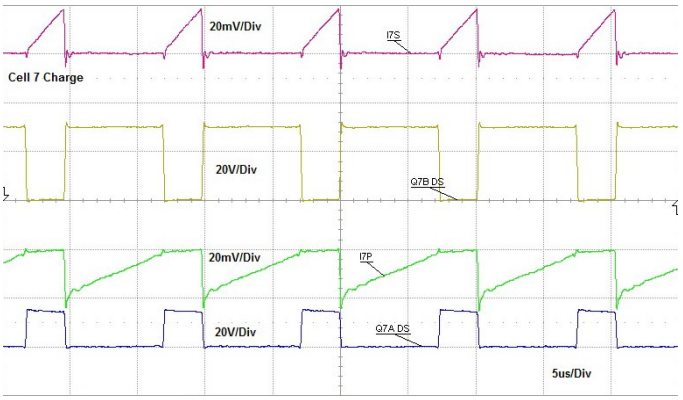


Figure 18. 6 Cell Charge Waveforms

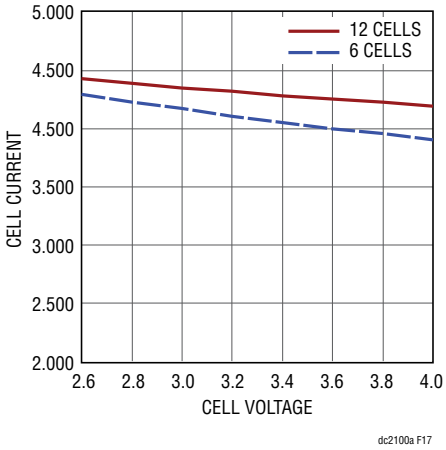


Figure 19. Cell Discharge Current

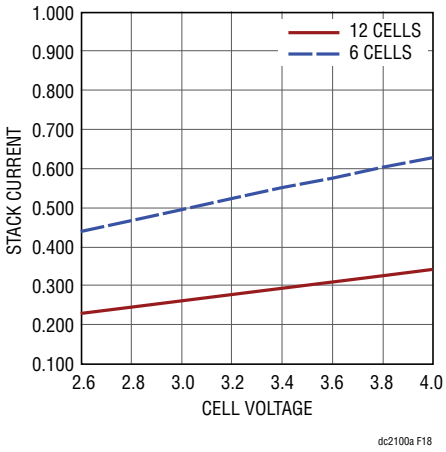


Figure 20. Stack Discharge Current

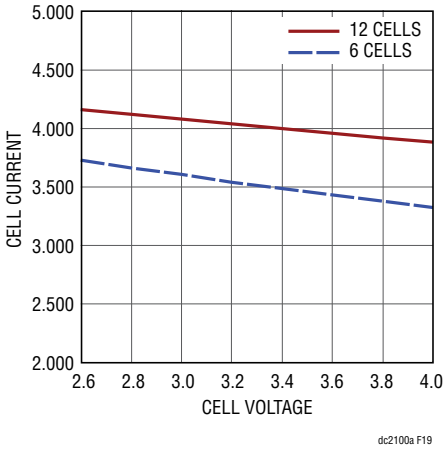


Figure 21. Cell Charge Current

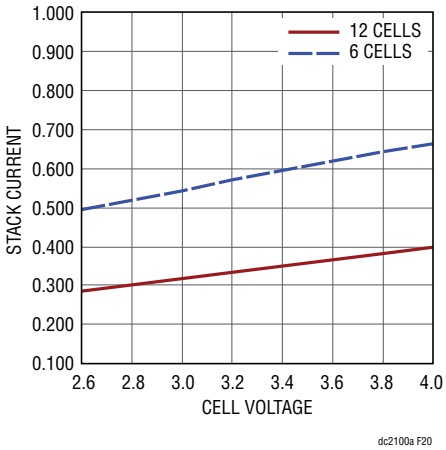


Figure 22. Stack Charge Current

QUICK START PROCEDURE

Two or More Board Setup and Operation

When connecting two or more DC2100A boards together, the interface cables must be connected in sequence as shown in Figure 23 to avoid large inrush currents. When connecting more than one DC2100A's into a system containing more than 12 batteries, DC2100A-D are used in locations 2 through 8. The PC USB port is connected to the bottom DC2100A-C (J19) board first and then the next DC2100A-D (J18) may be connected to the bottom DC2100A-C (J1) with a CAT-5 cable. CAT-5 cables are used for communication connects between all DC2100A demo boards in the system. J1 is the output port while J18 is the input port. The Top DC2100A-D must have the JP6 in position 1. All other DC2100A will have JP6 in position 0.

The 24 cell should be interconnected as shown in Figure 24 to allow balancing between the two 12 cell stacks.

Additional Circuitry

Additional circuitry has been added to increase the robustness of the design for fault insertions.

Cell 6 Wire Disconnection

A 10A 200V Schottky diode has been added for a high current path when the connection between battery cells is broken when a battery stack load is present. The 200V reverse voltage rating of the diode was selected to minimize the reverse leakage current with cell voltage of 4V. The 10A current rating was selected for its low forward voltage drop which will minimize the current in the parallel diode within the LTC3300-1 as well as surviving the fusing current of the 12A cell fuses on the DC2100A.

Two overvoltage detection circuits have been added to the design that will sense an overvoltage condition on Cell 6 and Cell 7 when a disconnection of the Cell 6 wire connection between Cell 6 + and Cell 7- of the battery stack occurs. When Cell 6 is being discharged and other cells controlled by the U1, the lower LTC3300-1, and U2, the upper LTC3300-1 are operational, an overvoltage can occur on Cell 7. The overvoltage on Cell 7 will shut down the operation of Cell 7 – Cell 12 but Cell 1 – Cell 6 will continue to operate. The overvoltage sensing circuit Q4, D8, D10 and R56 will turn off Cell 1 – Cell 6 through the internal overvoltage protection circuit within the LTC3300-1 of U1.

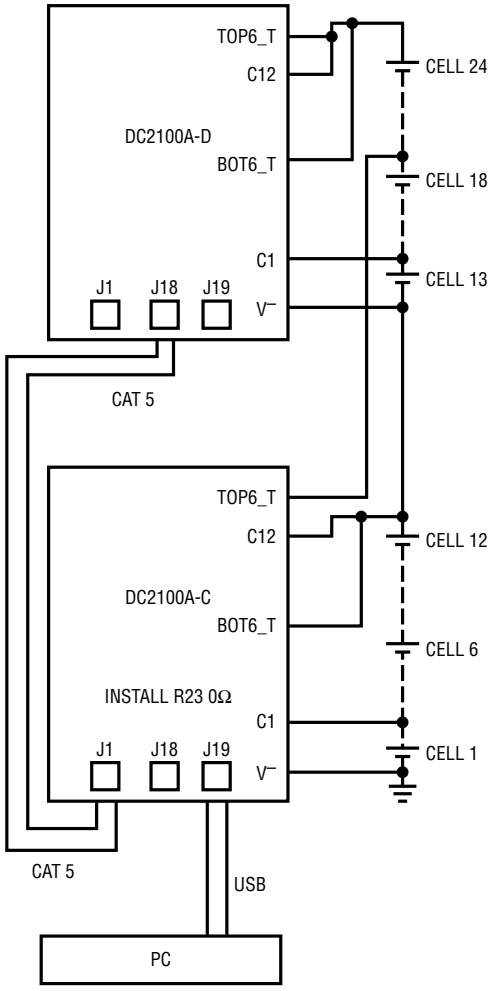


Figure 24. 24 Cell Interconnecting Stacks

Figure 23. Two DC2100A SPI Connection

QUICK START PROCEDURE

A similar event occurs when Cell 6 is operating in the Charge Mode and other cells controlled by the U1, the lower LTC3300-1, and U2, the upper LTC3300-1 are operational, an overvoltage can occur on Cell 6. The overvoltage on Cell 6 will shut down the operation of Cell 1 – Cell 6 but Cell 7– Cell 12 will continue to operate. The overvoltage sensing circuit Q5, Q6, D12, D13 and R58 will turn off the operations of Cell 7 – Cell 12 through the internal overvoltage protection circuit within the LTC3300-1 of U2.

Cell Bypass Capacitors

The DC2100A contains bypass capacitors from the cell connections and the stack connections. These capacitors have a dual function of smoothing the high triangular current wave before the current travels down the interconnecting wires to the cells and they also help balance the voltage between cells when hot-plugging cells in a random order. The RMS current rating of these capacitors is a critical parameter for these bypass capacitors as well as their physical size. These high triangular current waveforms produce an RMS current that passes through the capacitors which result in an internal heat rise. Larger physical size MLCC capacitors have higher RMS current rating due to their greater surface area to dissipate the heat rise. The capacitance of MLCC capacitors decreases with applied voltage and this must be taken into account when selecting the capacitance value. If a connection is lost during balancing, the differential voltage seen by the LTC3300-1 power circuit on each side of the break may increase or decrease depending on whether the power stage is charging or discharging and where the break occurred. The worst-case scenario is when the balancers on each side of the break are active and balancing in opposite directions. Here the differential voltage will increase rapidly on one side and decrease rapidly on the other. The LTC3300-1 contains an overvoltage protection comparator which monitors the cell voltage and will shut down all balancers before the differential voltage on any cell input reaches the maximum absolute voltage rating.

Each cell node must have an equivalent capacitance across it to prevent an overvoltage condition when randomly connecting cells to the LTC3300-1 battery balancer circuit. In addition to the smoothing capacitors across each balancer power circuit, there are capacitor across the Cx pins of the LTC3300-1 to reduce high frequency noise on these pins and capacitors across adjacent cells to act as a reservoir of charge for the cell's MOSFET gate circuit. These reservoir capacitors must also be of equal value to maintain the balancing of voltage and a capacitor of 2x the value of the reservoir capacitors must be connected between C1 and V^- of the lowest LTC3300-1 and from the top cell to the cell below it to insure an equal voltage across all cells when the battery stack is initially connected. Figures 25 and 26 detail these capacitor connections and their values. The reservoir capacitors must be large compared to the capacitors across the Cx pins to force the MOSFET gate driver charging current to flow through the reservoir capacitors. An effective 10:1 ratio between these cell capacitors was selected when considering that a capacitor across two cells would result in a 5:1 ratio.

Temperature Monitor

The DC2100A has the ability to monitor 12 temperature locations within the battery pack. The GUI Control Panel Window, Figure 29, displays these temperatures in two temperature displays, item 16 of Figure 29, for 6 temperature locations. The DC2100A contains a daughter card that can be used to connect twisted pair wires to twelve 10K NTC thermistors, Vishay NTHS0603N01N1002JE or equivalent, within the battery pack. The daughter card is shipped with fixed resistors to simulate temperature readings within a battery pack. These resistor values are selected to display the range of possible temperatures that may be measured. When connecting the daughter card to the actual thermistor, these resistors should be removed and the twisted pair wires connected to the turrets provided.

QUICK START PROCEDURE

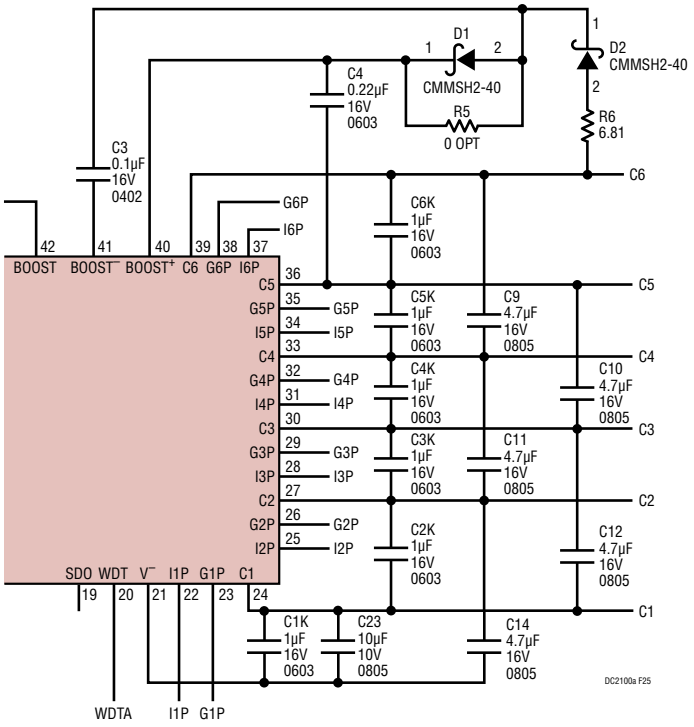


Figure 25. Bypass Capacitors on Lowest LTC3300-1

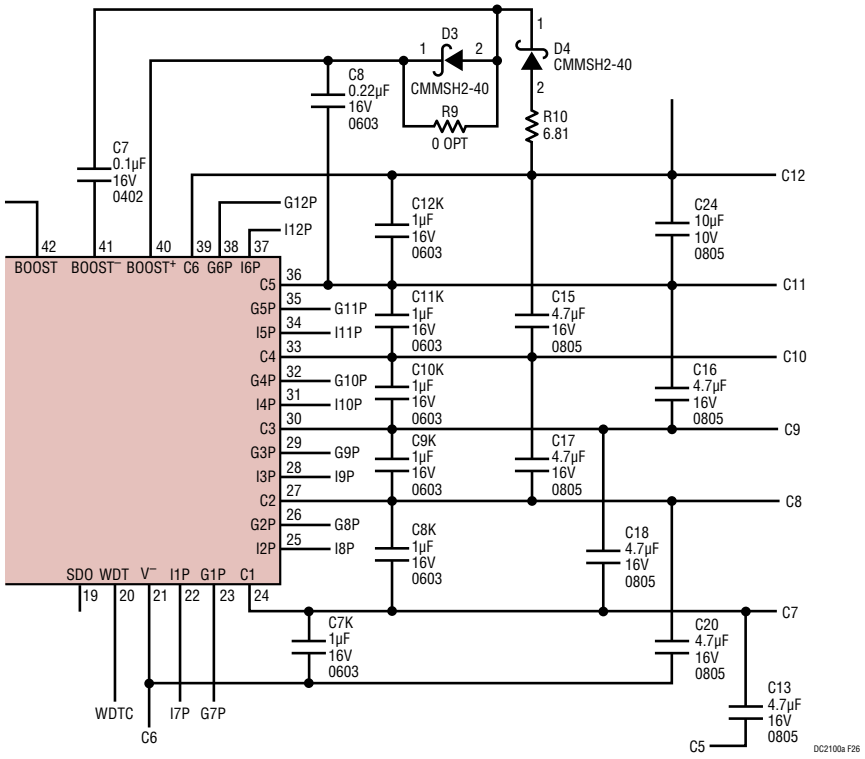


Figure 26. Bypass Capacitors on the Top LTC3300-1

QUICK START PROCEDURE

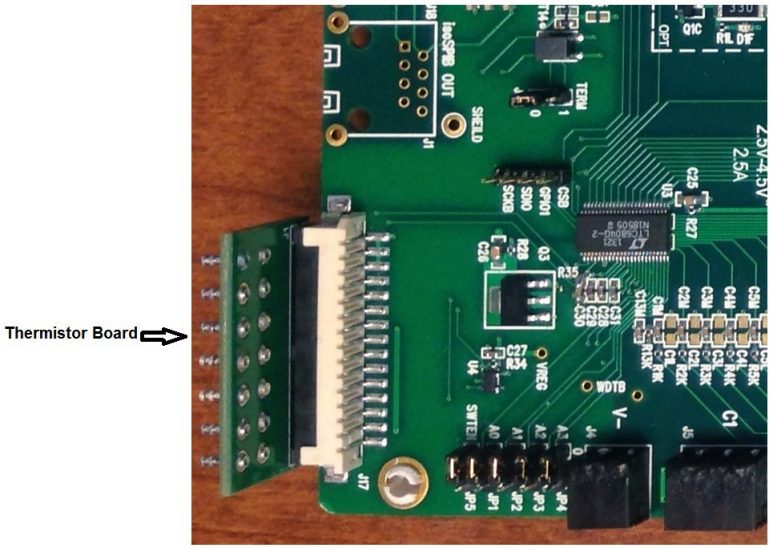
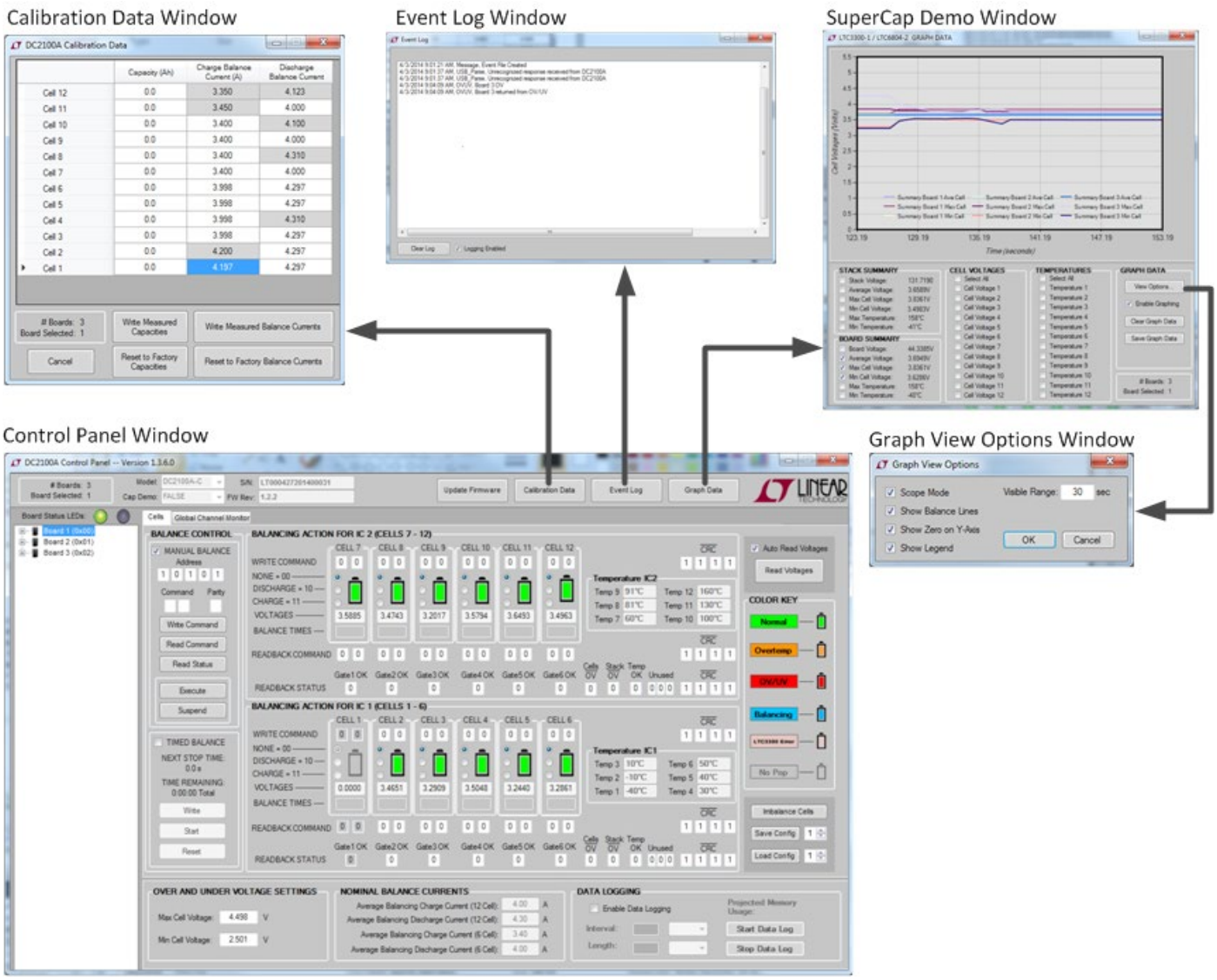


Figure 27. Thermistor Board Location

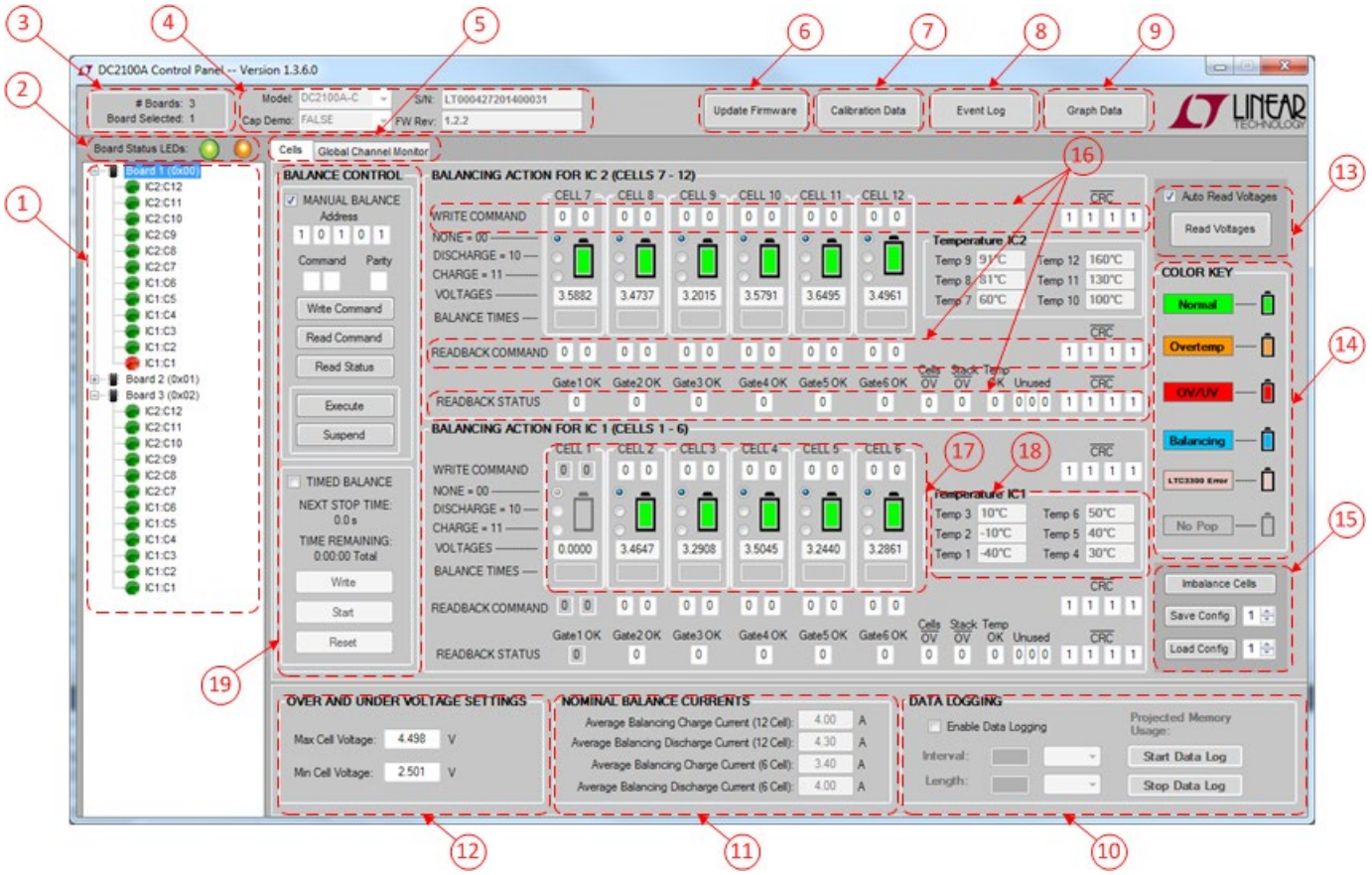
QUICK START PROCEDURE



1. CONTROL PANEL WINDOW – FIGURE 28 (CELLS TAB)
2. CONTROL PANEL WINDOW – FIGURE 29 (GLOBAL CHANNEL MONITOR TAB)
3. CALIBRATION DATA WINDOW - FIGURE 30
4. EVENT LOG WINDOW - FIGURE 31
5. GRAPH VIEW WINDOW - FIGURE 32

Figure 28. GUI Navigation

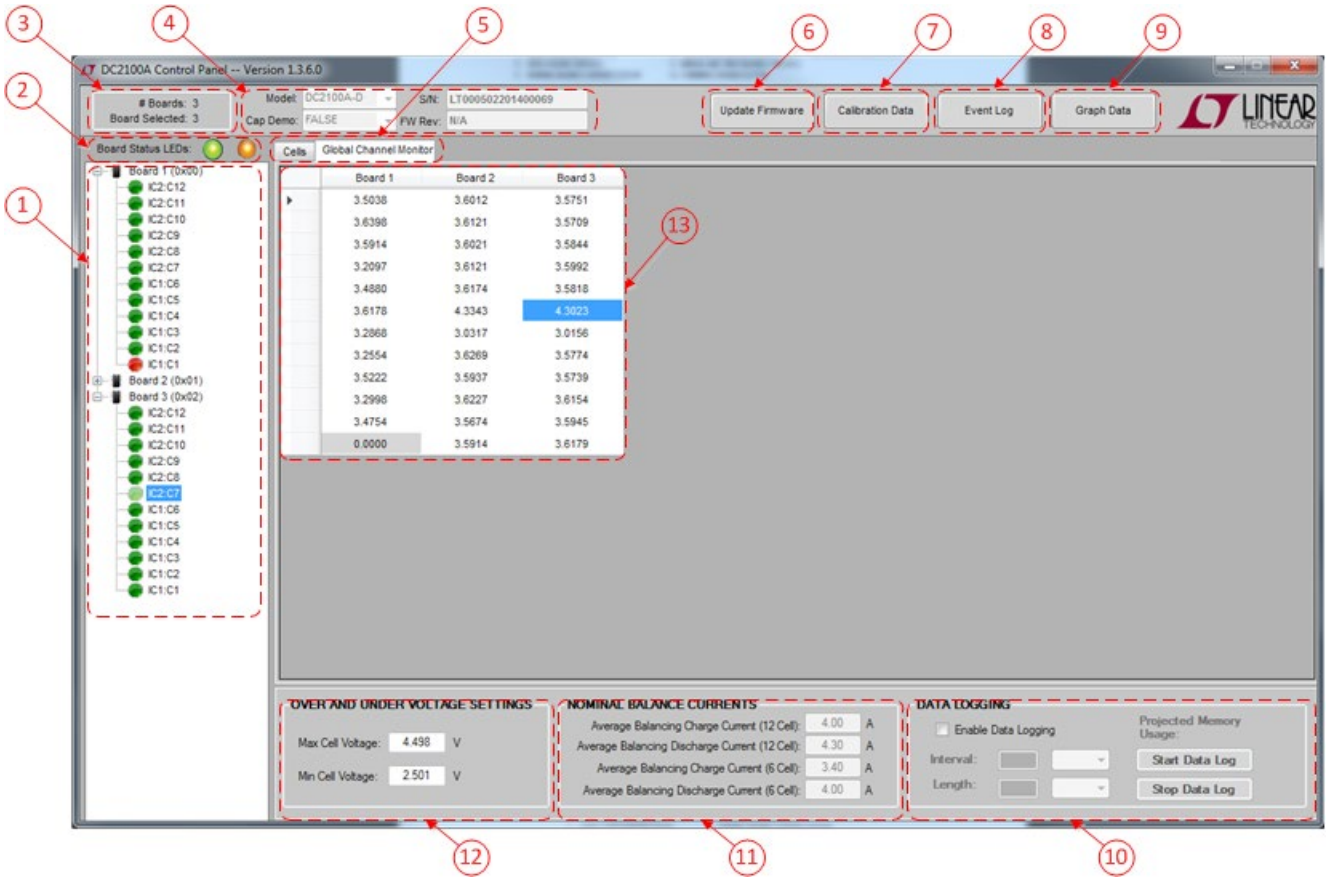
QUICK START PROCEDURE



1. SYSTEM TREE VIEW
2. BOARD STATUS LED
3. SELECTED BOARD INDICATOR
4. BOARD IDENTIFICATION DISPLAY
5. DATA DISPLAY TABS
6. FIRMWARE UPGRADE BUTTON
7. CALIBRATION DATA WINDOW BUTTON
8. EVENT LOG WINDOW BUTTON
9. GRAPH VIEW WINDOW BUTTON
10. DATA LOGGING CONTROLS
11. NOMINAL BALANCE CURRENTS DISPLAY
12. OVER AND UNDER VOLTAGE SETTING CONTROLS
13. VOLTAGE DISPLAY CONTROLS
14. CELL STATE COLOR KEY
15. BOARD CONFIGURATION
16. LTC3300-1 REGISTER DISPLAY (2 INSTANCES FOR 2 ICS ON DC2100A)
17. BALANCE MODE SELECT BOXES (2 GROUPS, WITH 6 CELLS IN EACH GROUP)
18. TEMPERATURE DISPLAY (2 GROUPS, WITH 6 TEMPERATURES IN EACH GROUP)
19. MANUAL AND TIMED BALANCE CONTROLS

Figure 29. Control Panel Window – Cells Tab View

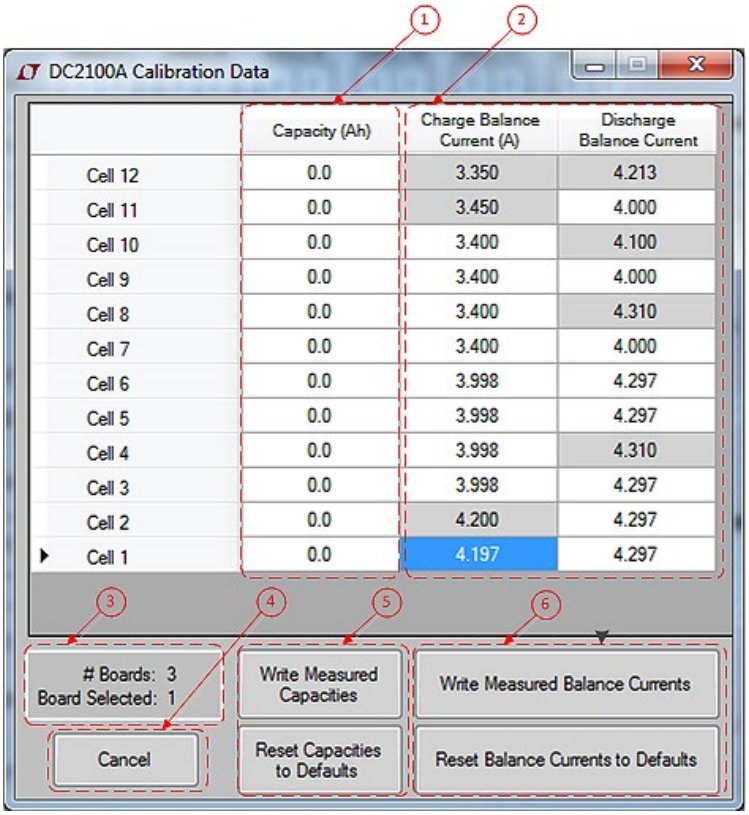
QUICK START PROCEDURE



1. SYSTEM TREE VIEW
2. BOARD STATUS LED
3. SELECTED BOARD INDICATOR
4. BOARD IDENTIFICATION DISPLAY
5. DATA DISPLAY TABS
6. FIRMWARE UPGRADE BUTTON
7. CALIBRATION DATA WINDOW BUTTON
8. EVENT LOG WINDOW BUTTON
9. GRAPH VIEW WINDOW BUTTON
10. DATA LOGGING CONTROLS
11. NOMINAL BALANCE CURRENTS DISPLAY
12. OVER AND UNDER VOLTAGE SETTING CONTROLS
13. CELL VOLTAGE DISPLAY GRID

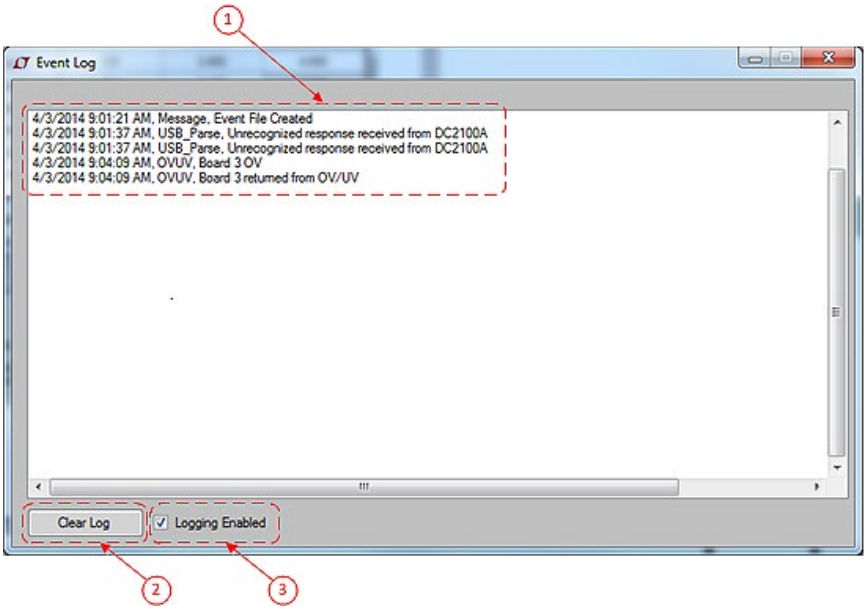
Figure 30. Control Panel Window – Global Channel Monitor View

QUICK START PROCEDURE



1. CELL CAPACITY DATA GRID
2. BALANCE CURRENT DATA GRID
3. SELECTED BOARD INDICATOR
4. CANCEL BUTTON
5. CELL CAPACITY CALIBRATION CONTROLS
6. BALANCE CURRENT CALIBRATION CONTROLS

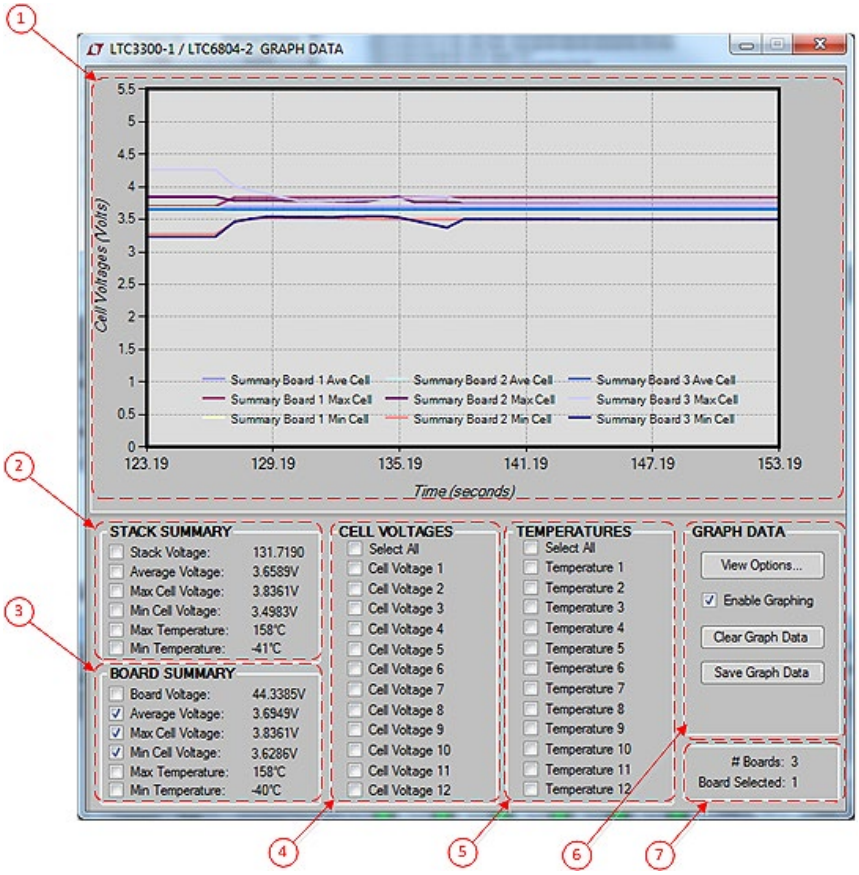
Figure 31. Calibration Data Window



1. EVENT LOG DATA
2. LOG CLEAR CONTROL
3. LOG FILE CONTROL

Figure 32. Event Log Window

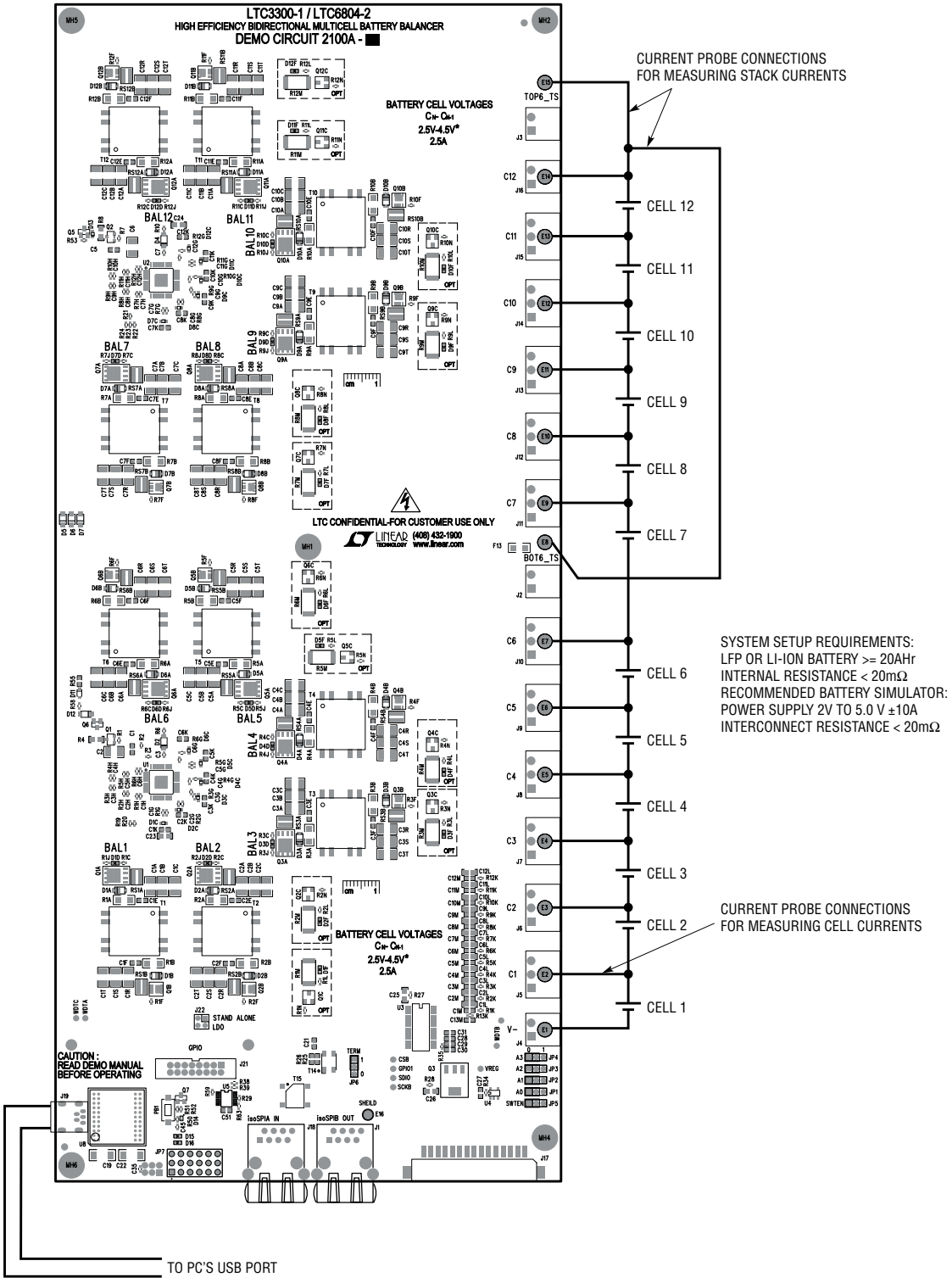
QUICK START PROCEDURE



1. GRAPH DISPLAY
2. STACK SUMMARY DATA SELECTION BOXES
3. BOARD SUMMARY DATA SELECTION BOXES
4. BOARD CELL VOLTAGE SELECTION BOXES
5. BOARD TEMPERATURE SELECTION BOXES
6. GRAPH DATA CONTROLS
7. SELECTED BOARD INDICATOR

Figure 33. Graph View Window

QUICK START PROCEDURE



NOTE: ALL CONNECTIONS FROM EQUIPMENT SHOULD BE KELVIN CONNECTED DIRECTLY TO THE BOARD PINS WHICH THEY ARE CONNECTED TO ON THIS DIAGRAM AND ANY INPUT, OR OUTPUT, LEADS SHOULD BE TWISTED PAIR, WHERE POSSIBLE.

Figure 34. Proper Measurement Equipment Setup for Bi-Directional Cell Balancer

QUICK START PROCEDURE

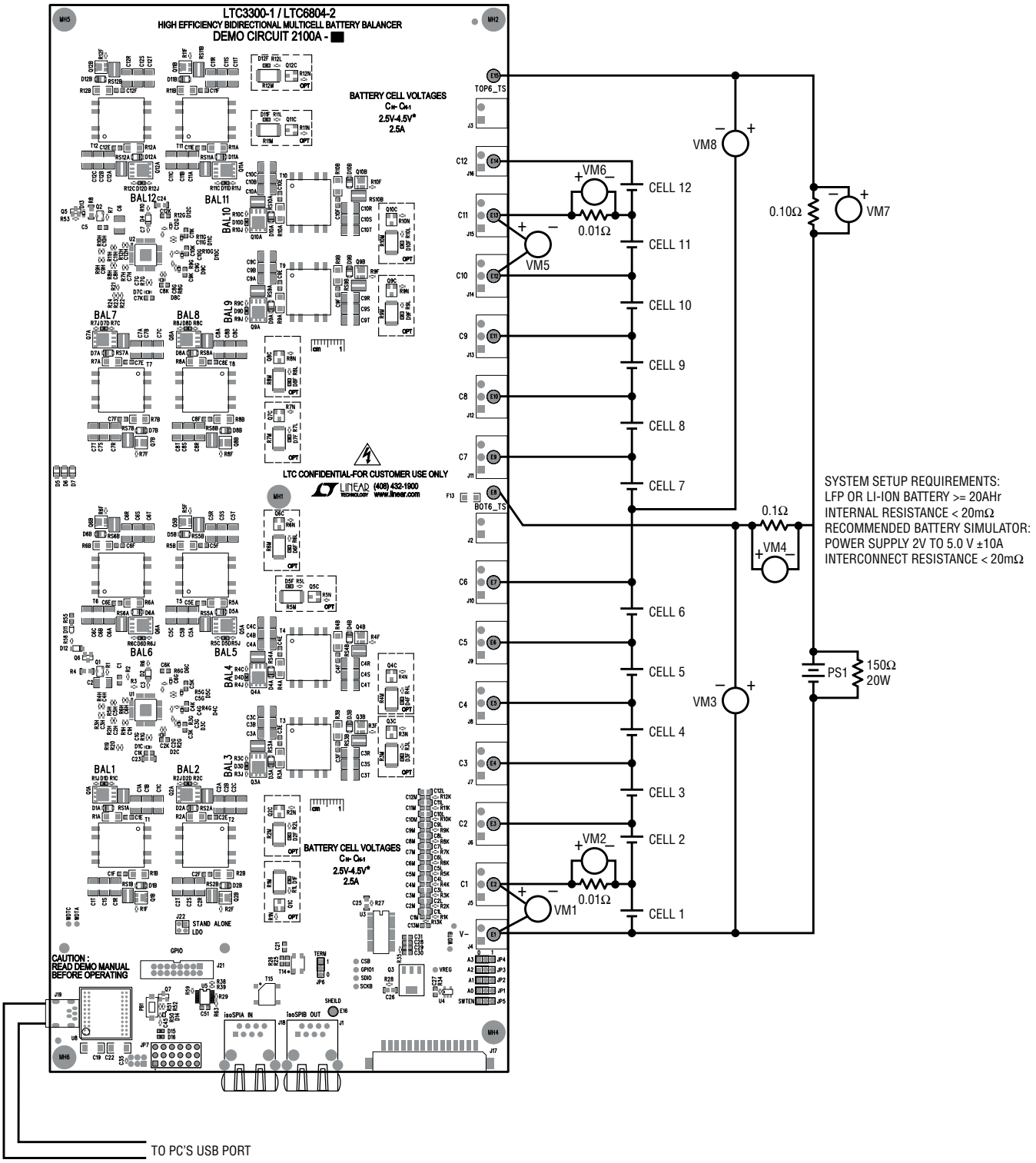


Figure 35. Proper Equipment Setup for Cell Balancer Efficiency Measurements

QUICK START PROCEDURE

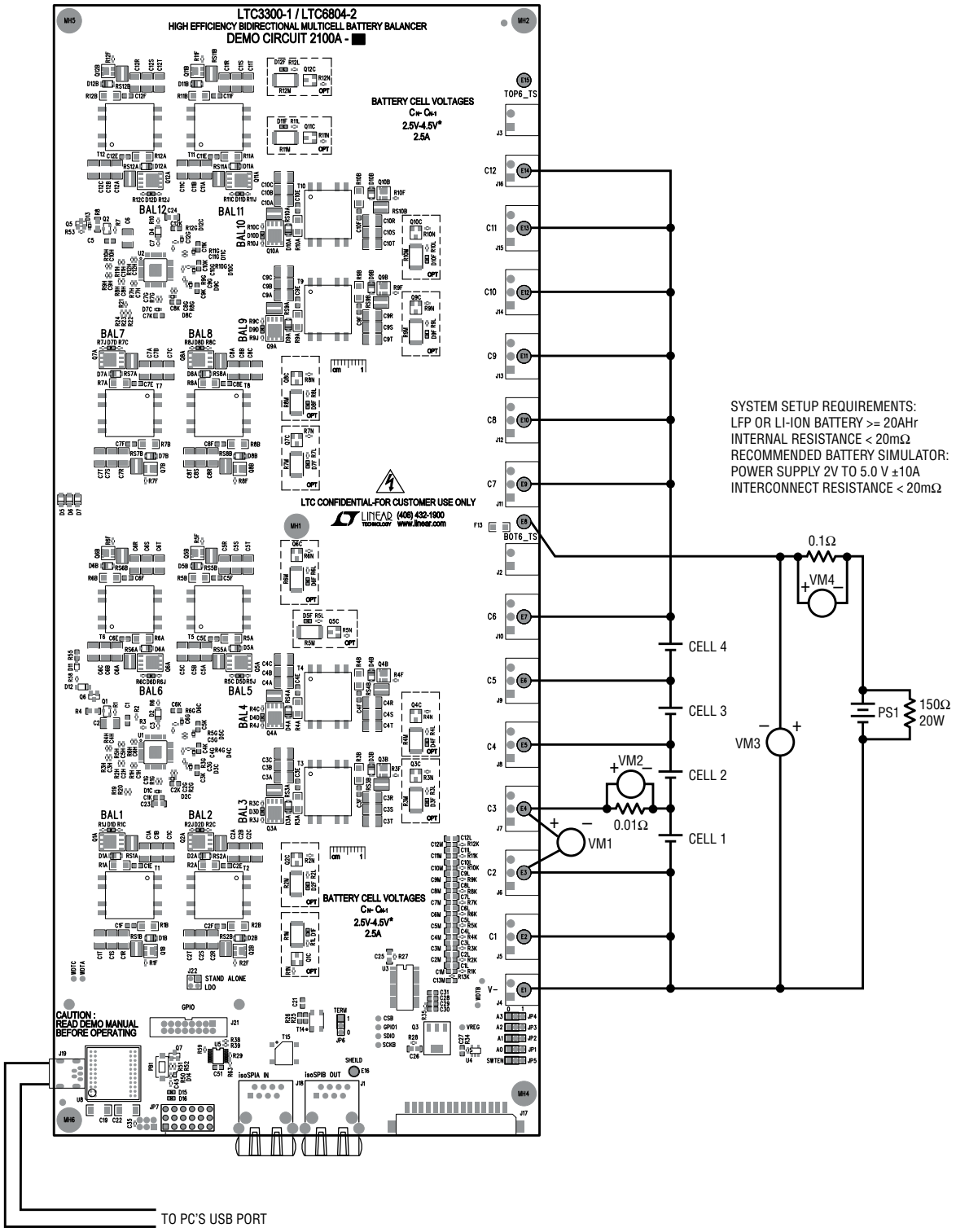


Figure 36. Proper Equipment Setup for Minimum Number (4) of Cell Efficiency Measurements

QUICK START PROCEDURE

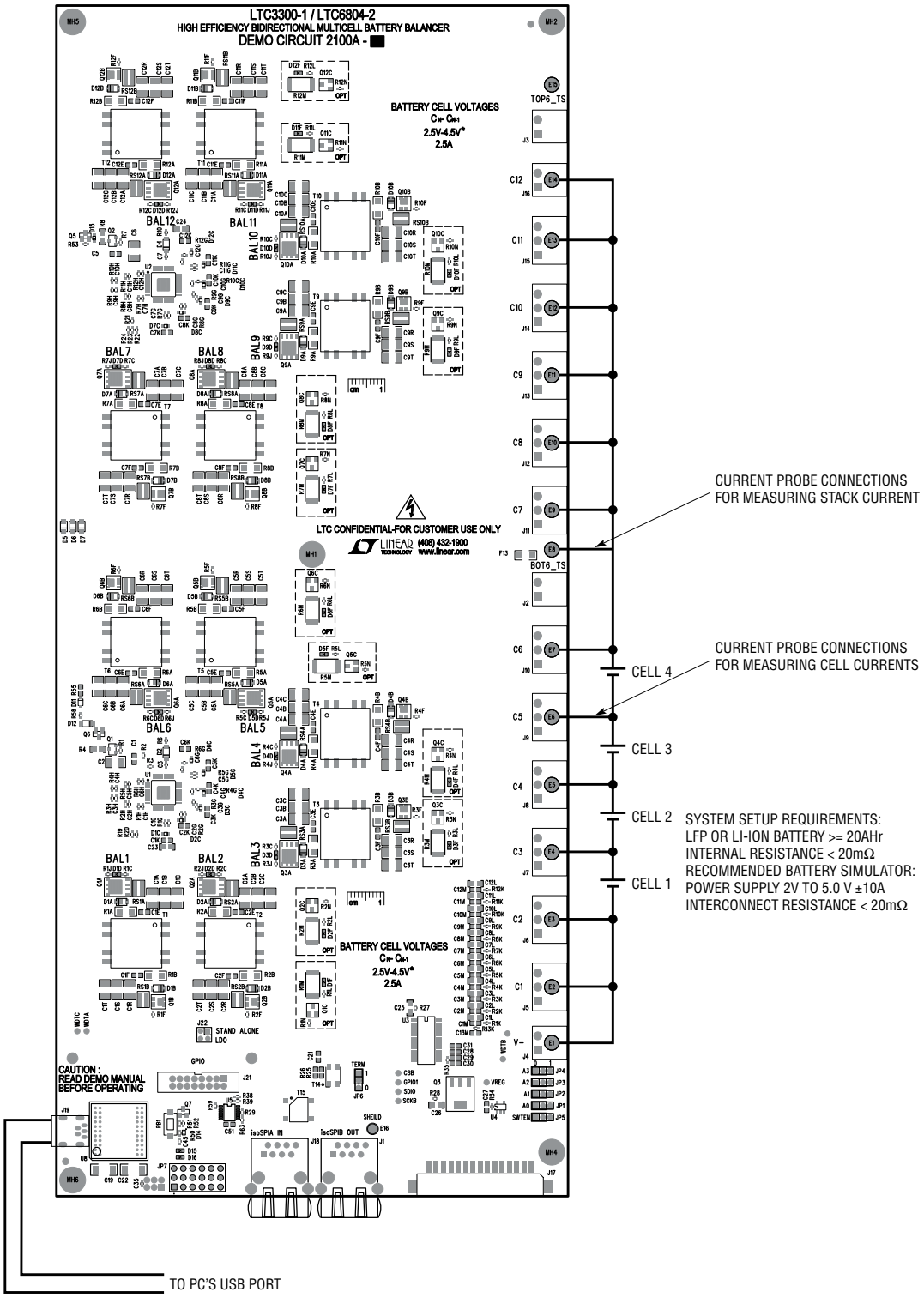


Figure 37. Configuring the Board for 4 Cells

QUICK START PROCEDURE

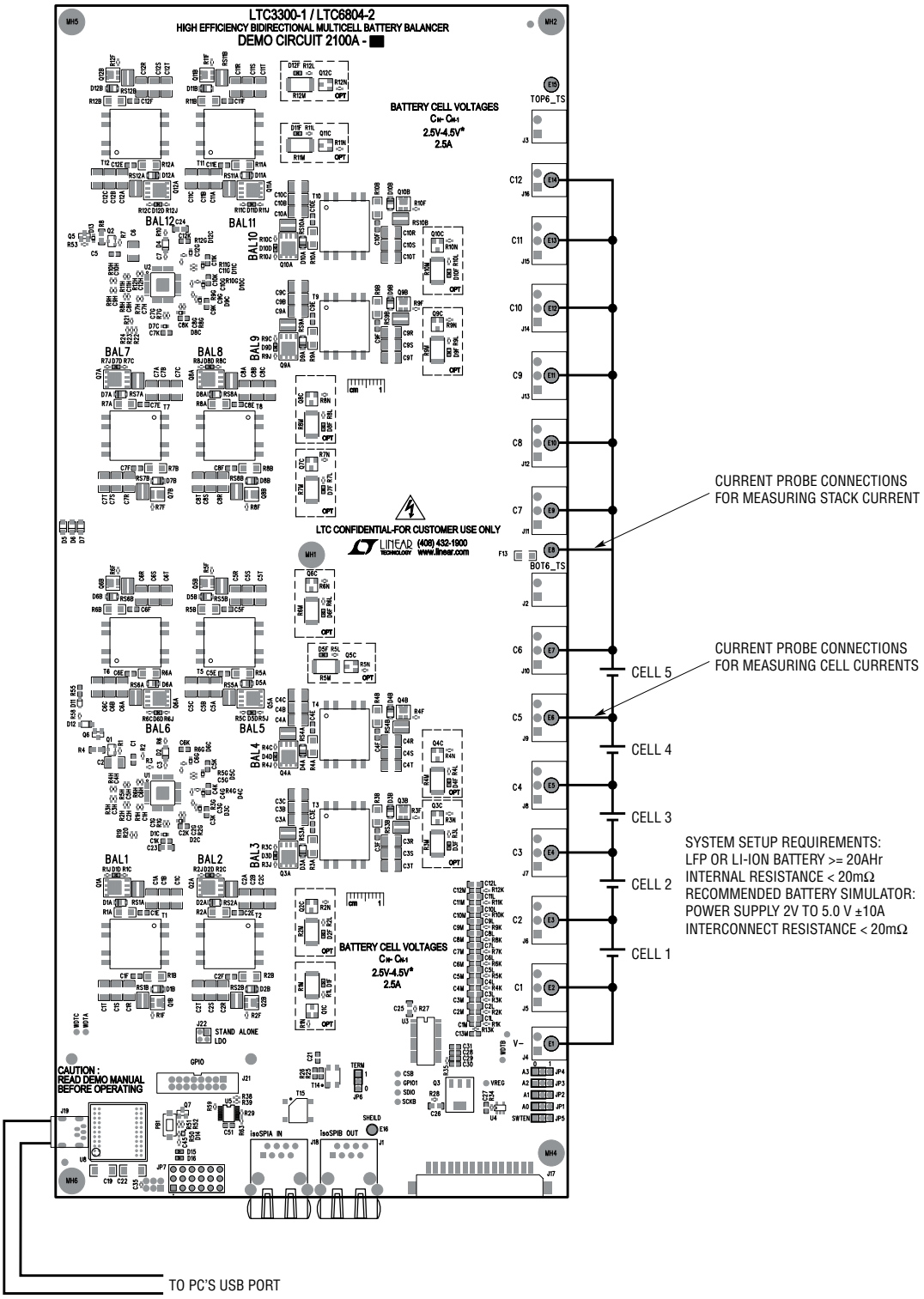


Figure 38. Configuring the Board for 5 Cells

QUICK START PROCEDURE

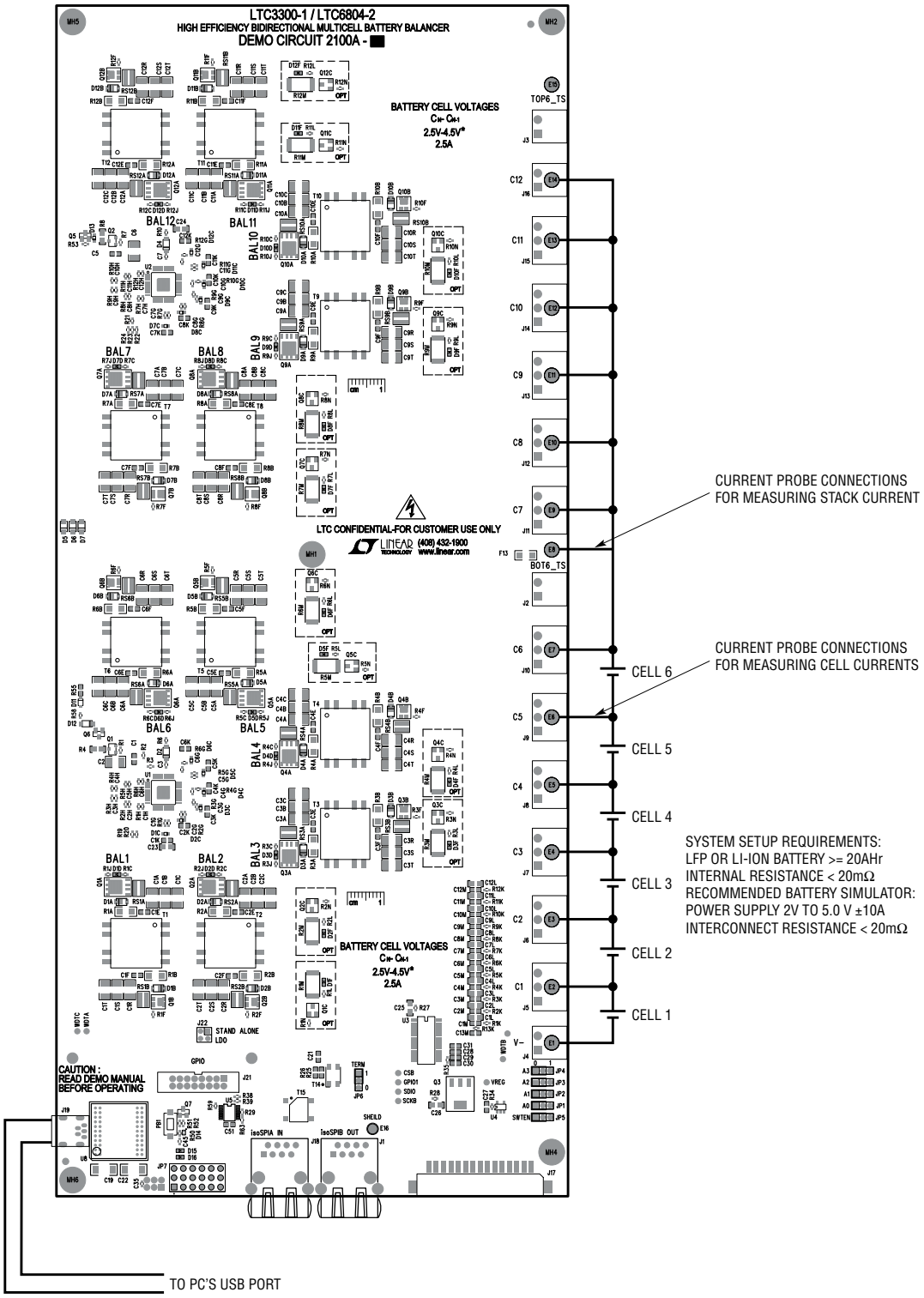


Figure 39. Configuring the Board for 6 Cells

QUICK START PROCEDURE

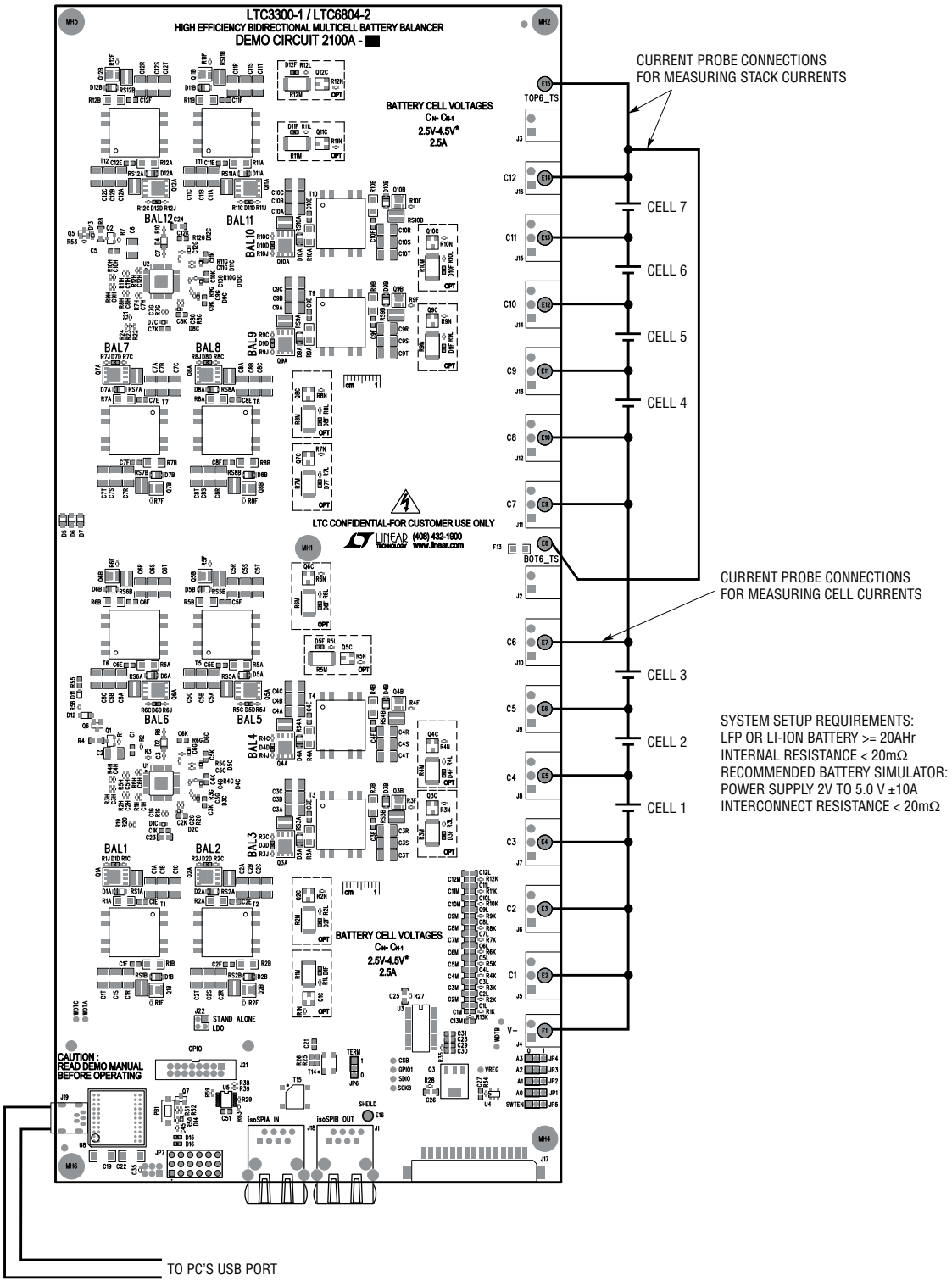


Figure 40. Configuring the Board for 7 Cells

QUICK START PROCEDURE

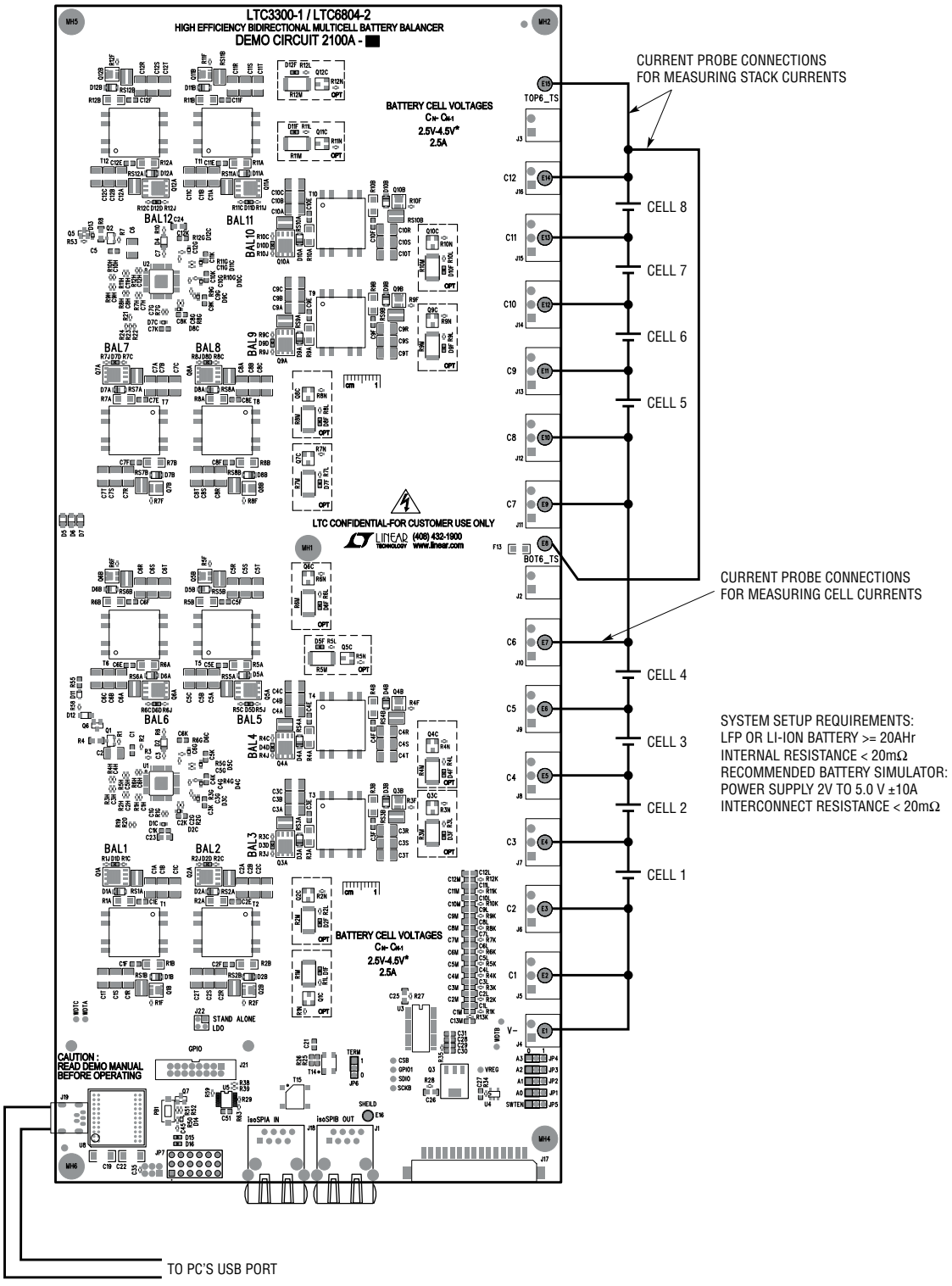


Figure 41. Configuring the Board for 8 Cells

QUICK START PROCEDURE

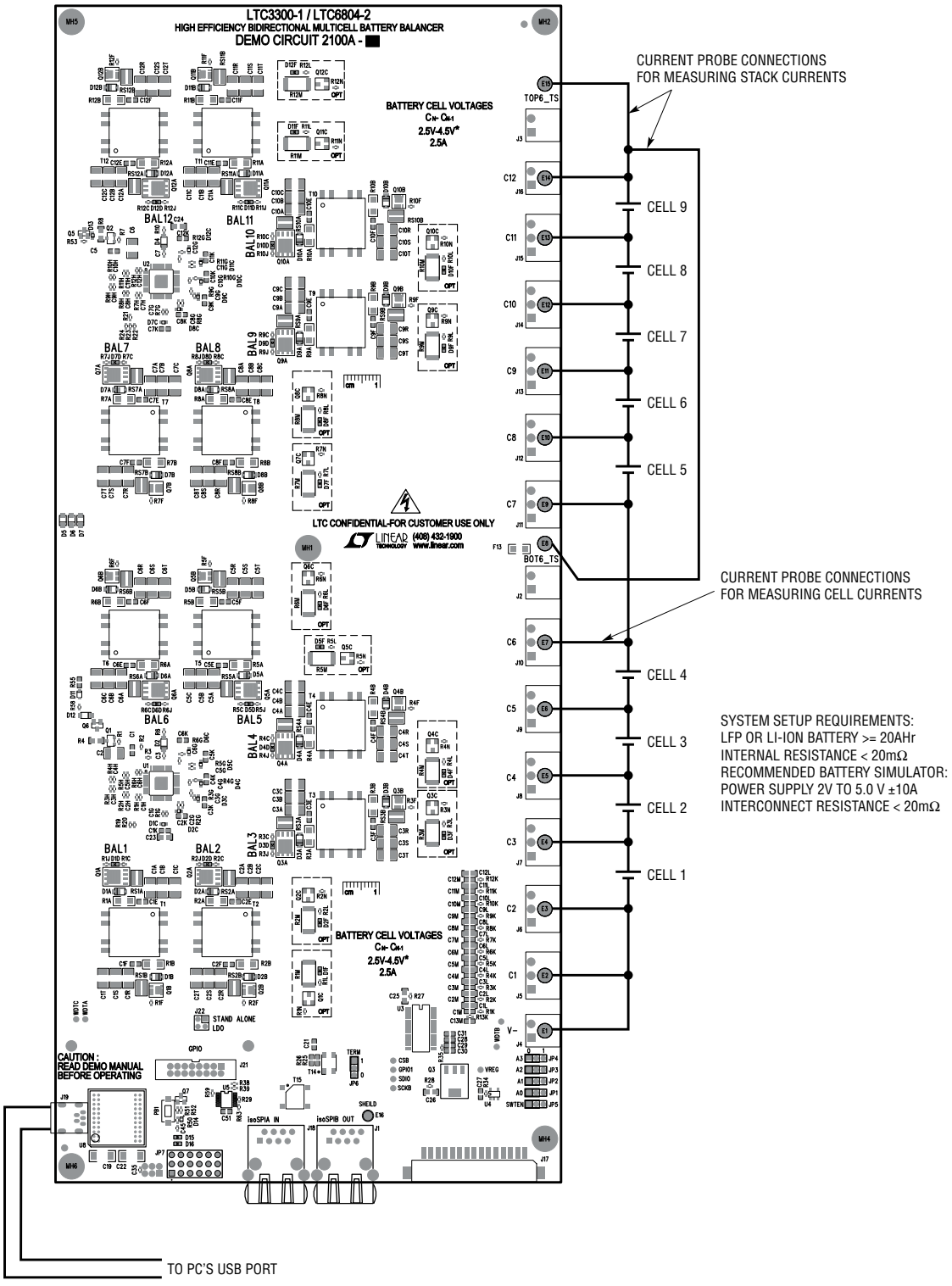


Figure 42. Configuring the Board for 9 Cells

QUICK START PROCEDURE

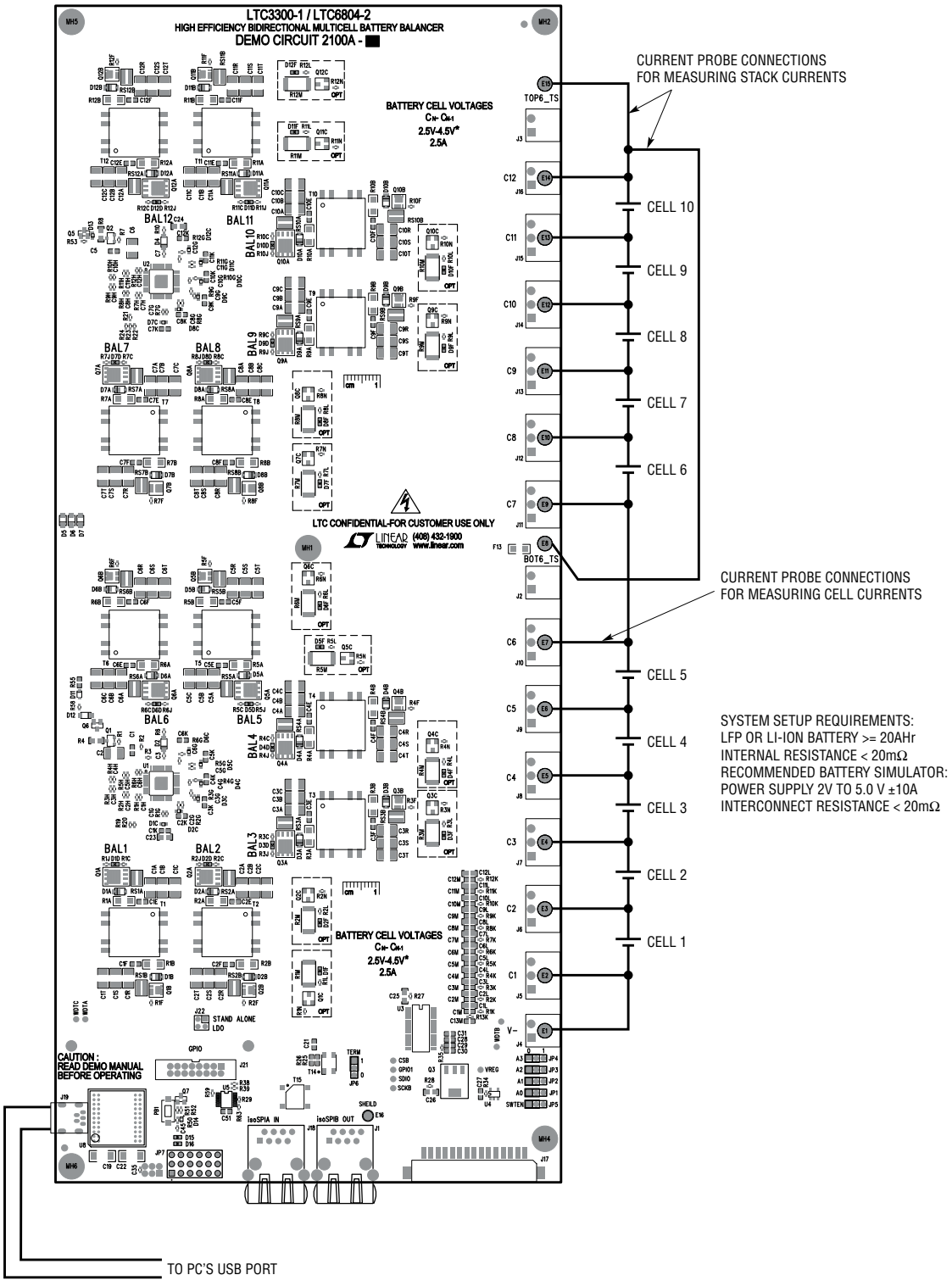


Figure 43. Configuring the Board for 10 Cells

QUICK START PROCEDURE

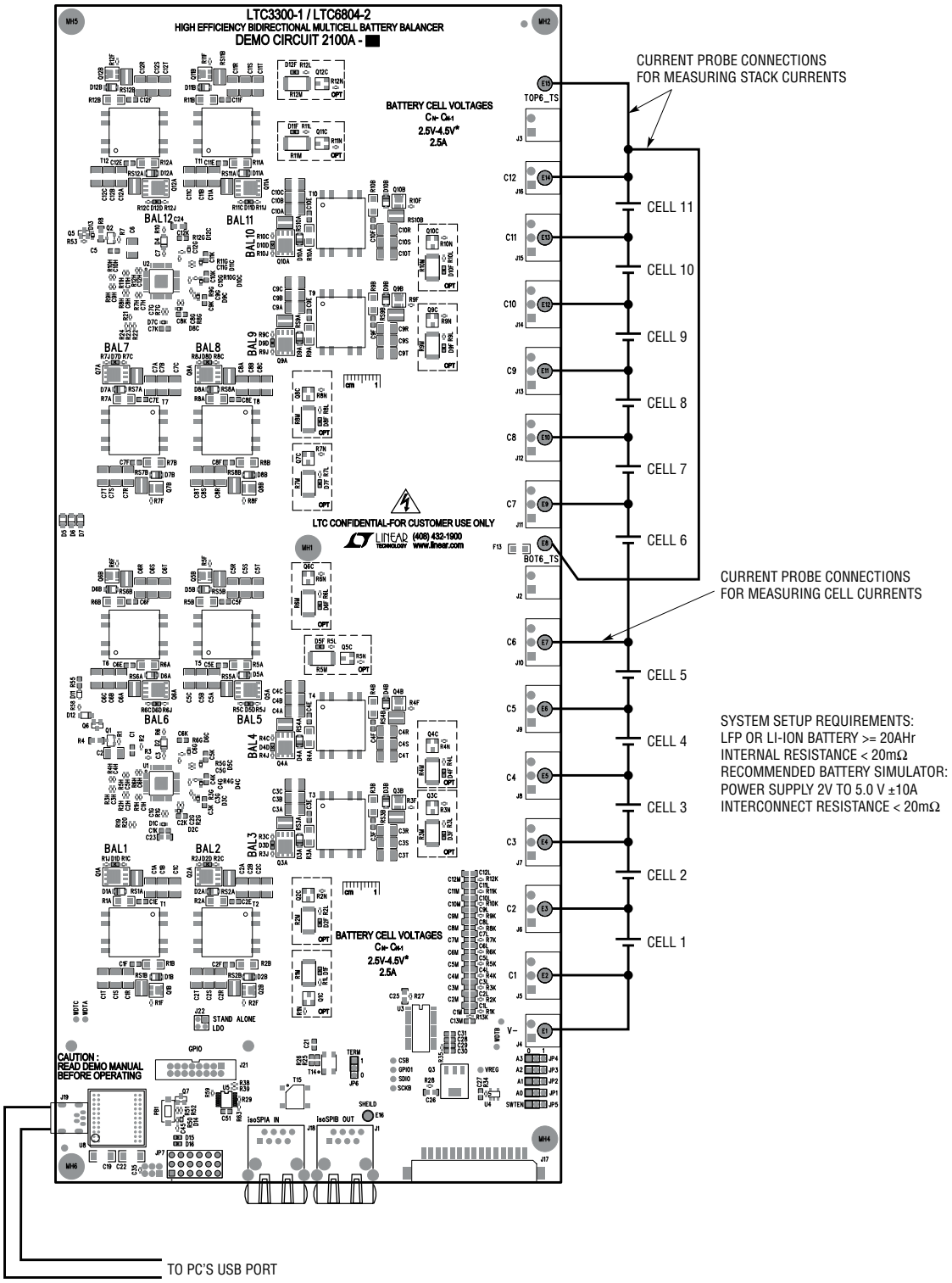
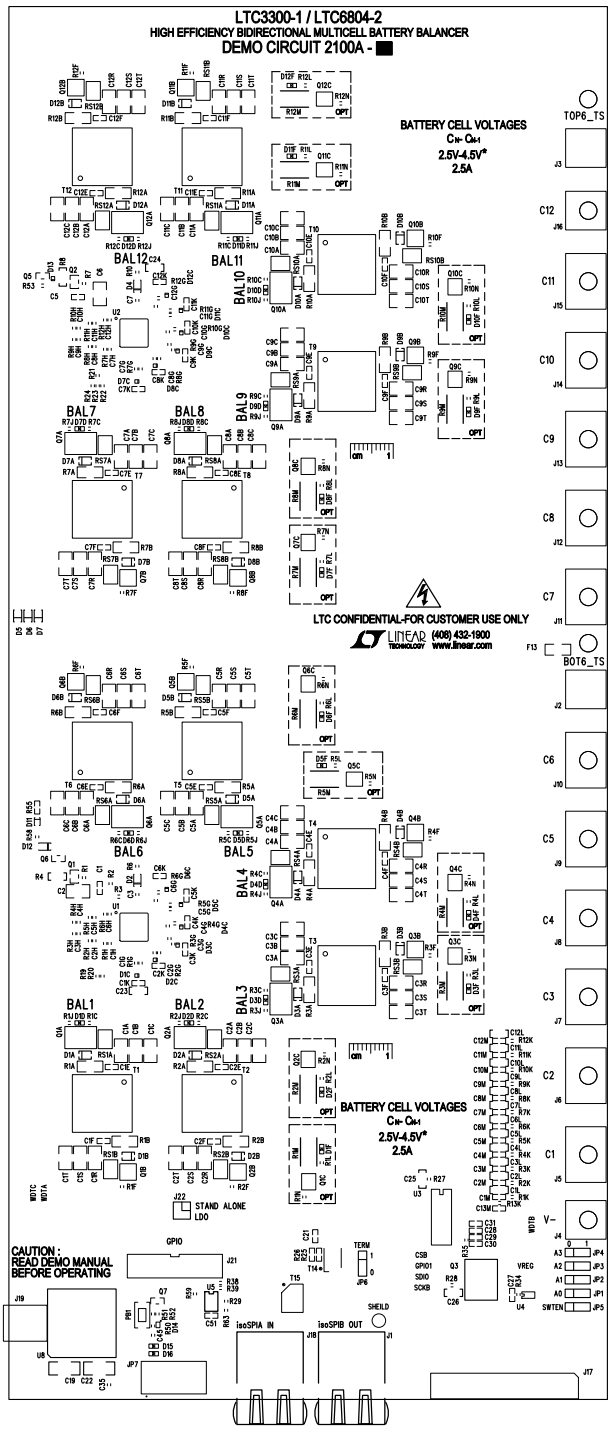
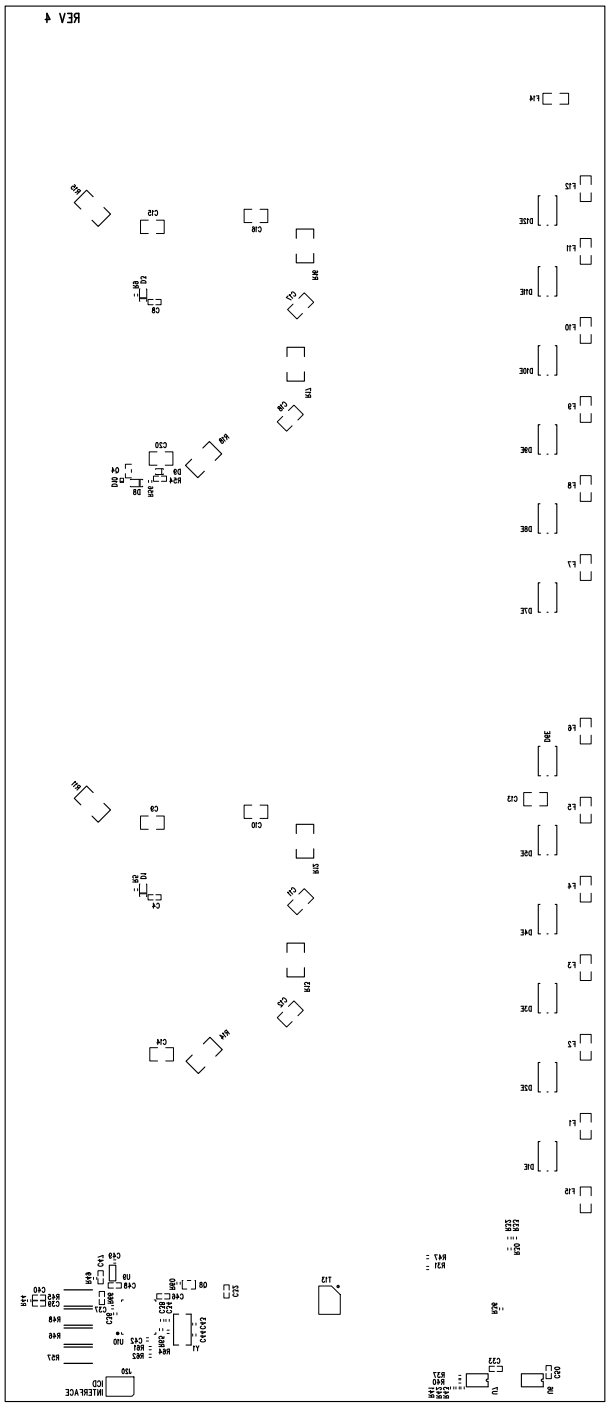


Figure 44. Configuring the Board for 11 Cells

PCB LAYOUT

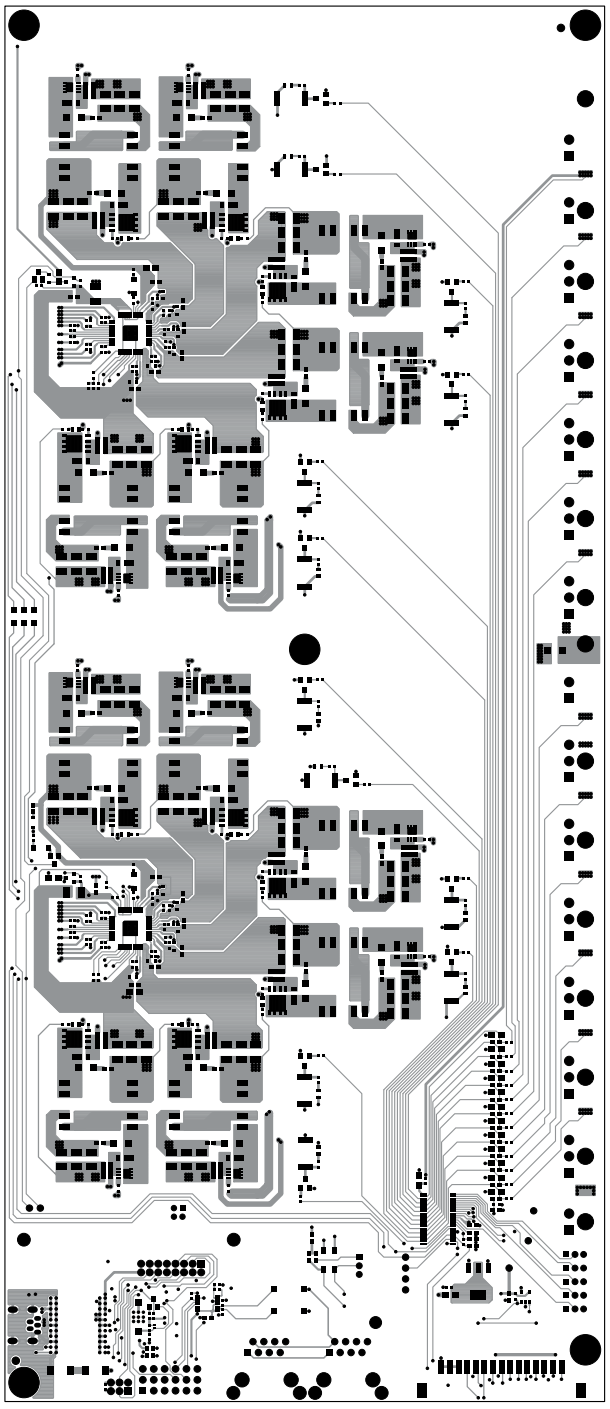


Top Silk Screen

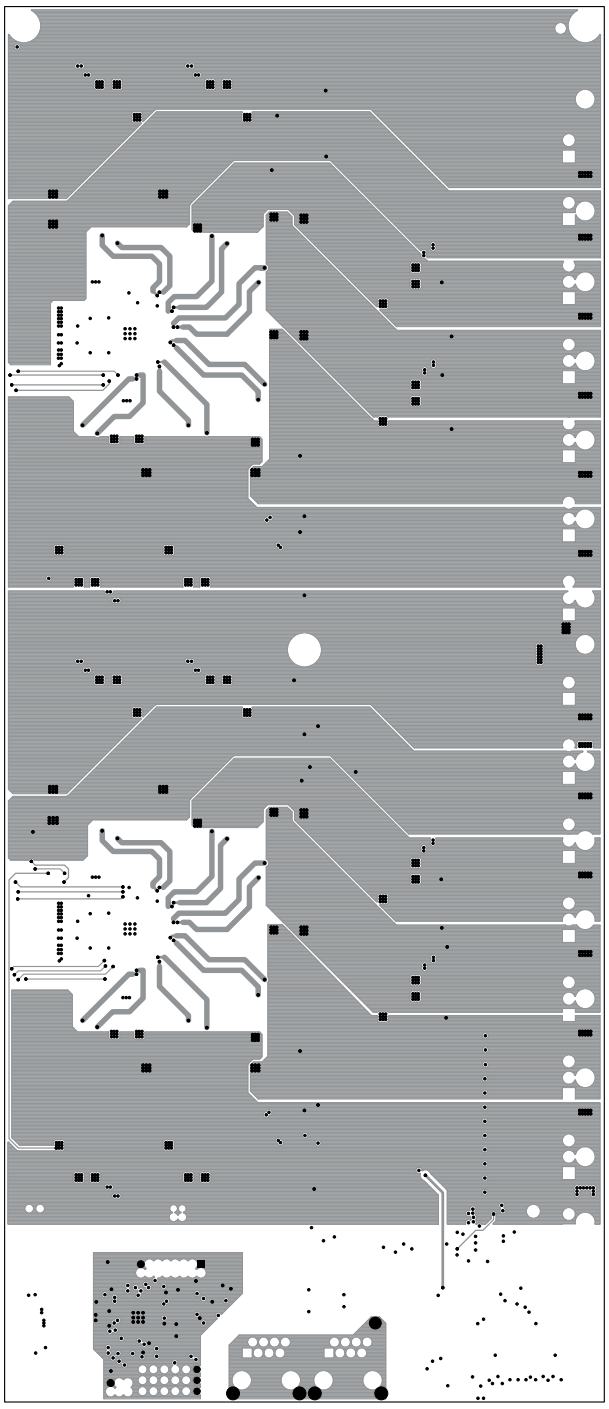


Bottom Silk Screen

PCB LAYOUT

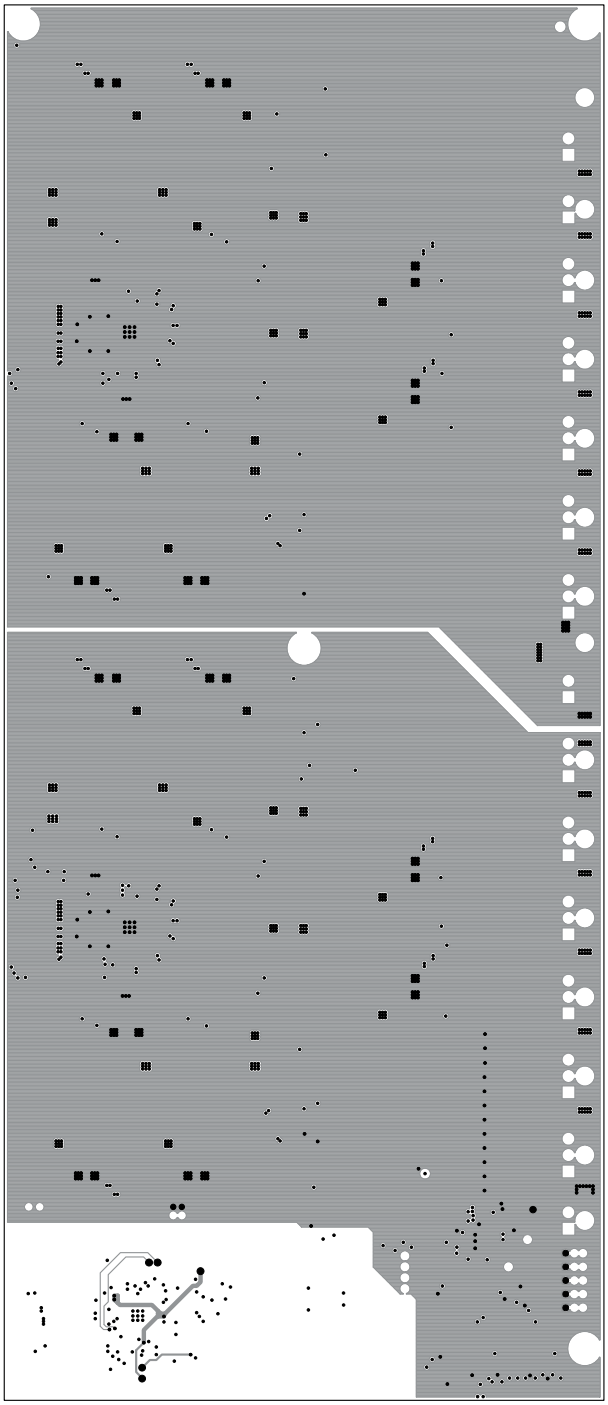


Layer 1

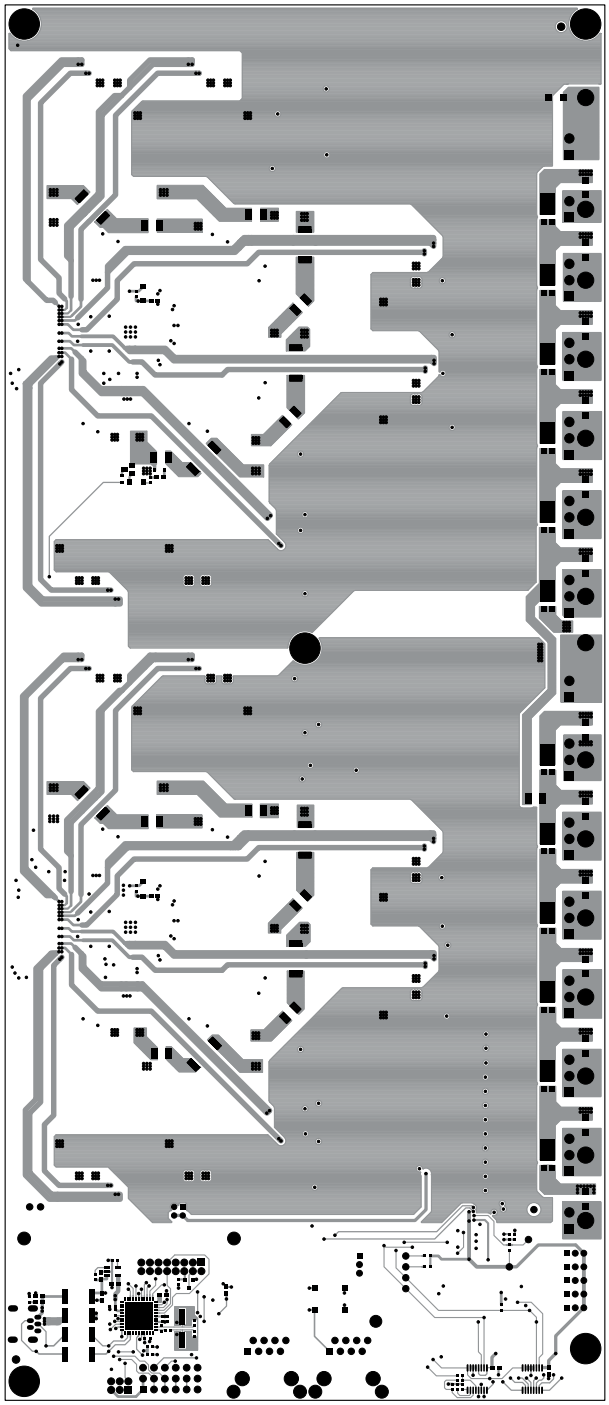


Layer 2

PCB LAYOUT



Layer 3



Layer 4

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	24	C1A-C12A, C1B-C12B	CAP.,X5R, 100µF, 6.3V, 20%, 1210	MURATA, GRM32ER60J107ME20L
2	24	C1E-C12E, C1F-C12F	CAP.,X7R, 470PF, 100V, 10%, 0603	AVX, 06031C471KAT2A
3	12	C1G-C12G	CAP.,X7R, 2200PF, 50V, 10%, 0402	MURATA, GRM155R71H222KA01D
4	12	C1H-C12H	CAP.,X7R, 470PF, 50V, 10%, 0402	MURATA, GRM155R71H471KA01D
5	13	C1M-C13M	CAP.,X7R, 0.01µF, 25V,10%, 0603	MURATA, GRM188R71E103KA01D
6	12	C1R-C12R	CAP.,X7R, 2.2µF, 100V,10%, 1210	MURATA, GRM32ER72A225KA35L
7	14	C1, C5, C1K-C12K	CAP.,X7R, 1.0µF, 16V,10%, 0603	MURATA, GRM188R71C105KA12D
8	13	C2, C6, C9-C18, C20	CAP.,X5R, 4.7µF, 16V,10%, 1206	MURATA, GRM31CR71C475KA01L
9	2	C3, C7	CAP, X7R, 0.1µF, 16V, 10% 0402	MURATA, GRM155R71C104KA88D
10	2	C4, C8	CAP.,X7R, 0.22µF, 16V,10%, 0603	TDK, C1608X7R1C224K
11	2	C19, C22	CAP., X7R, 470PF, 250VAC, 10%, 1808	MURATA, GA342QR7GF471KW01L
12	2	C23, C24	CAP.,X7R, 10µF, 10V,10%, 0805	MURATA, GRM21BR71A106K51L
13	2	C25, C26	CAP., X7R, 0.1µF, 100V, 10%, 0805	AVX, 08051C104KAT2A
14	4	C27, C33, C50, C51	CAP.,X7R, 0.1µF, 25V,10%, 0603	MURATA, GRM188R71E103KA01D
15	3	C28, C29, C31	CAP.,X5R, 1µF, 25V,10%, 0603	TDK, C1608X5R1E105K
16	3	C30, C39, C46	CAP, X5R, 10µF, 6.3V, 20%, 0603	MURATA, GRM188R71C105KA12D
17	6	C34-C38, C45	CAP, X7R, 0.1µF, 16V, 20%, 0402	AVX, 0402YC104MAT2A
18	1	C42	CAP.X5R, 047µF, 16V, 10%, 0402	TDK, C1005X5R1A474K
19	2	C43, C44	CAP,C0G, 22PF, 50V, 0402	MURATA, GRM1555C1H220JZ01D
20	2	C47, C48	CAP, X5R, 1.0µF, 6.3V, 10%, 0603	TAIYO YUDEN, JMK105BJ105KV
21	12	D1E-D12E	DIODE, SBR,200, 10A, POWERDI5	DIODES INC, SBR10U200P5-13
22	4	D1-D4	SMD, SCHOTTKY	CENTRAL SEMI, CMMSH2-40
23	3	D5-D7	SMD, SILICON SWITCHING DIODE	VISHAY, RS07J
24	2	D8, D12	SMD, SILICON ZENER, 5.1V	CENTRAL SEMI, CMHZ4689
25	2	D10, D13	SMD, SCHOTTKY, 70V	CENTRAL SEMI, CMOD6263 TR
26	2	D9, D11	DIODE, ZENER 5.6V, 400MW, SOD323	PHILIPS, PDZ5.6B
27	1	D14	DIODE, SWITCHING, 1.0mm × 0.6mm DFN2	DIODES INC, 1N4448HLP
28	25	D1D-D12D, D1F-D12F, D15	LED,GREEN, CLEAR 0603 SMD	LITE-ON, LTST-C190KGKT
29	1	D16	LED, YELLOW ORANGE CLEAR 0603 SMD	LITE-ON, LTST-C190KFKT
30	13	F1-F12, F15	SMD, FUSE, 12.0A, FAST ACTING, 1206	BUSSMANN, 3216FF12-R
31	2	F13, F14	SMD, FUSE, 7.0A, FAST ACTING, 1206	BUSSMANN, 3216FF7-R
32	1	J1	CONN MOD JACK R/A 8P8C SHIELDED RJ45	WÜRTH, 615008140121
33	1	J19	USB, B RECEPTACLE, RT, SMT	WÜRTH, 651005136521
34	1	J20	HEADER, 2mm, 2 × 3 TH HEADER	WÜRTH, 62000621121
35	1	J21	HEADER, 2mm, 2 × 8 TH HEADER	WÜRTH, 62501621621
36	1	J22	HEADER, 2mm, 2 × 2, TH HEADER	MOLEX, 87831-0420
37	1	PB1	SWITCH TACTILE SPST-NO 0.05A 12V	WÜRTH, 434111025826
38	12	R1A-R12A	RES, CHIP, 20Ω, 1/4W, 5%,1206	VISHAY, CRCW120620R0JNEA
39	12	R1B-R12B OPT	RES, CHIP,18Ω, 1/4W, 5%, 1206	VISHAY, CRCW120618R0JNEA
40	24	R1C-R12C, R1F-R12F	RES, CHIP, 5.1Ω, 1/16W, 5%, 0402	VISHAY, CRCW04025R10JNED
41	24	R1G-R12G, R1H-R12H	RES, CHIP, 20Ω, 1/16W, 5%, 0402	VISHAY, CRCW040220R0JNED

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
42	14	R1J-R12J, R56, R58	RES, CHIP, 2.0k, 1/16W, 5%, 0402	VISHAY, CRCW04022K00JNED
43	16	R1K-R13K, R27, R28, R37	RES, CHIP, 100Ω, 1/16W, 5%, 0402	VISHAY, CRCW0402100RJNED
44	12	R1L-R12L	RES, CHIP, 470Ω, 1/16W, 5%, 0402	VISHAY, CRCW0402470RJNED
45	12	R1M-R12M	RES, CHIP, 33Ω, 1W, 5%, 2512	VISHAY, CRCW251233R0JNEG
46	12	R1N-R12N	RES, CHIP, 3.3k, 1/16W, 5%, 0402	VISHAY, CRCW04023K30JNED
47	1	R2	RES, CHIP, 0Ω, JUMPER, 1/16W, 5%, 0402	VISHAY, CRCW04020000Z0ED
48	2	R4, R8	RES, CHIP, 1.27M, 1/8W, 1%, 0805	VISHAY, CRCW08051M27FKED
49	2	R6, R10	RES,CHIP, 6.81Ω, 1/16W, 1%, 0402	VISHAY, CRCW04026R81FKED
50	8	R11-R18	RES, CHIP, 0Ω, 2512	VISHAY, CRCW25120000Z0EG
51	3	R19, R21, R24	RES, CHIP, 23.7k, 1/16W, 1%, 0402	VISHAY, CRCW040223K7FKED
52	2	R20, R22	RES, CHIP, 33.2K, 1/16W, 1%, 0402	VISHAY, CRCW040233K2FKED
53	2	R25, R26	RES, CHIP, 60.4Ω, 1/10W, 1%, 0603	VISHAY, CRCW060360R4FKED
54	2	R29, R63	RES, CHIP, 60.4Ω, 1/16W, 1%, 0402	VISHAY, CRCW040260R4FKED
55	4	R30, R31, R40, R41	RES, CHIP, 1.00M, 1/16W, 5%, 0402	VISHAY, CRCW04021M00JNED
56	2	R32, R39	RES, CHIP, 1.40k, 1/16W, 1%, 0402	VISHAY, CRCW04021K40JKED
57	2	R33, R38	RES, CHIP, 604Ω, 1/16W, 1%, 0402	VISHAY, CRCW0402604RJKED
58	5	R34, R36, R47, R61, R62	RES, CHIP, 2.0k, 1/16W, 5%, 0402	VISHAY, CRCW04022K00JNED
59	1	R35	RES, CHIP, 10k, 1/16W, 1%, 0402	VISHAY, CRCW040210K0FKED
60	6	R42, R43, R50-R52, R60	RES, CHIP, 10.0k, 1/16W, 5%, 0402	VISHAY, CRCW040210K0JNED
61	1	R44	RES, CHIP, 1.0Ω, 1/16W, 5%, 0402	VISHAY, CRCW04021R00JNED
62	1	R49	RES, CHIP, 1.0k, 1/16W, 5%, 0402	VISHAY, CRCW04021K00JNED
63	1	R53	RES, CHIP, 100k, 1/16W, 1%, 0402	VISHAY, CRCW0402100KFKED
64	2	R54, R55	RES, CHIP, 20Ω, 1/10W, 5%, 0603	VISHAY, CRCW060320R0JNEA
65	1	R59	RES, CHIP, 5.1k, 1/16W, 5%, 0402	VISHAY, CRCW04025K10JNED
66	1	R64	RES, CHIP, 2.49k, 1/16W, 1%, 0402	VISHAY, CRCW04022K49FKED
67	1	R65	RES, CHIP, 1.00M, 1/16W, 1%, 0402	VISHAY, CRCW04021M00FKED
68	1	R66	RES, CHIP, 301, 1/10W, 1%, 0603	VISHAY, CRCW0603301RFKED
69	12	RS1A-RS12A	RES, CHIP, 5mΩ, 1W, 1%, 1206	SUSUMU, PRL1632-R005-F
70	12	RS1B-RS12B	RES, CHIP, 10mΩ, 1W, 1%, 1206	SUSUMU, PRL1632-R010-F
71	12	Q1A-Q12A	MOSFET, 100V, 0.0087Ω, 60A, POWERPAK-SO8	VISHAY, SiR882ADP-GE3
72	12	Q1B-Q12B	MOSFET, 100V, 0.058Ω, 25A, POWERPAK-1212-8	VISHAY, SiS892ADN-GE3
73	12	Q1C-Q12C	MOSFET, P-CHANNEL 30V, 80MΩ, MPAK	INFINEON, BSS308PEH6327XT
74	2	Q1, Q2	MOSFET, 100V, 10Ω, SOT-323	DIODES INC, BSS123W-7-F
75	1	Q3	TRANS. NPN, 180V, 0.6A, SOT-223	CENTRAL SEMI, CZT5551
76	1	Q4	TRANS, PNP, 60V, SOT-23	CENTRAL SEMI, CMPT3906E
77	1	Q5	MOSFET, P-CHANNEL 50V, 4Ω, SOT-23	CENTRAL SEMI, CMPDM8002A
78	2	Q6, Q7	TRANS, NPN, 60V, SOT-23	CENTRAL SEMI, CMPT3904E
79	1	Q8	MOSFET, 100V, 10Ω, SOT-323	DIODES INC, BSS123W
80	12	T1-T12	TRANSFORMER, 1:1, 3.0µH, 10.8A	WÜRTH, 750312504
81	1	T13, T15	TRANSFORMER, ISOLATION	PULSE ENG., PE-68386NLT
82	1	T14	IND., CHOKE COM MODE 22µH, 1.2kΩ SMD	TDK, ACT458-220-2P-TL003

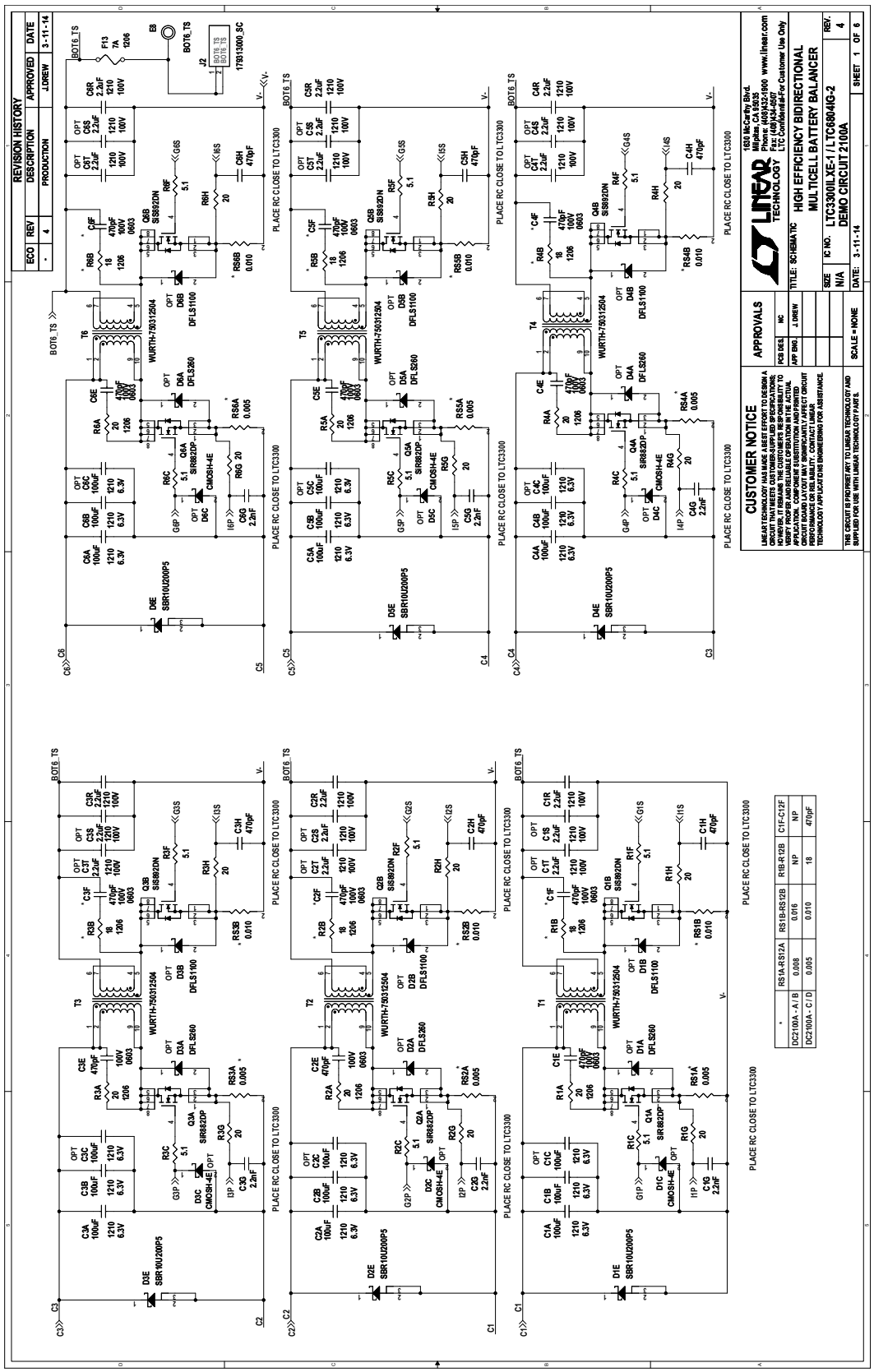
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
83	2	U1, U2	IC,SMT, BI-DIRECTIONAL BATTERY BALANCER	LINEAR, LTC3300ILXE-1#PBF
84	1	U3	IC,SMT, BATTERY MONITOR	LINEAR, LTC6804IG-2#PBF
85	1	U4	IC,SMT, 24AA64	MICROCHIP TECH. 24AA64T-I/OT
86	1	U5	IC,SMT, isospi ISOLATED COMM. INTERFACE	LINEAR, LTC6820IMS#PBF
87	2	U6, U7	IC,SMT, 8-CHANNEL MUX, SSOP-16	LINEAR, LTC1380CGN#PBF
88	1	U8	MODULE, USB ISOLATOR	LINEAR, LTM2884CY#PBF
89	1	U9	IC,SMT, MICRO POWER VLDO, 3.3V, SOT23-5	LINEAR, LT1761ES5-3.3#PBF
90	1	U10	14-Bit uc w/usb, 8mm × 8mm QFN44	MICROCHIP, PIC18F47J53-I/ML
91	1	Y1	12MHz CRYSTAL	ECS INC, ECS-120-20-3X
Components and Hardware for Demo Board Only				
1	15	E1-E15	TURRET, 0.09"	MIL-MAX, 2501-2-00-80-00-00-07-0
2	1	J17	HEADER, SMD, 1 × 15, TIN PLATED, RT ANGLE	HIROSE, DF3DZ-15P-2(21)
3	6	JP1-JP6	HEADER, 3PINS, 2mm	WÜRTH, 62000311121
4	6	JP1-JP6	SHUNT 2mm	WÜRTH, 60800213421
5	1	JP7	HEADER, 2.54mm, 3 × 6 THT VERT 18POS	SAMTEC, TSW-106-07-L-T
6	1	JP7(mate)	JP7 JUMPER BOARD	LINEAR, DC2100-ASSY-1
7	1	J17(mate)	DC2100A THERMISTOR BOARD	LINEAR, DC2100A - THERM-1
8	10		STAND-OFF HEX, NYL 8/32 THR 0.25" L	KEYSTONE, 1904A
9	10		SCREW, PAN PHILLIPS 8-32 1/4 NYL	B&F FASTENER, NY PMS 8320025PH
Optional Components				
1	0	C1C-C12C	CAP., X5R, 100µF, 6.3V, 10%, 1210	MURATA, GRM32ER60J107ME20L
2	0	C1S-C12S, C1T-C12T	CAP., X7R, 2.2µF, 100V, 10%, 1210	MURATA, GRM32ER72A225KA35L
3	0	C1L-C12L OPT	CAP, OPT, 100V, 0805	
4	0	C21, C32 OPT	CAP., X7R, 100PF, 100V, 10%, 0603	AVX, 06031C101KAT
5	0	C40 OPT	CAP, X5R, 10µF, 6.3V, 20% 0603	MURATA, GRM188R60J106ME47D
6	0	C49	CAP, OPT, 16V, 0402	
7	0	D1A-D12A OPT	DIODE, SCHOTTKY 2.0A 60V HI EFFICIENCY	DIODES INC, DFLS260-7
8	0	D1B-D12B OPT	DIODE, SCHOTTKY 100V 1A BARRIER RECTIFIER POWERDI123	DIODES INC, DFLS1100-7
9	0	D1C-D12C OPT	SMD, SCHOTTKY	CENTRAL SEMI, CMOSH-4E
10	0	R1, R7 OPT	RES, CHIP, 1.00M, 1/16W, 5%, 0402	VISHAY, CRCW04021M00JNED
11	0	R3, R5, R9, R23 OPT	RES, CHIP, 0Ω, 0402	VISHAY, CRCW04020000Z0ED
12	0	R45, R46, R48, R57 OPT	RES, CHIP, 0Ω, 2512	VISHAY, CRCW25120000Z0EF
13	0	J2, J3, J4, J16 OPT	HEADER 1 × 2	WEIDMULLER, 179313000_SC
14	0	J2, J3, J4, J16 (mate) OPT	SOCKET 1 × 2	WEIDMULLER, 1792770000
15	0	J5-J15 OPT	HEADER, 1 × 3	WEIDMULLER, 179314000_SC
16	0	J5-J15 (mate) OPT	SOCKET, 1 × 3	WEIDMULLER, 1792780000

PARTS LIST

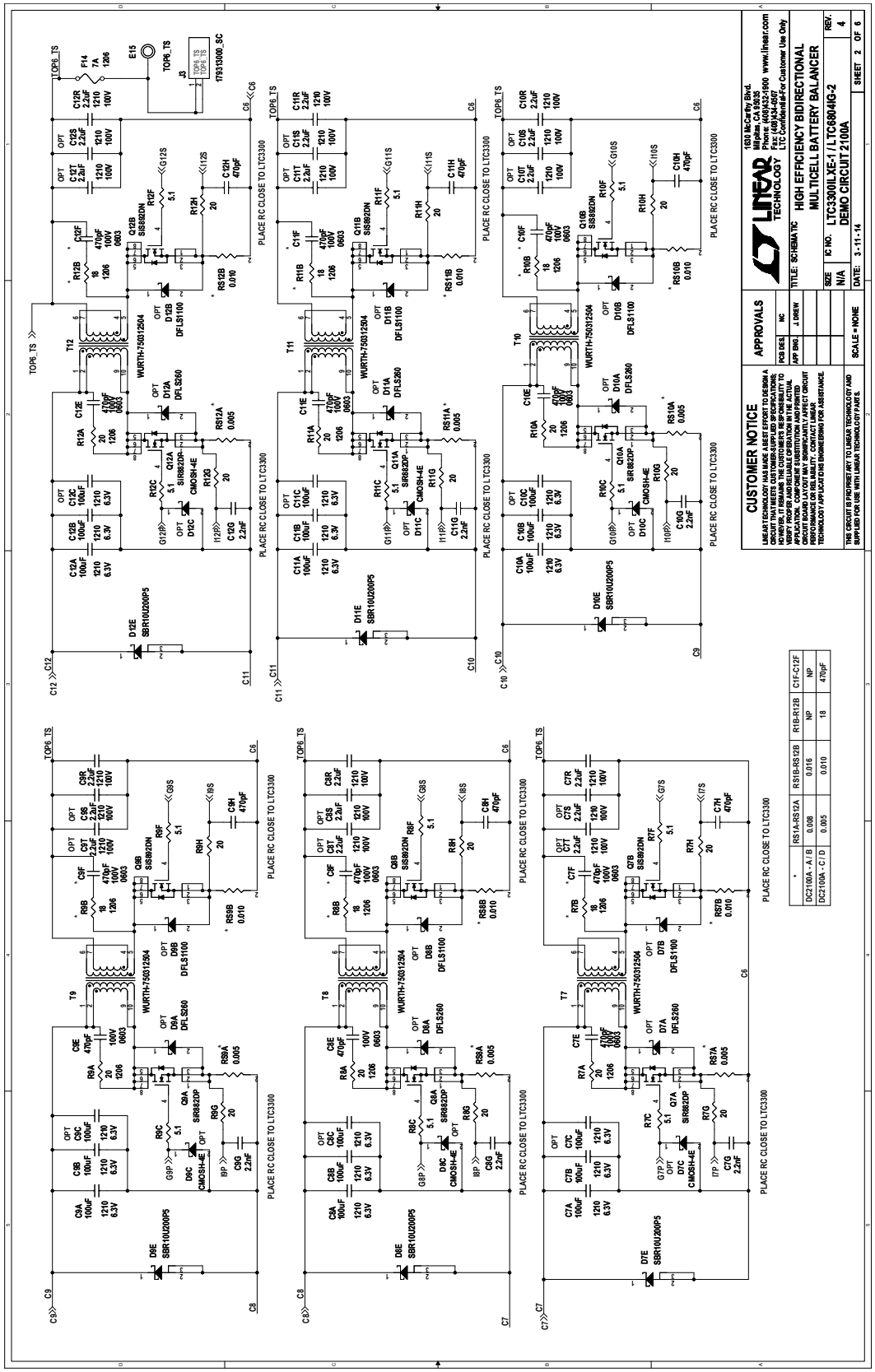
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Thermistor Board				
1	1	J1	CONN RECEPT 15POS 2MM VERT TIN	HIROSE, DF3-15S-2DSA(25)
2	1	R1	RES, CHIP, 340k, 1/16W, 1%, 0402	VISHAY, CRCW0402340KFKED
3	1	R2	RES, CHIP, 54.9k, 1/16W, 1%, 0402	VISHAY, CRCW040254K9FKED
4	1	R3	RES, CHIP, 20k, 1/16W, 1%, 0402	VISHAY, CRCW040220K0FKED
5	1	R4	RES, CHIP, 8.06k, 1/16W, 1%, 0402	VISHAY, CRCW04028K06FKED
6	1	R5	RES, CHIP, 5.36k, 1/16W, 1%, 0402	VISHAY, CRCW04025K36FKED
7	1	R6	RES, CHIP, 3.65k,1/16W,1%, 0402	VISHAY, CRCW04023K65FKED
8	1	R7	RES, CHIP, 2.49k,1/16W,1%, 0402	VISHAY, CRCW04022K49FKED
9	1	R8	RES, CHIP, 1.24k,1/16W,1%, 0402	VISHAY, CRCW04021K24FKED
10	1	R9	RES, CHIP, 909Ω,1/16W,1%, 0402	VISHAY, CRCW0402909RFKED
11	1	R10	RES, CHIP, 681Ω,1/16W,1%, 0402	VISHAY, CRCW0402681RFKED
12	1	R11	RES, CHIP, 301Ω,1/16W,1%, 0402	VISHAY, CRCW0402301RFKED
13	1	R12	RES, CHIP, 147Ω,1/16W,1%, 0402	VISHAY, CRCW0402147RFKED
14	14	E1-E14	TURRET, 0.061 DIA	MILL MAX, 2308-2-00-80-00-00-07-0

SCHEMATIC DIAGRAM



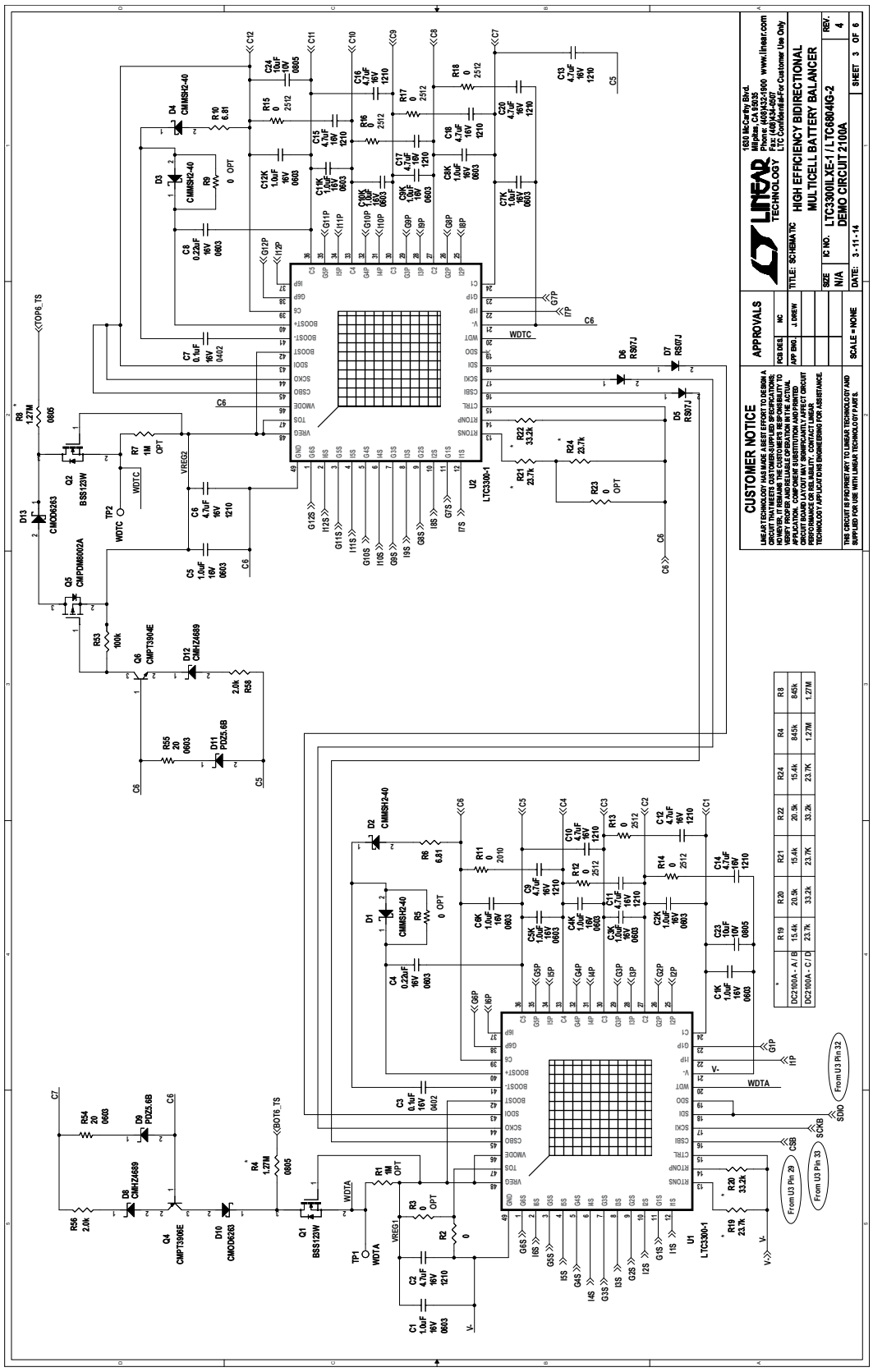
*	RS1A-RS12A	RS1B-RS12B	R1B-R12B	C1F-C12F
DC2100A - A / B	0.008	0.016	NP	NP
DC2100A - C / D	0.005	0.010	18	470pF

SCHEMATIC DIAGRAM



*	R51A-R52A	R51B-R52B	R1B-R12B	C1F-C12F
DC2100A - A / B	0.008	0.016	NP	NP
DC2100A - C / D	0.005	0.010	18	470pF

SCHEMATIC DIAGRAM



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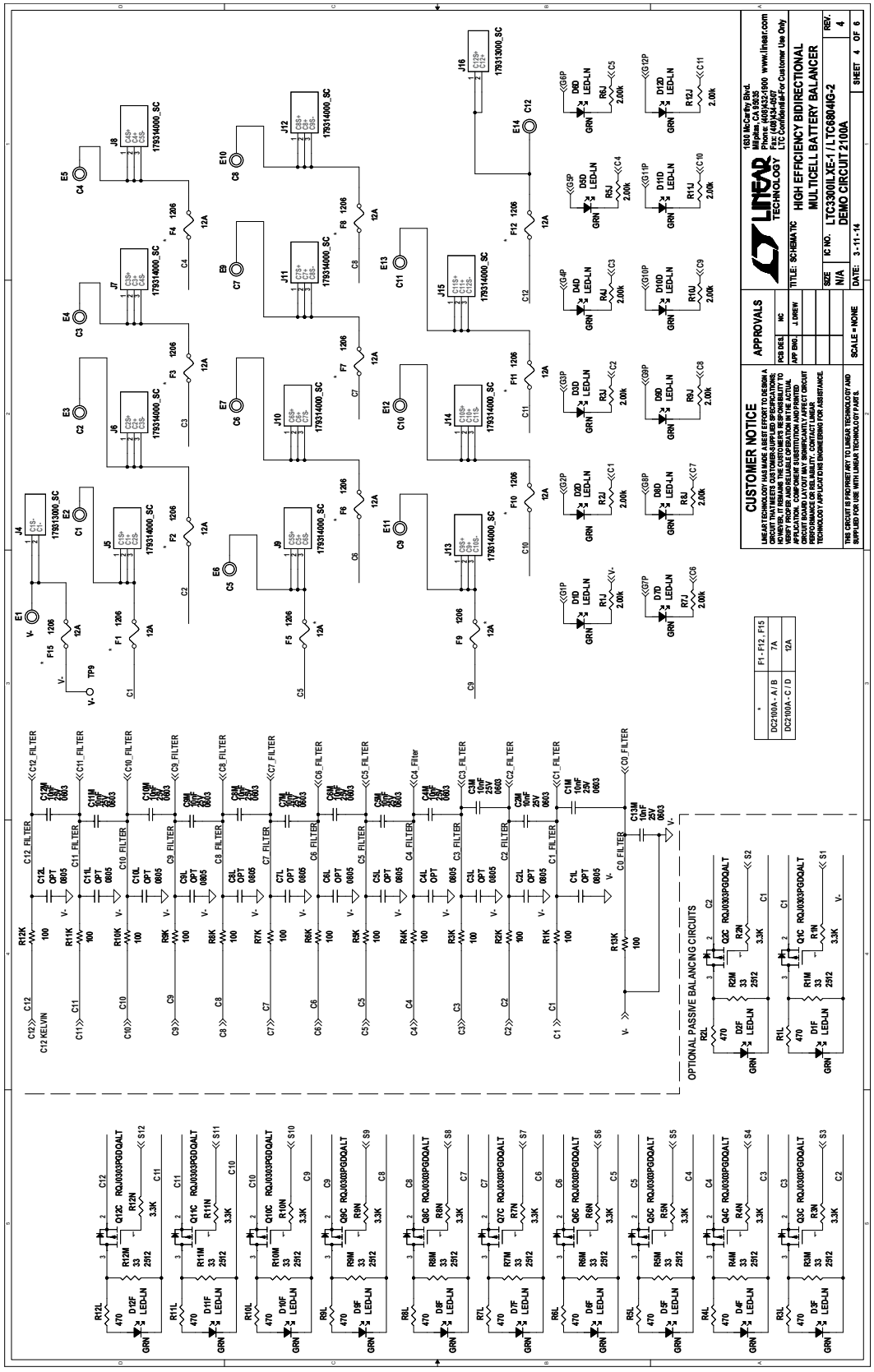

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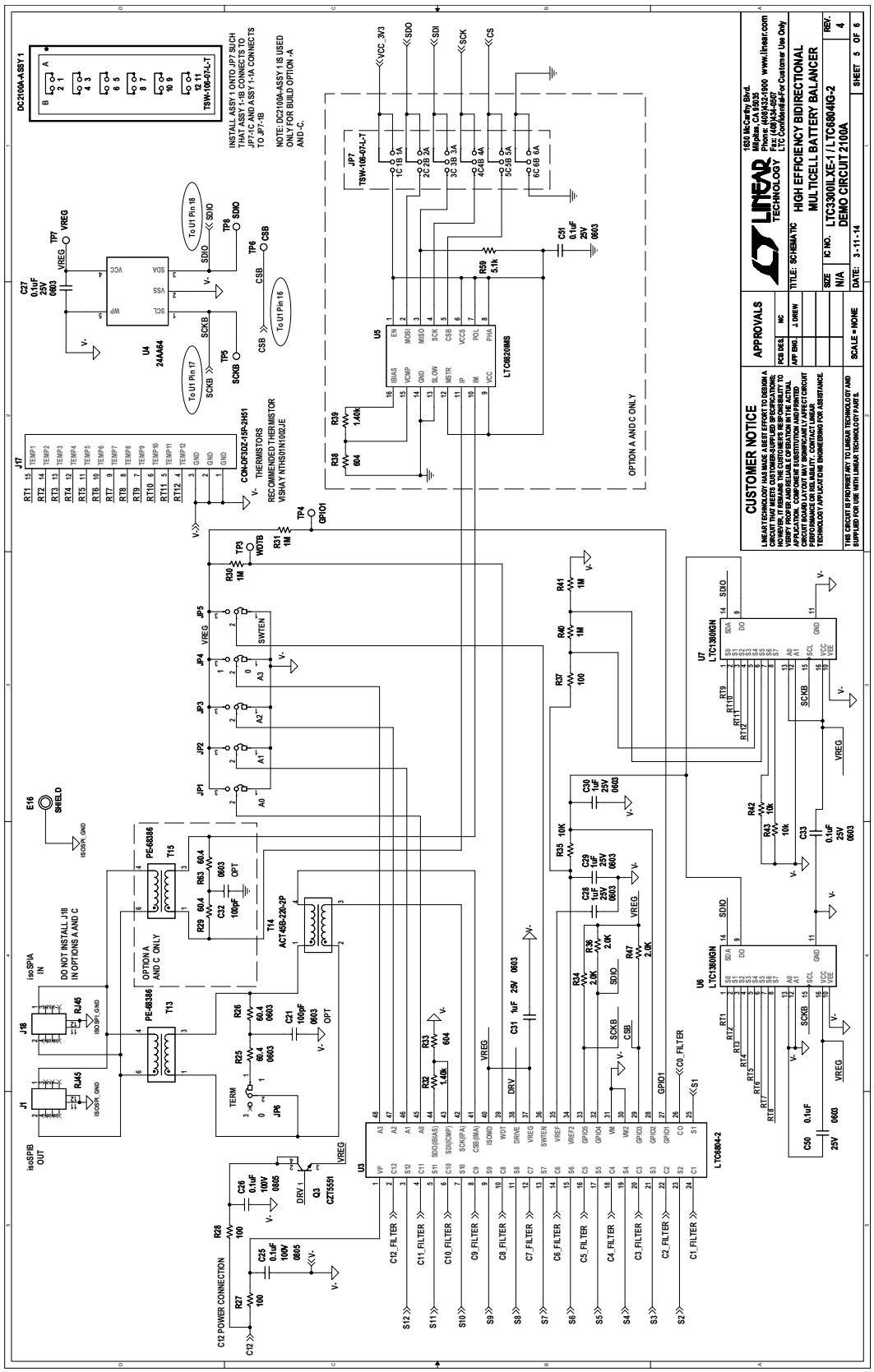

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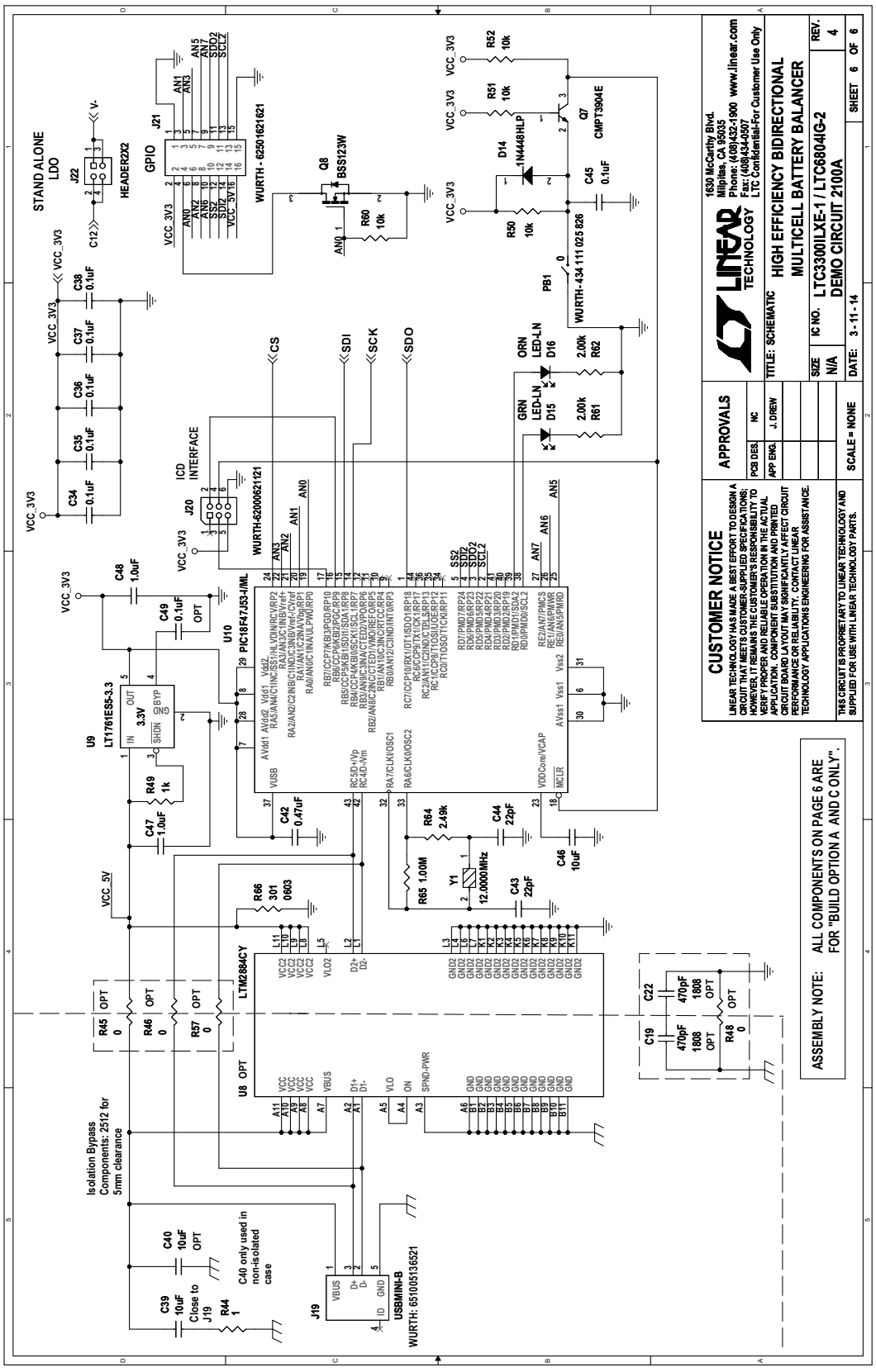

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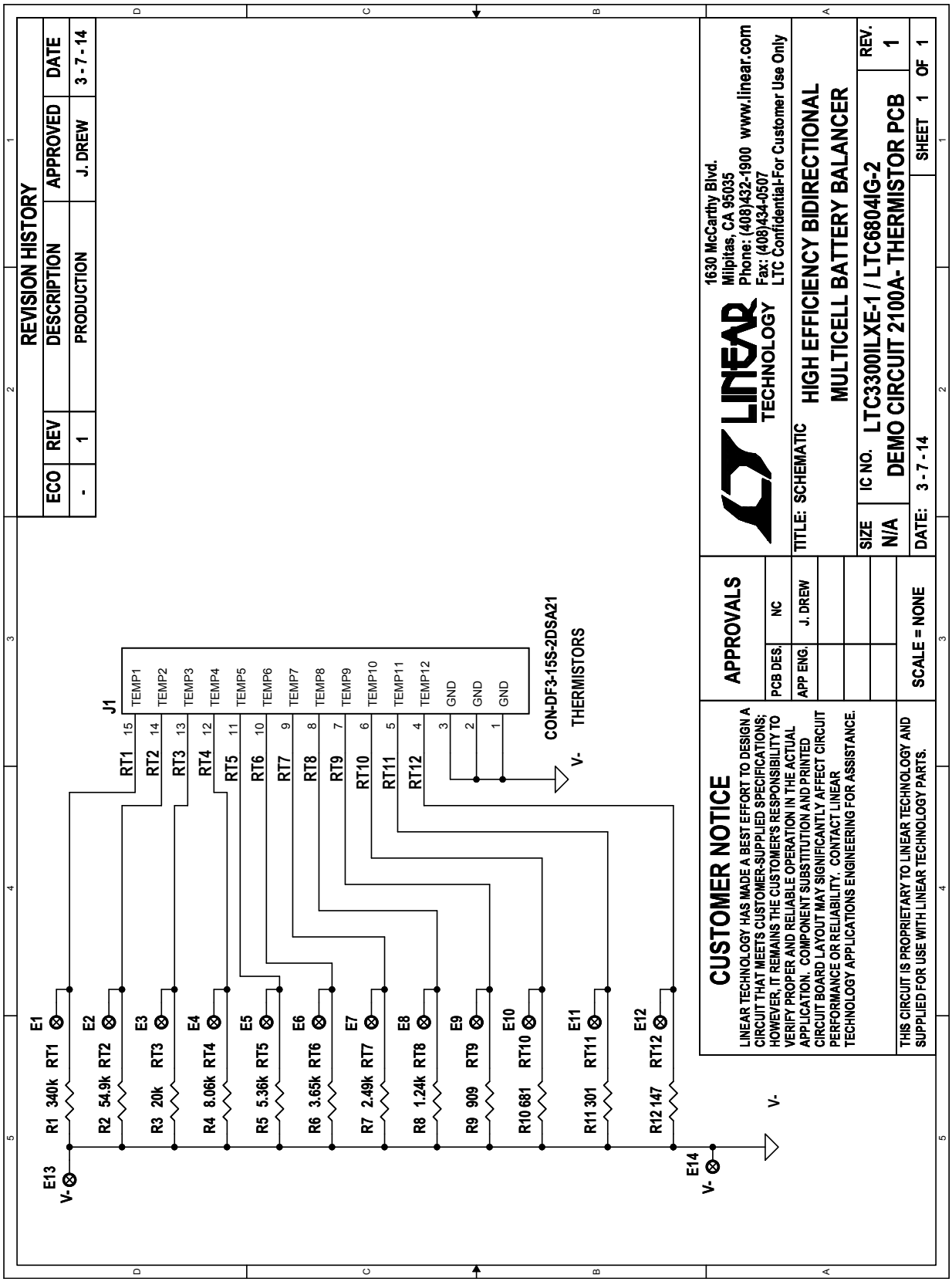
SCHEMATIC DIAGRAM



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