Ultrafast Frequency Switching Using a PLL

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Oftentimes, and specifically in wireless communications applications, the need arises for switching the output frequency of a PLL (phase-locked loop) synthesizer in a very short amount of time. In these cases, it is usually desirable to achieve a settled output frequency following a relatively large frequency jump in less than 20µs. In the following, we will discover how the LTC6946, an ultralow noise and spurious 0.37GHz to 6.39GHz integer-N PLL synthesizer with integrated VCO, can deliver such objectives.

To be more specific, let us pick the LTC6946 parameters such that its output is settled to within 10kHz from the final frequency in the shortest amount of time possible for 20MHz frequency steps. For this example, we can use a comparison frequency (phase-frequency detector frequency, or f_{PFD}) of 20MHz with the LTC6946. This means that if, for example, the reference input frequency (f_{REF}) is 100MHz, the reference divider (R) needs to be set equal to 5.

The rule of thumb for achieving a stable loop in a PLL system is to make the loop bandwidth (LBW) less than f_{PFD} by at least a factor of 10. Accordingly, and to optimize for fast settling, we can set the LBW equal to 2MHz in our example. This is as opposed to setting the LBW equal to the frequency offset, where the in-band phase noise of the PLL intersects the phase noise of the VCO to optimize for overall phase noise performance.

Let us pick the LTC6946-3 to produce a 4GHz output signal and use PLLWizard™ software tool to determine the filter component values required to build the circuit around the LTC6946. PLLWizard is a free tool available at www.linear.com/pllwizard to assist in the design and simulation of the LTC6946.

After entering the desired f_{PFD} and LBW values and performing a few mouse clicks in the PLLWizard GUI, we have the loop filter component values, which we can install in the LTC6946 circuit. The screenshot in Figure 1 shows how the PLLWizard tool streamlines the LTC6946 design process. To verify that our work is correct, we simulate the expected phase noise out of the LTC6946 under the given conditions. Figure 1 includes PLLWizard's prediction.

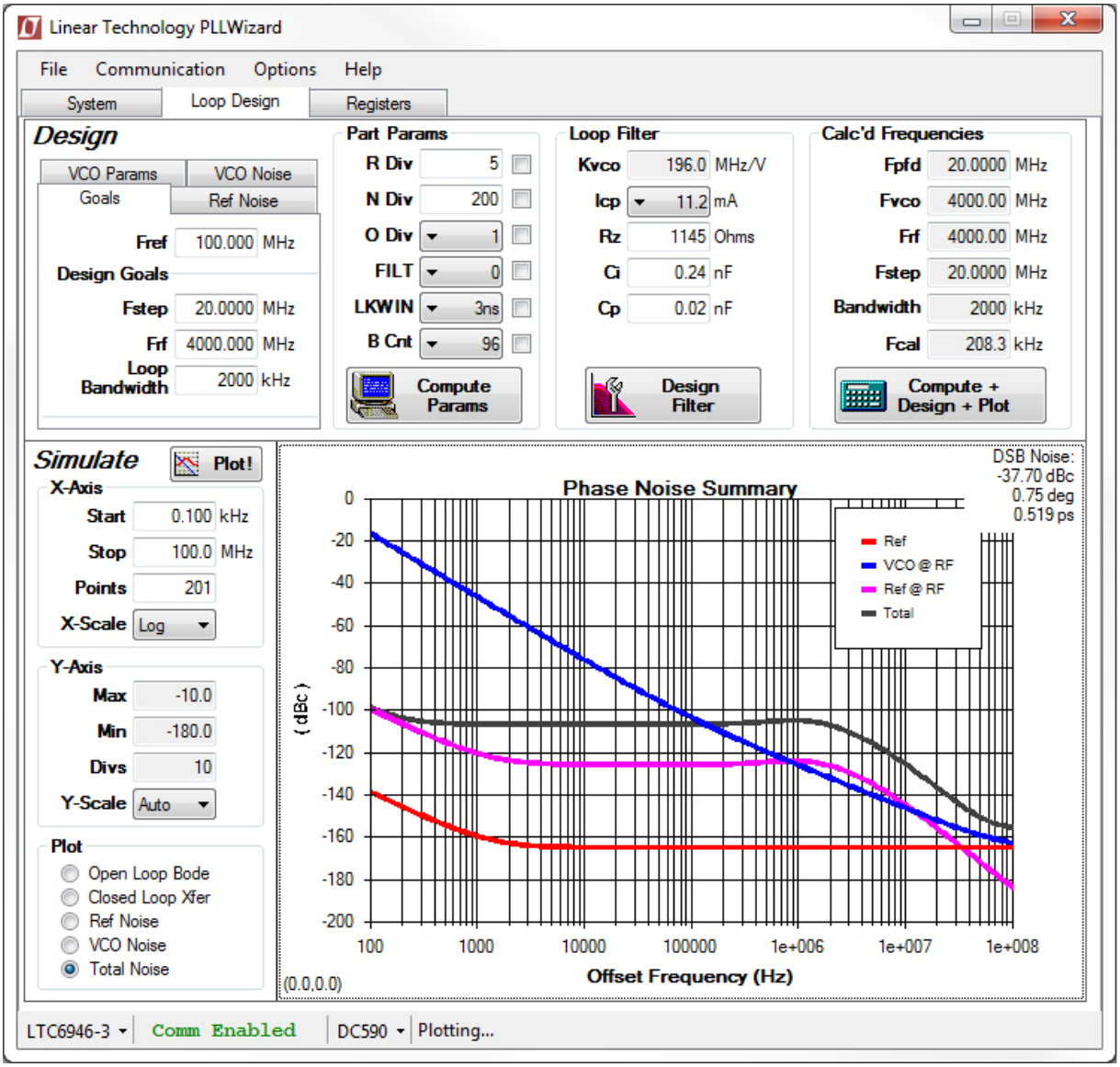

Figure 1. PLLWizard Tool's Settings and Prediction for the LTC6946 Phase Noise at 4GHz with an f_{PFD} of 20MHz and an LBW of 2MHz

Next, we power up the circuit and take a phase noise measurement using a Keysight E5052A Signal Source Analyzer. Figure 2 shows the result of this measurement, which closely agrees with the above simulation.

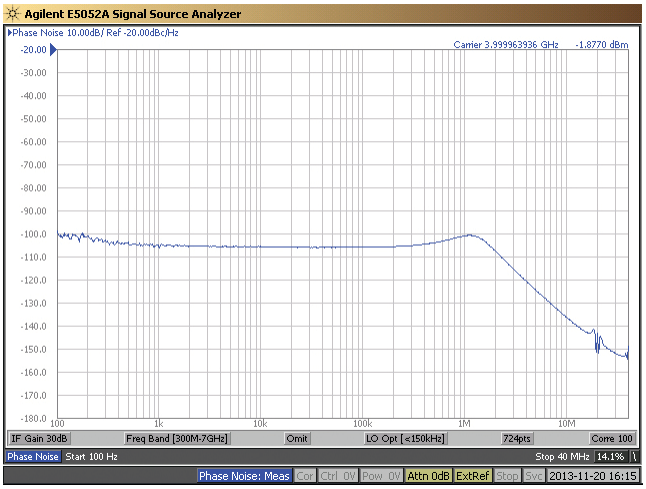

Figure 2. The LTC6946 Output Phase Noise Measured by the Keysight E5052A Signal Source Analyzer

Now let us check how fast the output of the LTC6946 settles to within 10kHz of the final frequency value following a 20MHz step going from an output of 3.98GHz to 4.00GHz. The E5052A can capture the transient response, as depicted in Figure 3.

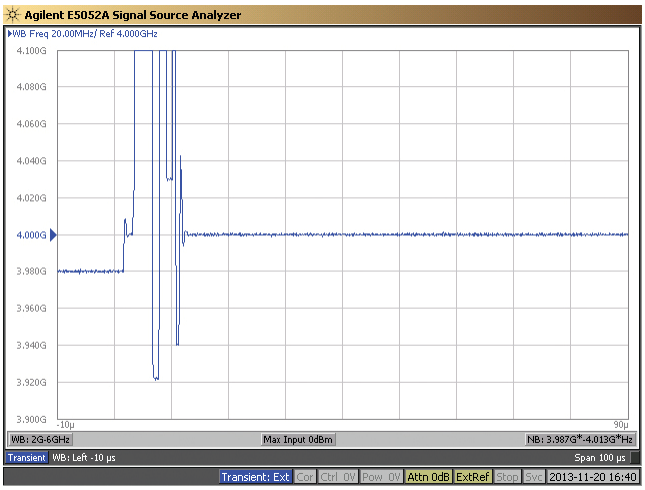

Figure 3. The LTC6946 Output Settling Following a 20MHz Frequency Jump

Let us zoom in on the y-axis by narrowing down the E5052A detector bandwidth in the measurement above to better pinpoint the settling time. Figure 4 illustrates how the LTC6946's output is settled within 10kHz of the final frequency value in less than 15µs.

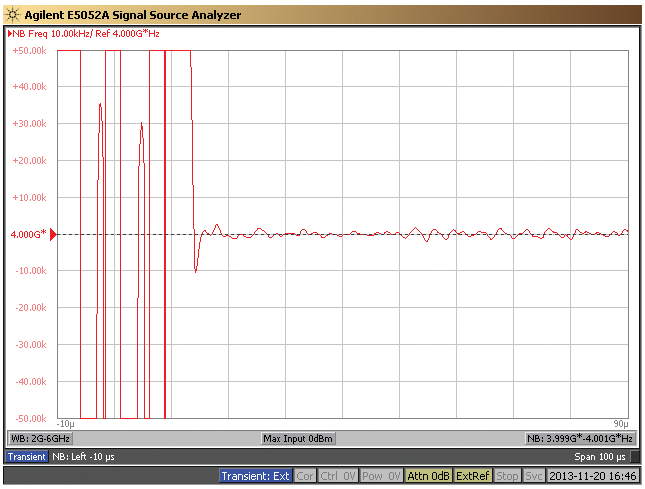

Figure 4. The LTC6946 Output Is Settled in Less than 15µs Following a 20MHz Frequency Step

It should be noted that a modern synthesizer IC with an integrated VCO uses multiple internal VCO sub-bands to cover its entire output frequency range. Every time the synthesizer IC output frequency is changed, the IC must run an internal VCO calibration routine to determine the correct VCO sub-band. In cases where the LBW of the PLL is relatively large, as in our example, the amount of time required to finalize this calibration process constitutes a large portion of the settling time when switching frequencies. Thanks to the LTC6946-3's ability to run this calibration process typically in a little over 10µs, we were able to achieve a total settling time of about 15µs.

Figures 3 and 4 show that the LTC6946 output frequency jumps around during VCO calibration. This behavior is shown here for illustration reasons. In most practical cases, it is undesirable to have the output frequency behave like this. Leaving the "MTCAL" register set equal to "1" ("1" is the default value) on the LTC6946 takes care of this by muting the RF output during calibration. It is recommended that "MTCAL" is always set to "1".

You can follow and modify the steps in this article to determine the appropriate parameters to suit your application. The DC1705 (LTC6946 demo board) provides a comprehensive development platform for evaluating the performance of the PLLs under a variety of filter and frequency configurations. The DC2026 Linduino® USB controller board provides the communications interface between the PLL demo board and the PC using the PLLWizard tool.

The PLLWizard GUI allows full control of the DC1705. However, to program the PLL IC in a very short amount of time to make the fast frequency switching possible, we will write some Linduino code and run the DC2026 at its maximum SPI interface speed. The use of the DC2026 along with the custom code is crucial to achieving the fast programming of the PLL IC via its SPI interface, while also providing a code development environment using the Arduino IDE if desired.

We have evaluated the phase noise behavior of our fast settling synthesizer. However, given we have made the loop bandwidth relatively high, one would question what happens to the spurious performance. One would expect the spurious performance to suffer under these conditions when using a typical synthesizer IC. This is not the case with the LTC6946. With a loop bandwidth of 2MHz and an f_{PFD} of 20MHz, achieving close to −90dBc reference spurs (unwanted signals at f_{PFD} = 20MHz offset from the carrier at 4GHz) is remarkable, as the LTC6946 frequency spectrum presented in Figure 5 confirms.

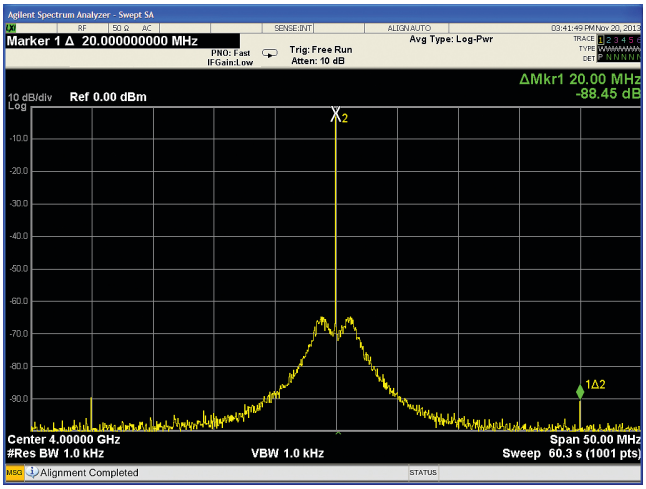

Figure 5. The LTC6946 Output Spectrum Showing Extraordinarily Low Spurs at 4GHz Output with a Loop Bandwidth of 2MHz

The LTC6946 is known for its ability to generate low phase noise and low spurious outputs. Here we have demonstrated that it is possible to achieve ultrafast frequency switching with the LTC6946 without compromising the spurious performance. The LTC6946 is an excellent choice for low phase noise frequency generation in frequency hopping communications applications.