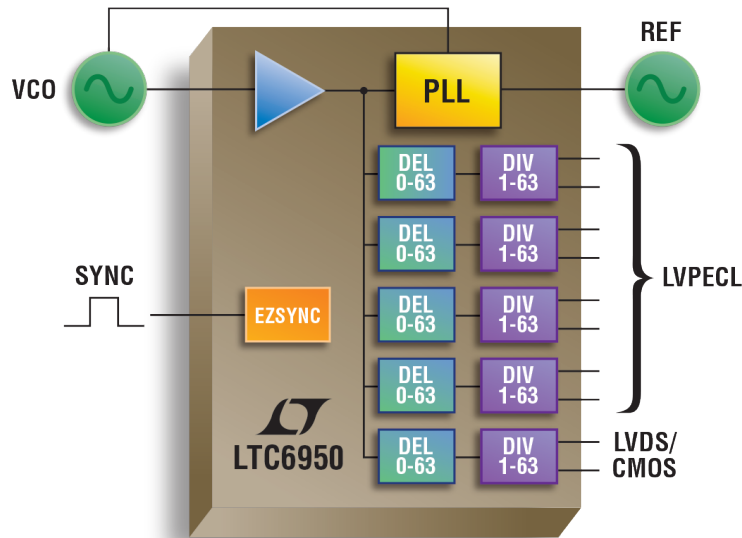


# Ultralow Jitter Clock Generation and Distribution



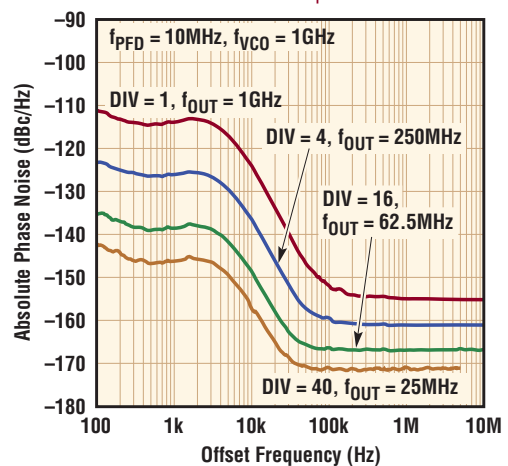
## 1.4GHz Clean Clocking Solution with $18\text{fs}_{\text{RMS}}$ Jitter (12kHz to 20MHz Bandwidth)

The LTC6950 improves SNR performance and solves clocking problems in high end data converter applications. The LTC6950 integrates a low phase noise integer-N synthesizer along with an ultralow jitter clock distribution output section to produce the low jitter signals essential to clocking data converters with high SNR levels. Besides minimizing jitter, the LTC6950 introduces EZSync™ synchronization, a simple synchronization method that guarantees repeatable edge-synchronized outputs from one chip or multiple chips.

### Features

- Additive Jitter:  $18\text{fs}_{\text{RMS}}$  (12kHz to 20MHz)
- EZSync Multichip Clock Edge Synchronization
- Full PLL Core with Lock Indicator
- $-226\text{dBc/Hz}$  Normalized In-Band Phase Noise Floor
- $-274\text{dBc/Hz}$  Normalized  $1/f$  Phase Noise
- 1.4GHz Maximum VCO Input Frequency
- Four Independent, Low Noise 1.4GHz LVPECL Outputs
- One LVDS/CMOS Configurable Output
- Five Independently Programmable Dividers
- Five Independently Programmable VCO Clock Cycle Delays

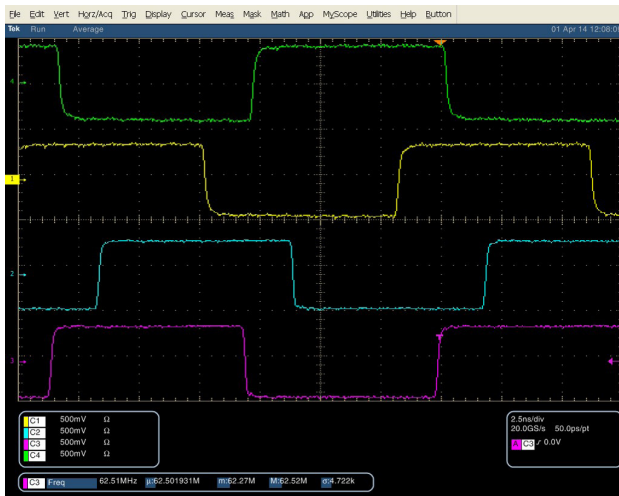
### LTC6950 Closed-Loop Phase Noise



LT, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks and EZSync and ClockWizard are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

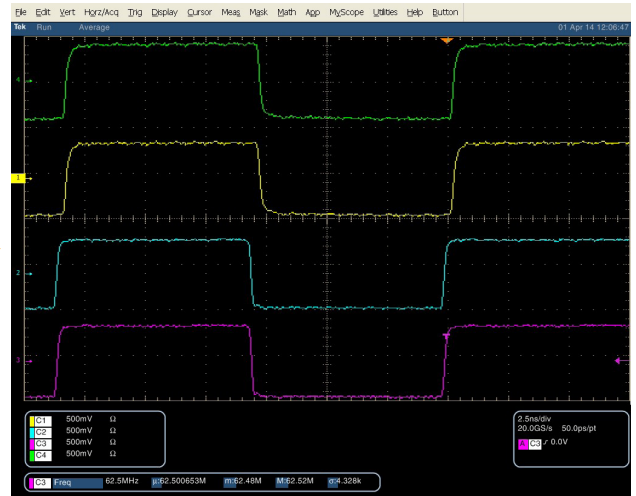
# EZSync Synchronization Simplifies the Generation of Repeatable Edge-Synchronized Outputs from One Chip or Multiple Chips

**EZSync Disabled: Random Phase Relationship Between the Outputs of the LTC6950's Clock Dividers**



With EZSync

**EZSync Enabled: Repeatable Rising-Edge Aligned Outputs of the LTC6950's Clock Dividers**



## ClockWizard™ GUI Streamlines the Design and Simulation Processes



### Advantages

- Find PLL Parameters Quickly
- Show PLL Frequency Response and Stability
- Simulate Output Phase Noise and Jitter
- Simulate Output Clock Phase Relationships Based on EZSync Settings
- Read and Write All Device Registers
- Configure Using a Block Diagram Programming Interface
- Troubleshoot Common Setup Problems
- Import and Export VCO, Reference and Output Noise Data

