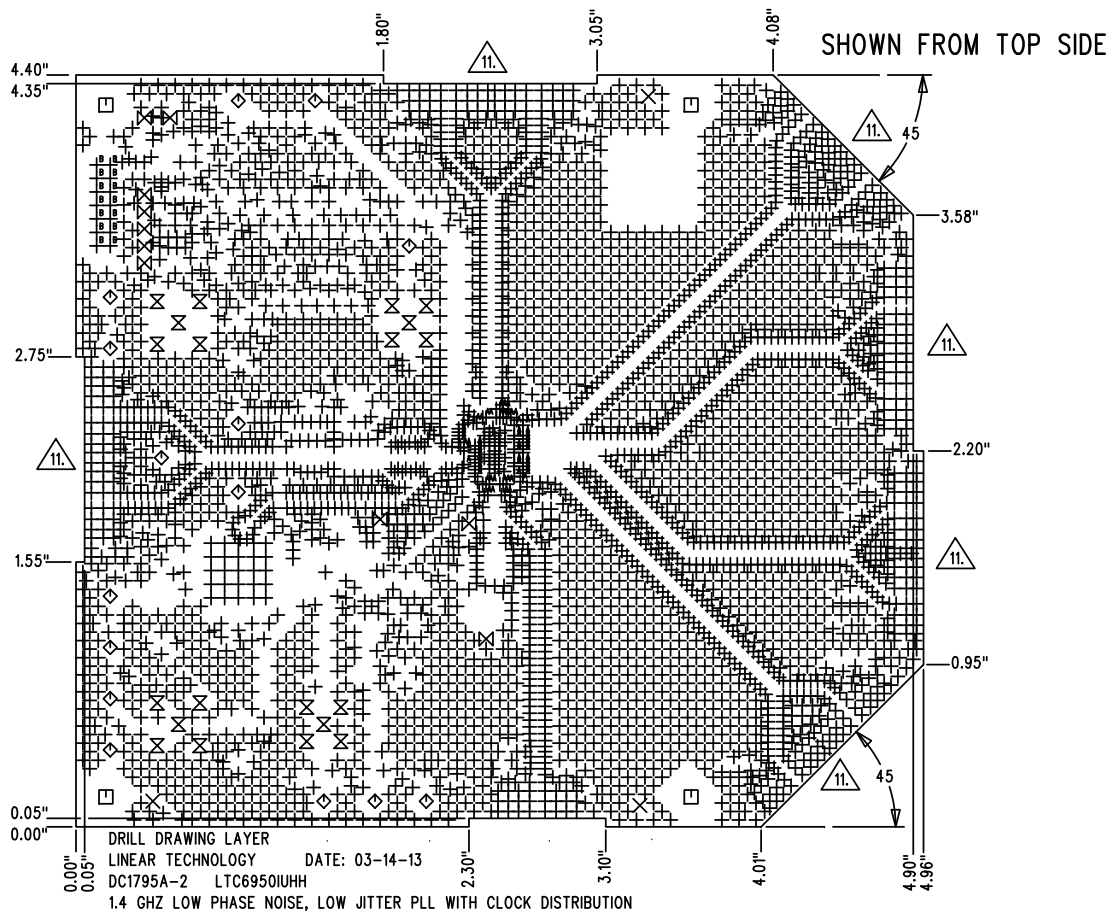
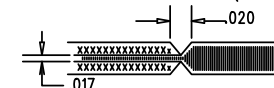


REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	2	2nd PROTOTYPE	MICHEL A.	03-14-13



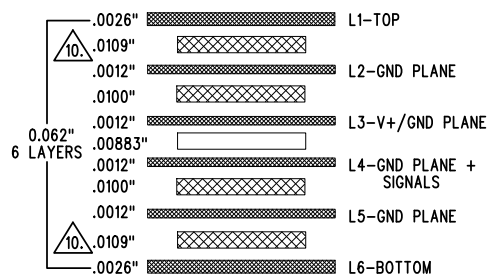
NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -EPOXY FIBERGLASS, NELCO 4000-13
 -FINISHED THICKNESS TO BE 0.062" +/- .005"
 -TOTAL OF 6 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
 -FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
 0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
 -ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
 -HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
 -GOLD IMMERSION BOTH SIDES.
 -FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
 PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



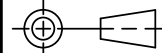
- CONTROLLED 50 OHM +/-10% IMPEDANCE FOR LAYERS 1-2
 LAYER 6-5, USING 0.02" TRACE.
- SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.
- INNER AND OUTER LAYER COPPER SHALL BE EXPOSED ALONG BOARD EDGES. DO NOT MODIFY INNER LAYER COPPER BACKOFF OUTLINE (SMA CONNECTOR).

LAYER STRUCTURE



SIZE	QTY	SYM	PLATED	TOL
0.012	3980	+	YES	+/-0.003"
0.07	3	X	NO	+/-0.003"
0.19	4	□	NO	+/-0.003"
0.064	15	◇	YES	+/-0.003"
0.055	20	⊗	YES	+/-0.003"
0.025	10	⊗	YES	+/-0.003"
0.006	62	+ ^A	YES	+/-0.003"
0.04	14	+ ^B	YES	+/-0.003"

UNLESS OTHERWISE SPECIFIED
 DIMENSIONS ARE IN INCHES
 TOLERANCES:
 0.XX" = ±0.01"
 0.XXX" = ±0.005"
 INTERPRET DIM AND TOL
 PER ASME Y14.5M-1994
 THIRD ANGLE PROJECTION



APPROVALS

PCB DES. KIM T.
 APP ENG. MICHEL A.

LINEAR TECHNOLOGY

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 1.4 GHZ LOW PHASE NOISE, LOW JITTER PLL
 WITH CLOCK DISTRIBUTION

SIZE IC NO. LTC6950IUHH REV
 N/A DEMO CIRCUIT 1795A 2

SCALE = NONE

FILENAME: DC1795A-2.PCB

SHT 1 OF 1