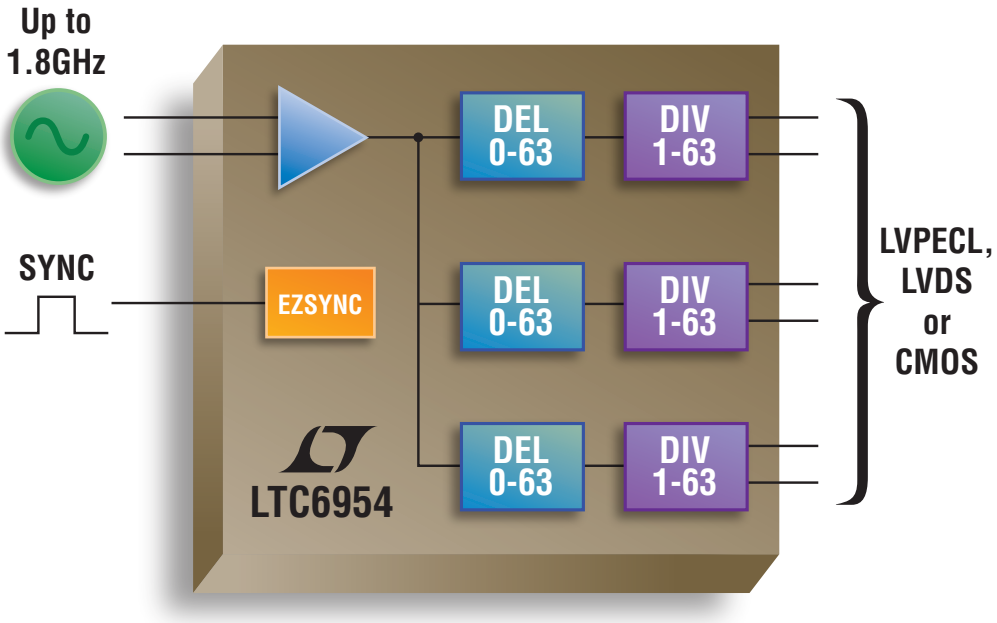
Less than 20fs$_{RMS}$ Additive Jitter Clock Distribution Solution with EZSync



Ultralow Additive Jitter for Uncompromised Data Converter SNR Performance

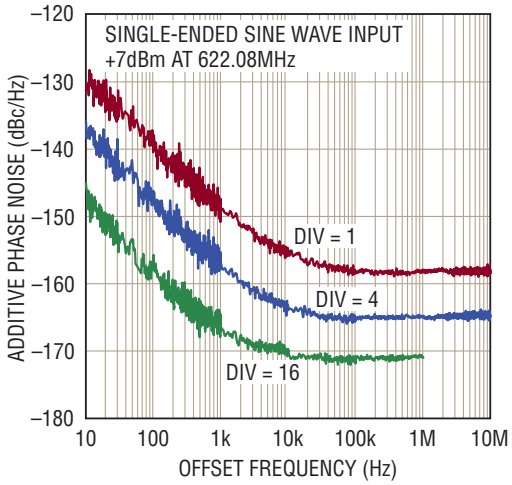
With less than 20fs$_{RMS}$ additive jitter over the 12kHz to 20MHz bandwidth, the LTC®6954 is ideal for distributing the low jitter clocks necessary to achieve the best SNR when driving high resolution data converters. Besides minimizing jitter, the LTC6954 features EZSync™ synchronization method that guarantees repeatable edge-synchronized outputs from one or multiple chips.

Features

- Three Independent, Low Noise Outputs
- Additive Jitter < 20fs$_{RMS}$ (12kHz to 20MHz)
- Additive Jitter < 85fs$_{RMS}$ (10Hz to Nyquist)
- Up to 1.8GHz Maximum Input Frequency
- EZSync Clock Synchronization Compatible
- Clock Dividers Covering All Integers from 1 to 63
- Phase Delays Covering All Integers from 0 to 63
- –40°C to 105°C Junction Temperature Range

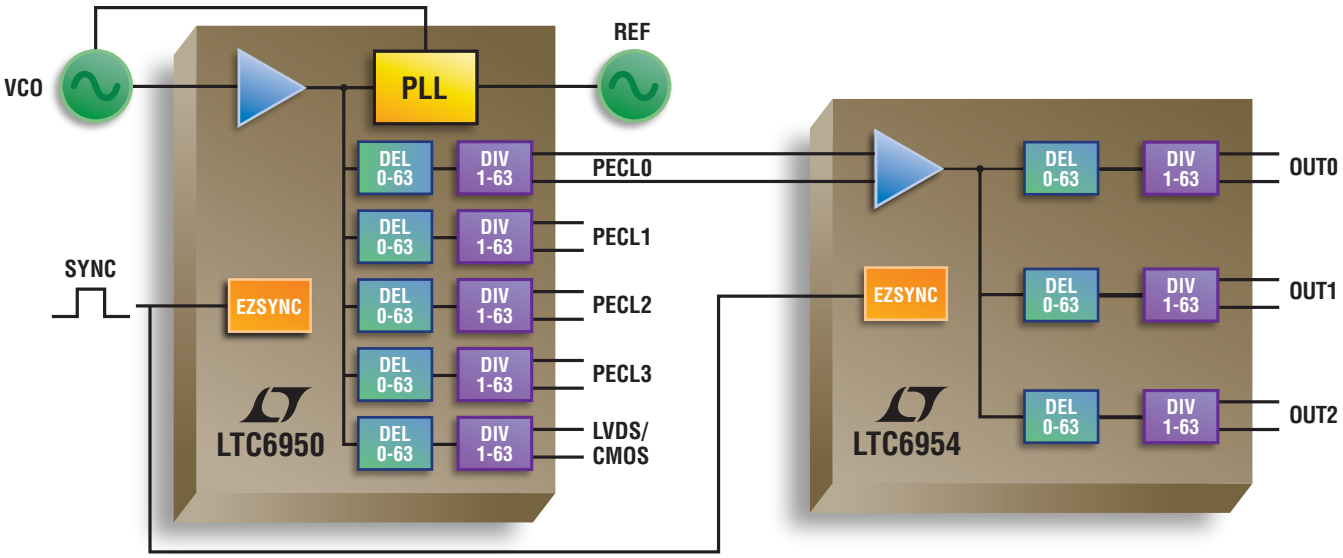
Part Number	Description
LTC6954-1	3 LVPECL Outputs
LTC6954-2	2 LVPECL and 1 LVDS/CMOS Outputs
LTC6954-3	1 LVPECL and 2 LVDS/CMOS Outputs
LTC6954-4	3 LVDS/CMOS Outputs

LVPECL Output Additive Phase Noise, f_{IN} = 622.08MHz



LINEAR TECHNOLOGY

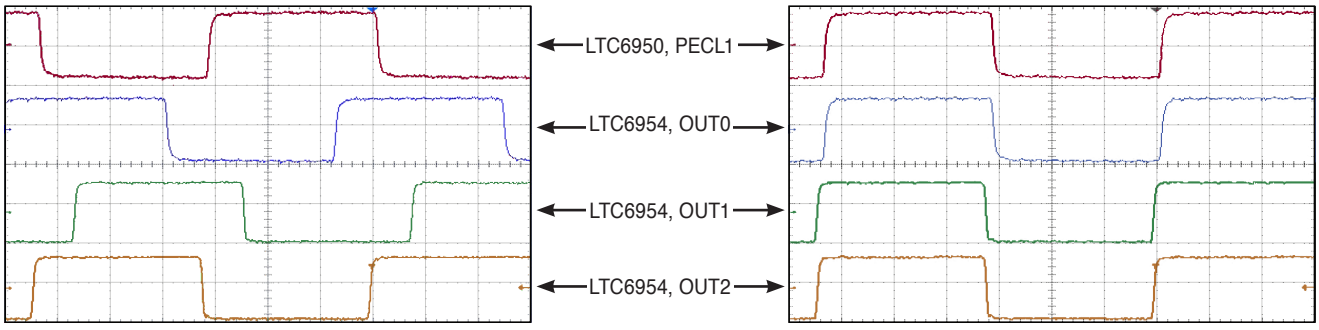
EZSync Multichip Synchronization Simplifies the Generation of Repeatable Edge-Synchronized Outputs



With EZSync Enabled and the PECL0 Output of the LTC6950 Driving the LTC6954 Input, All Seven Outputs of the Two Devices Are Rising-Edge Synchronized

EZSync Disabled:
Random Phase Relationship Between the Outputs of the LTC6950 and LTC6954 Clock Dividers

EZSync Enabled:
Repeatable Rising-Edge Aligned Outputs of the LTC6950 and LTC6954 Clock Dividers



2.5ns/DIV

2.5ns/DIV