25A Monolithic Synchronous DC/DC Step-Down Converter with PMBus Interface

FEATURES

- **4.5V to 20V V_{IN} Range**
- **1% Total V_{OUT} Accuracy Over Temperature**
- **Single Resistor-Programmable Reference Voltage: 0.4V to 3.5V**
- **PMBus Compliant Serial Interface:**
  - **Programmable Output Voltage Margining: Up to ±25% V_{OUT} Range with 0.1% Resolution**
  - **Read Back of Average and Peak Temperature, Current, and Voltage (25Hz Refresh Rate)**
  - **Fault Status**
- **Phase-Lockable Fixed Frequency Up to 2MHz**
- **Less Than 1ms Power-Up Time**
- Optional External Reference Input
- Pin Selectable Fast-Margining of the Output Voltage
- Power Good Flag with Pin Programmable Thresholds and Filter Delay
- Differential Remote Output Voltage Sensing
- Master Shutdown Mode: 125µA Supply Current
- Clock Out for 2-Phase Operation (50A Load)
- Available in a Thermally-Enhanced 6.25mm × 7.5mm × 2.22mm BGA Package

DESCRIPTION

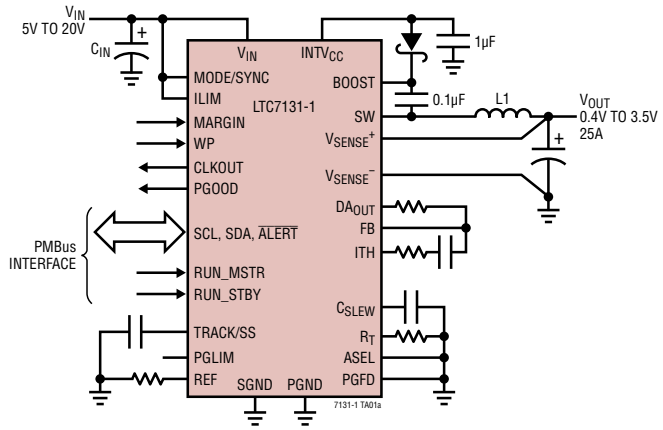
The LTC®7131-1 is a high efficiency, 25A monolithic synchronous buck regulator using a phase lockable controlled on-time, current mode architecture. The output voltage is programmable with a single external resistor or an external voltage reference through the reference input (REF) pin. The output voltage can be margined up or down up to ±25% with 0.1% resolution via a PMBus-compliant serial interface. The serial interface can also be used to read back fault status and both time-averaged (~4ms) and peak input/output current, input/output voltage and temperature. System configuration and monitoring is supported by the LTpowerPlay® development system.

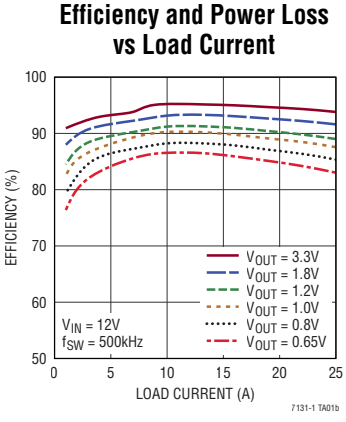
The architecture provides extremely fast response and allows operation at the very low on-times required to regulate low output voltages at high switching frequencies. The operating frequency is programmable from 250kHz to 2MHz with an external resistor or for noise sensitive applications, it can be synchronized to an external clock over the same range.

APPLICATIONS

- Intelligent Energy Efficient Power Conversion
- ASIC/FPGA/Processor Power
- Point of Load Conversion

TYPICAL APPLICATION



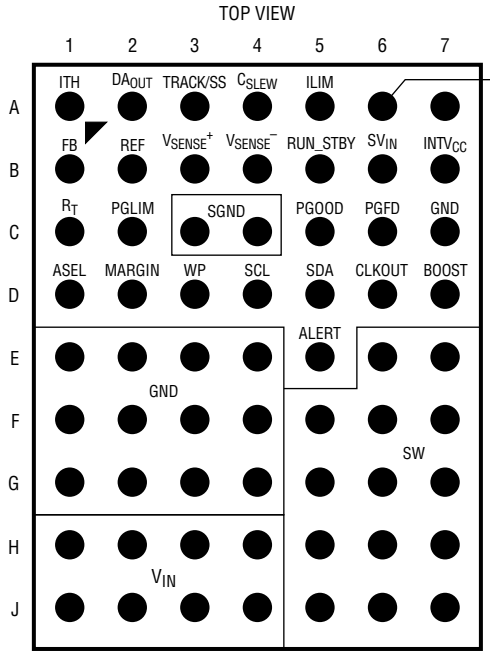


ABSOLUTE MAXIMUM RATINGS

(Notes 1,7)

SV_{IN}, V_{IN} ..... –0.3V to 20V
$INTV_{CC}$ Voltage ..... –0.3V to 6V
V_{SENSE}^+, V_{SENSE}^-, C_{SLEW}, R_T, ITH,
MODE/SYNC, REF, TRACK/SS, PGFD, PGLIM,
ASEL, DA_{OUT}, MARGIN, RUN_STBY,
FB, ILIM ..... –0.3V to ($INTV_{CC}$ + 0.3V)
RUN_MSTR, PGOOD, ALERT,
SCL, SDA Voltage ..... –0.3V to 6V
WP ..... –0.3V to 2.5V
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



BGA PACKAGE
63-LEAD (7.5Amm × 6.25mm × 2.22mm)
T_{JMAX} = 150°C, θ_{JA} = 18.5°C/W
θ_{JCtop}= 25.5°C/W, $\theta_{JCbottom}$ = 5.8°C/W

NOTE:
1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
2) θ_{JA} VALUE IS OBTAINED WITH ADI DEMO BOARD.
3) REFER TO PAGE 24 FOR LAB MEASUREMENT AND DE-RATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PACKAGE TYPE	BALL FINISH	PART MARKING		MSL RATING	TEMPERATURE RANGE
			DEVICE	FINISH CODE		
LTC7131RY-1#PBF	BGA	SAC305(RoHS)	LTC7131-1	e1	3	–40°C to 150°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, V_{IN} = 12V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Range		●	4.5		20	V
V_{REF}	REF Pin Programming Range		●	0.4		3.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, V_{IN} = 12V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	V_{IN} Supply Current Normal Mode Standby Shutdown	 V_{RUN_MSTR} > 1V (Note 4) V_{RUN_STBY} = 0V, V_{RUN_MSTR} > 1V V_{RUN_MSTR} = 0V			 5 500 125	 8 200	 mA µA µA
V_{UVLO}	$INTV_{CC}$ Undervoltage Reset Hysteresis	$INTV_{CC}$ Rising $INTV_{CC}$ Falling	●	3.6	3.9 0.32	4.25	V V
I_{REF}	Reference Current	LTC7131R-1 (Note 10)	●	99	100	101	µA
$\Delta I_{REF,LINE}$	Reference Current Line Regulation	V_{IN} = 5V to 20V (Note 10)	●			0.02	%/V
$\Delta V_{OUT,OFFSET}$	Regulation Accuracy $\Delta V_{OUT,OFFSET} = (V_{SENSE}^+ - V_{SENSE}^-) - V_{REF}$	V_{REF} = 1.5V (Notes 5, 10)	●	–0.5		0.5	%
$\Delta V_{OUT,MARGIN}$	Maximum Margining Range Set Point Accuracy Resolution LSD Step Size	 MFR_VOUT_COMMAND = –25% to 25%, V_{REF} = 1.5V (Note 5)	 ●	–25 –0.5	 9 0.1	25 0.5	% % Bits %
NL_V_{OUT}	DAC Nonlinearity					±1	LSB
A_{EA}	Error Amplifier Open Loop Gain	I_{TH} = 1V (Note 5)			80		dB
f_{BW}	Error Amp Gain Bandwidth Product	(Note 6)			20		MHz
R_{IN}	Differential Amplier Input Resistance	Measured at V_{SENSE}^+ Pin			160		kΩ
t_{SS}	Internal Soft-Start Time/V_{REF}	External C_{SS} = Float			1		ms/V
I_{CSLEW}	C_{SLEW} Pull-Up Current	V_{CSLEW} = 0V			10		µA
I_{LIM}	SW Valley Current Limit	Sourcing (Note 8), ILIM = $INTV_{CC}$ Sinking	●	25	 –20		A A
I_{RUN_MSTR}	RUN_MSTR Pull-Up Current	V_{RUN_MSTR} = 0V			1.5		µA
I_{RUN_STBY}	RUN_STBY Pull-Up Current	V_{RUN_STBY} = 0V			2.5		µA
V_{RUN_MSTR}	Regulator On Threshold (Master Shutdown) Regulator On Hysteresis Regulator Power-Down Threshold	Rising Edge Falling Edge I_Q < 200µA		0.8	0.9 0.1 0.6	1.0	V V V
V_{RUN_STBY}	Regulator On Threshold (Standby Mode) Hysteresis	Rising Edge Falling Edge		0.7	1 0.05	1.2	V V
I_{ASEL}	ASEL Programming Current				10		µA
I_{PGFD}	PGFD Programming Current				10		µA
I_{SS}	SS Current	V_{SS} = 0V		4	5	6	µA
$V_{IH,MARGIN}$ $V_{IL,MARGIN}$	MARGIN High Voltage MARGIN Low Voltage			1.3		 0.4	V V
I_{WP}	WP Pin Pull-Up Current	WP = 0V			10		µA
SR_{MARGIN}	Reference Slew Rate During Margin Change	C_{SLEW} = 1nF C_{SLEW} = OPEN C_{SLEW} = $INTV_{CC}$			0.1 23 10		%/ms %/ms %/µs
t_{INIT}	Initialization Time	Delay from Power Applied Until V_{OUT} Ramp Up (Note 6)			1		ms
Oscillator and Power Switch							
f_{OSC}	Oscillator Frequency	R_T = 25.5k R_T = $INTV_{CC}$	●	450 435	500 480	550 525	kHz kHz
$V_{IH,SYNC}$ $V_{IL,SYNC}$	SYNC Level High SYNC Level Low			1.2		 0.3	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, V_{IN} = 12V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{MODE}	Discontinuous Mode Threshold			0.7	1	1.3	V
$t_{ON(MIN)}$	Minimum On-Time				35		ns
$t_{OFF(MIN)}$	Minimum Off-Time				100		ns
R_{TOP}	Top Power NMOS On Resistance				7.3		mΩ
R_{BOTTOM}	Bottom Power NMOS On Resistance				2.1		mΩ
θ_{CLKOUT}	Relative Phase of CLKOUT	MODE/SYNC = 0V (Note 6)			180		Deg
PGOOD							
$V_{PGOOD,DEFAULT}$	Default PGOOD Threshold	V_{PGLIM} = $INTV_{CC}$, V_{OUT} >1V		±8	±10	±12	%
$V_{PGOOD,PROGRAM}$	Program PGOOD Threshold	V_{PGLIM}/V_{REF} = 0.19, V_{OUT} ≥ 1V V_{PGLIM}/V_{REF} = 0.38		±6 ±13	7.5 15	±9 ±17	% %
I_{LEAK}	PGOOD Leakage Current					±5	µA
V_{OL}	PGOOD Output Low Voltage	I_{OUT} = 3mA			0.1	0.3	V
t_{PGFD}	PGOOD Filter Delay	PGFD = 0V PGFD = 0.65V PGFD = Open		150 1.0 17	190 1.6 24	250 2.2 32.5	µs ms ms
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6 < V_{IN} < 20V		4.8	5	5.2	V
V_{LDO_INT}	V_{INTVCC} Load Regulation	I_{CC} = 0mA to 100mA			0.5		%
Output Voltage Readback							
N	Resolution LSB Step Size				13 0.5		Bits mV
$V_{F/S}$	Full Scale Output Voltage	(Note 9)			16.4		V
V_{OUT_TUE}	Total Unadjusted Error	LTC7131R-1	●			±1 ±0.5	% %
$t_{CONVERT}$	Conversion Time				40		ms
Input Voltage Readback							
N	Resolution LSB Step Size				13 4		Bits mV
$V_{F/S}$	Full Scale Input Voltage	(Note 9)			131		V
V_{IN_TUE}	Total Unadjusted Error		●			±1.5	%
$t_{CONVERT}$	Conversion Time				40		ms
Output Current Readback							
N	Resolution LSB Step Size				13 10		Bits mA
$V_{F/S}$	Full Scale Output Current				±82		A
I_{OUT_TUE}	Total Unadjusted Error					±10	%
$t_{CONVERT}$	Conversion Time				40		ms
Input Current Readback							
N	Resolution LSB Step Size				13 10		Bits mA
$V_{F/S}$	Full Scale Input Current				±82		A
I_{IN_TUE}	Total Unadjusted Error				±10		%
$t_{CONVERT}$	Conversion Time				40		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, V_{IN} = 12V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Temperature Readback							
N	Resolution LSB Step Size				9 1		Bits °C
$V_{F/S}$	Full Scale Temperature				±256		°C
T_{TUE}	Total Unadjusted Error				±3		°C
$t_{CONVERT}$	Conversion Time				40		ms
PMBus Interface Parameters							
$V_{IH,}$ SDA, SCL	Input High Voltage			1.35			V
$V_{IL,}$ SDA, SCL	Input Low Voltage					0.8	V
$I_{IH,}$ SDA, SCL	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V		–5		5	µA
$V_{OL,\ SDA}$	Output Low Voltage (SDA)	I_{SDA} = 3mA				0.4	V
$V_{OL,\ ALERT}$	Output Low Voltage ($\overline{ALERT}$)	I_{ALERT} = 1mA				0.4	V
f_{SCL}	Serial Bus Operating Frequency			10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_SDA}	Hold Time After (Repeated) Start Condition			0.6			µs
t_{SU_SDA}	Repeated Start Condition Setup Time			0.6			µs
t_{SU_STO}	Stop Condition Setup Time			0.6			µs
$t_{HD\_DAT(OUT)}$	Data Hold Time			150		900	ns
$t_{HD\_DAT(IN)}$	Input Data Hold Time			0			ns
t_{SU_DAT}	Data Set-Up Time			100			ns
t_{LOW}	Clock Low Period			1.3		10000	µs
t_{HIGH}	Clock High Period			0.6			µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer	Measured from Last PMBus Start Event			30		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7131-1R is specified over the –40°C to 150°C operating junction temperature range. High Junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (PD, in Watts) according to the formula:

$$T_J = T_A + (PD \bullet \Theta_{JA})$$

where Θ_{JA} (in °C/W) is the package thermal impedance.

Note 4 : The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \times f_{OSC}$). See applications Information for more information.

Note 5: The LTC7131-1 is tested in a feedback loop that servos FB to a referenced voltage with the I_{TH} pin forced to a voltage between 0.6V and 1V.

Note 6: Guaranteed by design, not subject to test.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum junction temperature may impair device reliability or permanently damage the device.

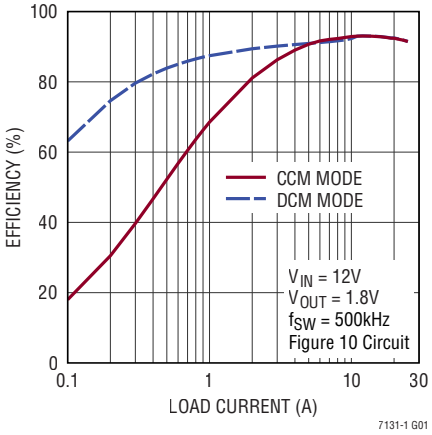
Note 8: The LTC7131-1 uses valley current mode control so the current limits specified correspond to the valley of the inductor current waveform. Maximum load current is higher and equals the valley current limit I_{LIM} plus one half of the inductor ripple current.

Note 9: The maximum input voltage is 20V and output voltage is 5V.

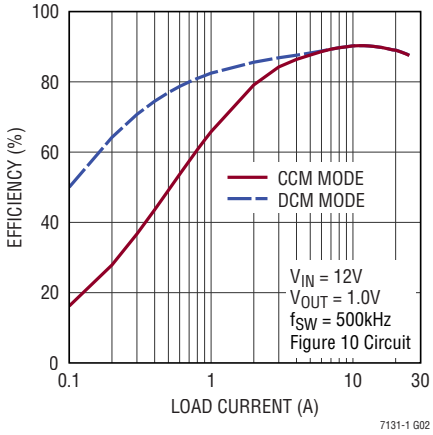
Note 10: Total output accuracy is the sum of the tolerances of I_{REF}, $R_{REF(EXTERNAL)}$, $\Delta V_{OUT,OFFSET}$, and $\Delta I_{REF,LINE} \bullet \Delta V_{IN}$.

TYPICAL PERFORMANCE CHARACTERISTICS

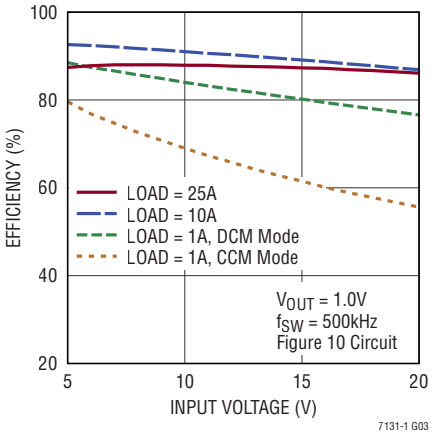
Efficiency vs Load Current and Mode



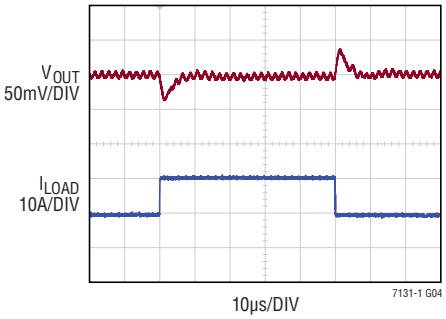
Efficiency vs Load Current and Mode



Efficiency vs Input Voltage

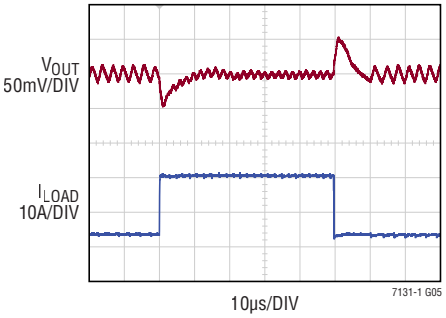


Load Step (Forced Continuous Mode)



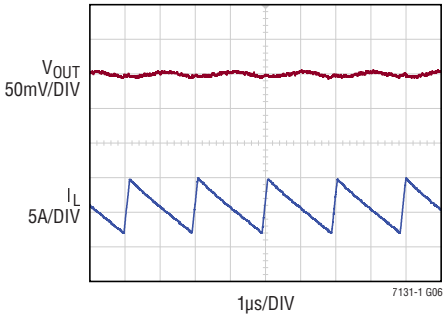
V_{OUT} = 1V
I_{LOAD} = 10A TO 20A
V_{MODE} = 0V
FIGURE 10 CIRCUIT

Load Step (Discontinuous Mode)



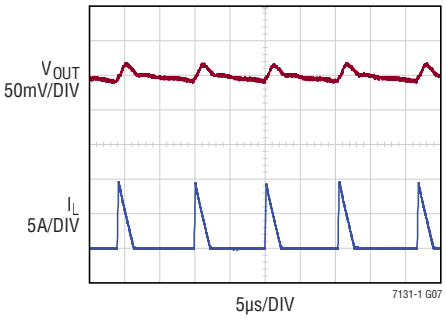
V_{OUT} = 1V
I_{LOAD} = 3A TO 20A
V_{MODE} = 3.3V
FIGURE 10 CIRCUIT

Forced Continuous Mode



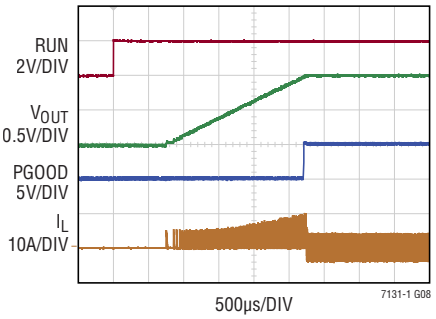
V_{OUT} = 1V
I_{LOAD} = 1A
V_{MODE} = 0V
FIGURE 10 CIRCUIT

Discontinuous Mode Operation



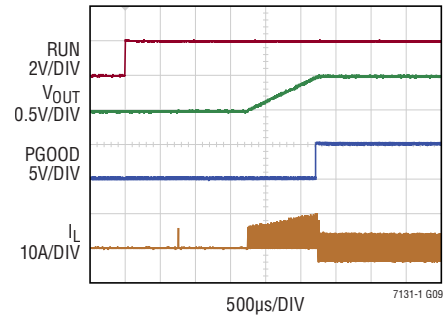
V_{OUT} = 1V
I_{LOAD} = 1A
V_{MODE} = 3.3V
FIGURE 10 CIRCUIT

Normal Start-Up



V_{IN} = 12V
V_{OUT} = 1V
FIGURE 10 CIRCUIT

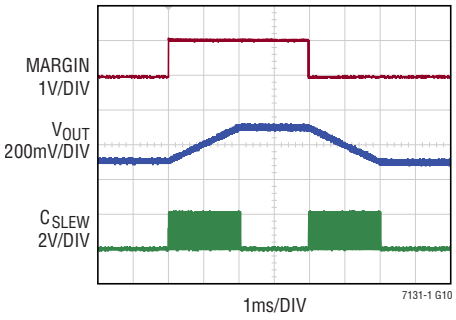
Start-Up Into Prebiased Output



V_{IN} = 12V
V_{OUT} = 1V
FIGURE 10 CIRCUIT

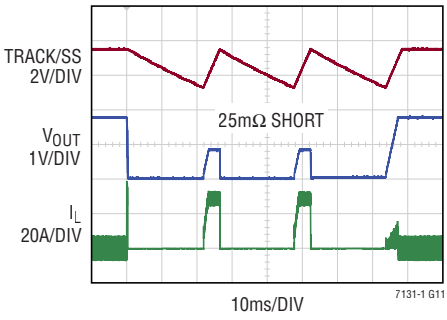
TYPICAL PERFORMANCE CHARACTERISTICS

Output Margining

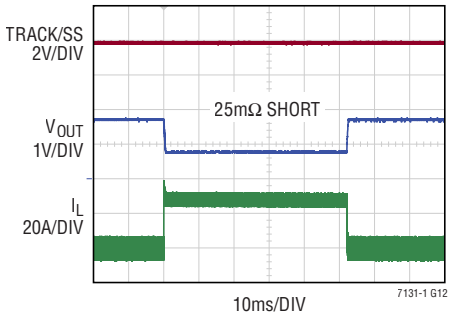


MARGIN REGISTERS PRE–LOADED
TO –10% and 10%
C_{SLEW} = 56pF

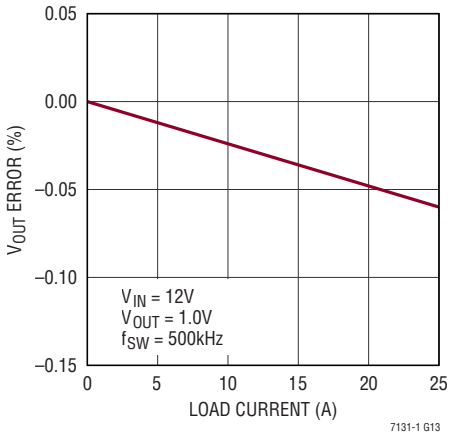
V_{OUT} Short Circuit and Recovery Hiccup Mode Enabled



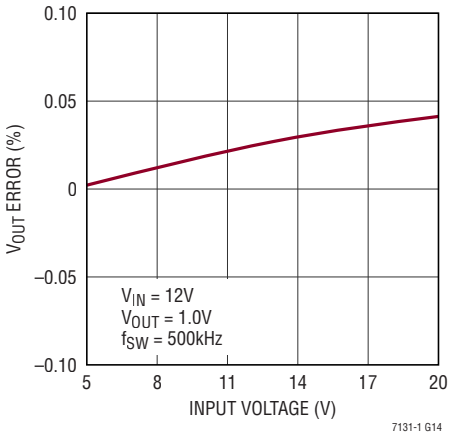
V_{OUT} Short Circuit and Recovery Hiccup Mode Disabled



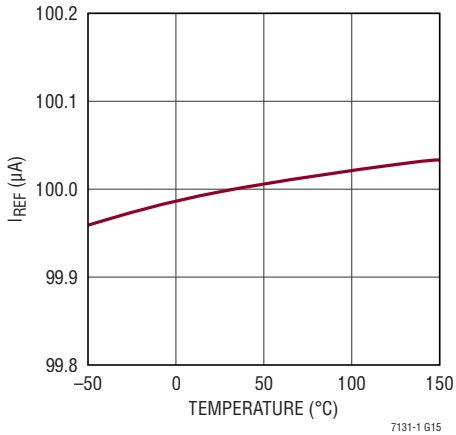
Load Regulation



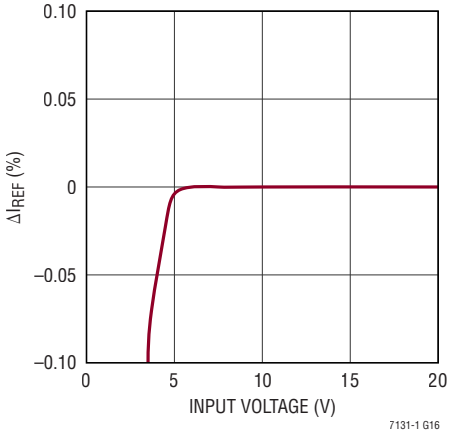
Line Regulation



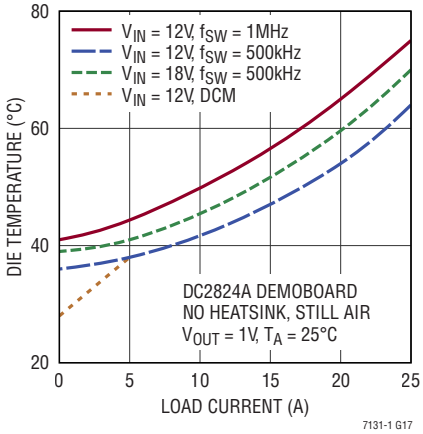
I_{REF} vs Temperature



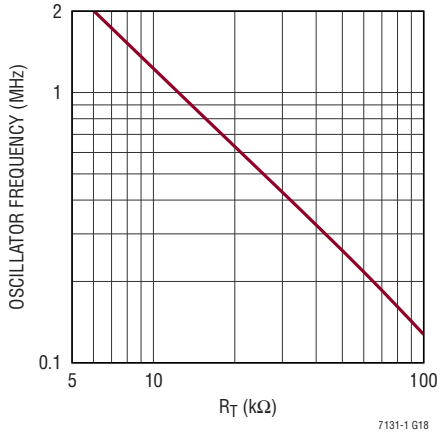
I_{REF} vs Input Voltage



Die Temperature vs Load

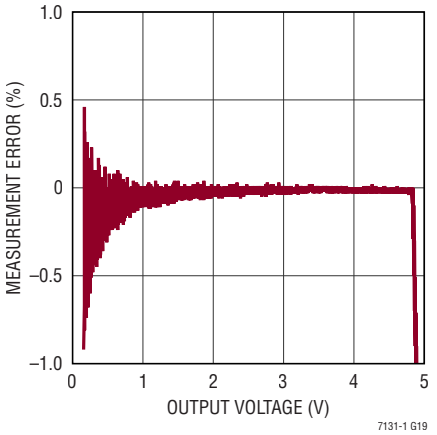


Oscillator Frequency vs R_T

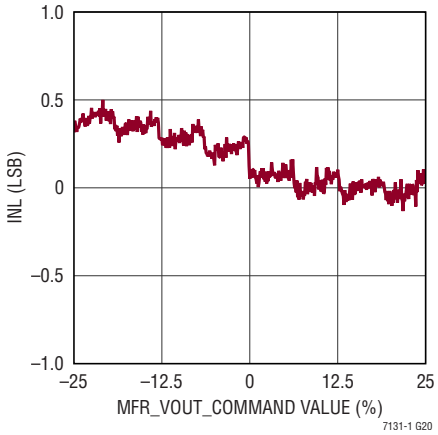


TYPICAL PERFORMANCE CHARACTERISTICS

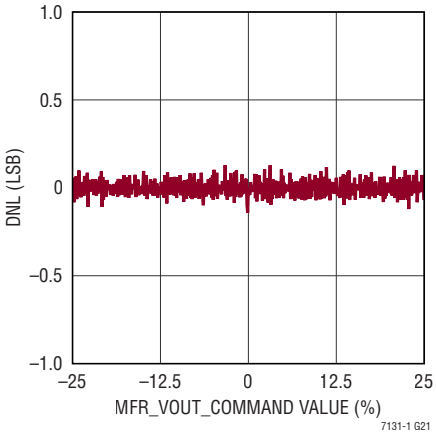
V_{OUT} Error vs V_{OUT}



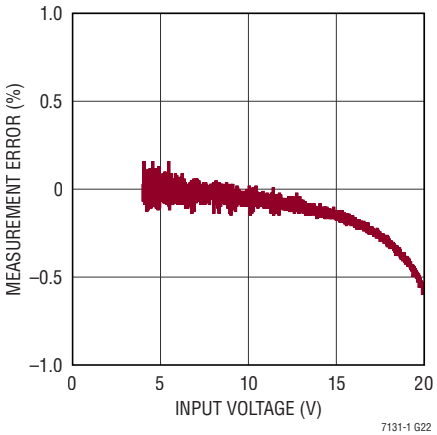
V_{OUT} Command INL



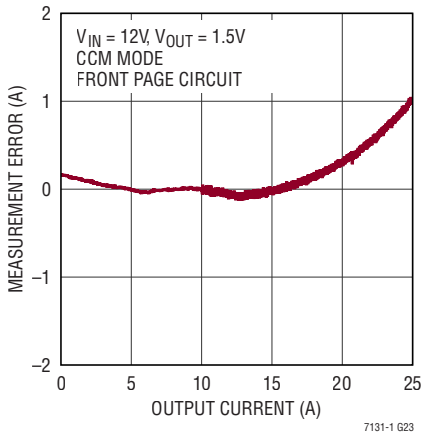
V_{OUT} Command DNL



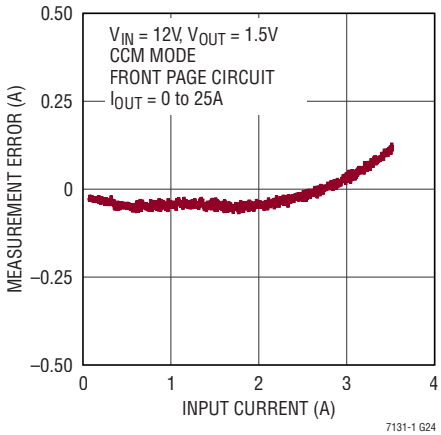
V_{IN} Measurement Error vs V_{IN}



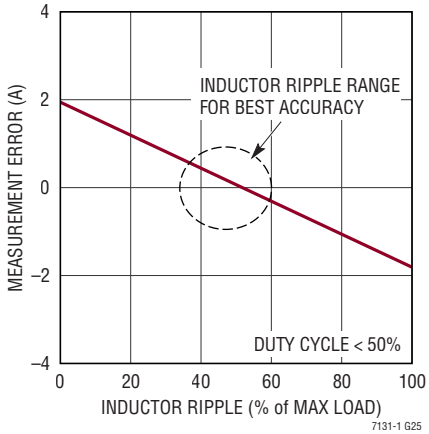
I_{OUT} Measurement Error vs I_{OUT}



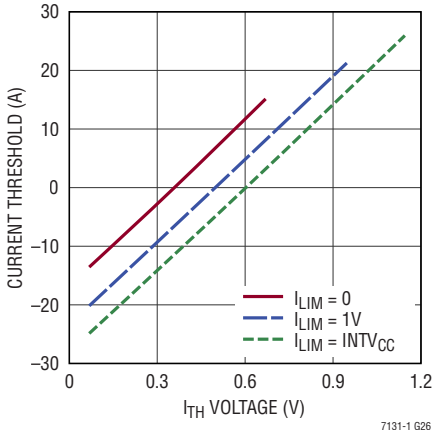
I_{IN} Measurement Error vs I_{IN}



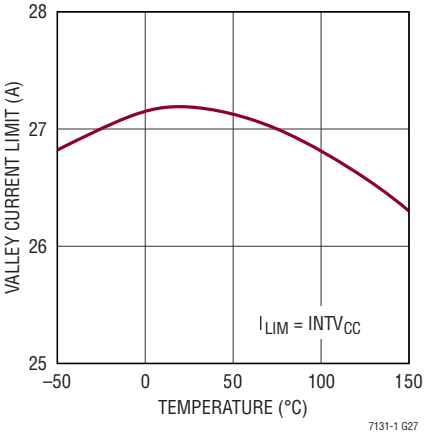
I_{OUT} Measurement Error vs Inductor Ripple Current



Valley Current Threshold vs I_{TH} Voltage

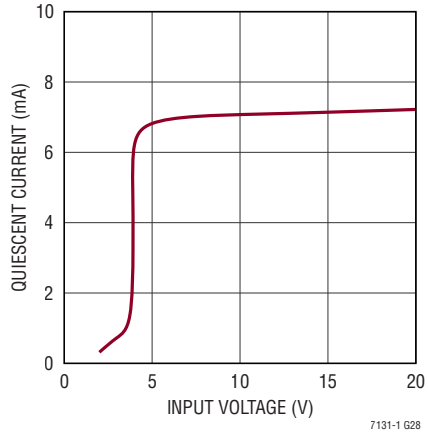


Current Limit vs Temperature

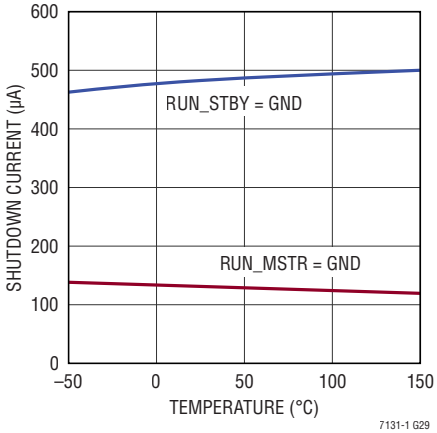


TYPICAL PERFORMANCE CHARACTERISTICS

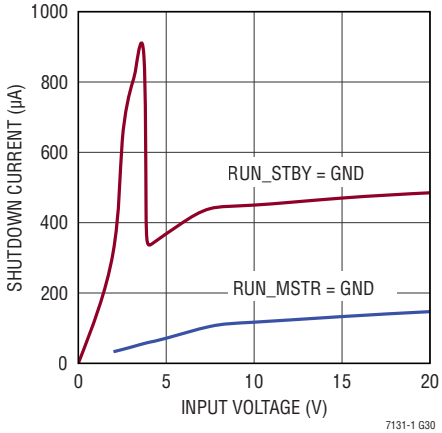
Quiescent Current vs Input Voltage



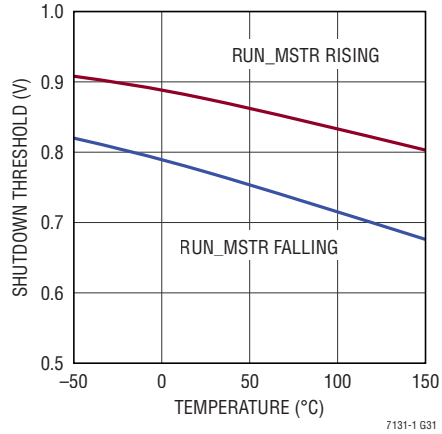
Shutdown Current vs Temperature



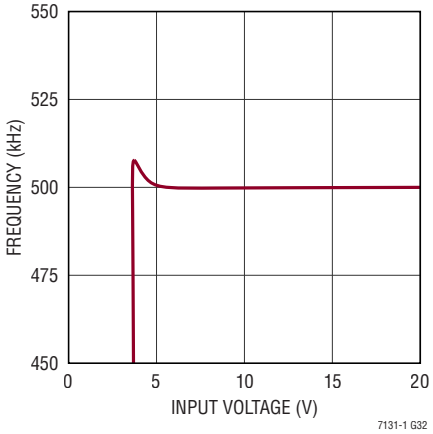
Standby Current vs Input Voltage



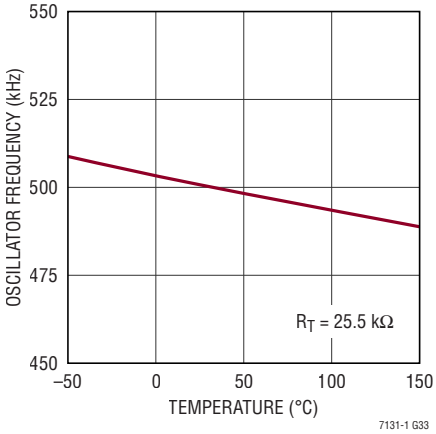
Shutdown (RUN_MSTR) Threshold vs Temperature



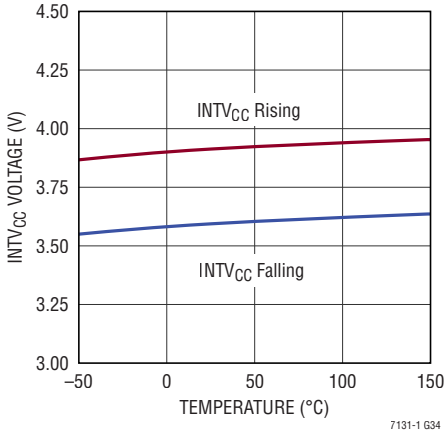
Oscillator Frequency vs Input Voltage



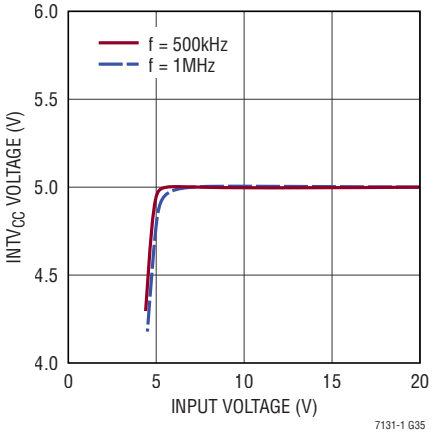
Oscillator Frequency vs Temperature



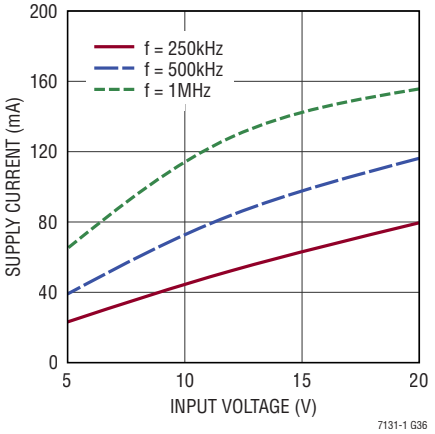
Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



$INTV_{CC}$ Line Regulation



Dynamic Supply Current vs Input Voltage



PIN FUNCTIONS

ITH (Pin A1): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage. Use an RC network between the ITH pin and the FB pin to compensate the feedback loop for optimum transient response.

DA_{OUT} (Pin A2): Differential Amplifier Output.

TRACK/SS (Pin A3): Tracking/Soft-Start Input. For soft-start, a capacitor to ground at this pin sets the ramp rate of the output voltage (approximately 5V/sec/µF). For coincident tracking, connect this pin to a resistive divider between the voltage to be tracked and ground.

C_{SLEW} (Pin A4): Slew Rate Control. Add a capacitor to program the V_{OUT} transition slew rate during margining. The slew rate is equal to 0.1% per ms per nF slew rate capacitance. With a 1nF capacitor, the slew rate is 0.1%/ms. Two default slew rates are also available when this pin is open or shorted to $INTV_{CC}$.

ILIM (Pin A5): Current Limit Programming Pin. 3-state pin ($INTV_{CC}$, float or SGND) provides 3 choices of current limit: 25A, 15A or user defined.

RUN_MSTR (Pin A6): Enable Run Control Input. When forced below 0.8V, the voltage regulator is shut off. When forced below 0.6V, all circuitry is shut off and the IC is put into a low current shutdown mode (I_Q = 125µA).

MODE/SYNC (Pin A7): Mode Selection and External Clock Input. If this pin is tied to $INTV_{CC}$, discontinuous mode is enabled at light loads. If this pin is connected to ground, forced continuous mode is selected. Driving the MODE/SYNC pin with an external clock signal will synchronize the switching frequency to the applied frequency and disable discontinuous mode operation.

FB (Pin B1): Error Amplifier Input. FB will be servoed to the REF pin voltage plus or minus any margining offset set through the serial interface.

REF (Pin B2): Reference Input and Programming Pin. The voltage at this pin is the default reference that the output is regulated to. The PMBus interface allows margining around this default voltage by up to ±25%. This pin can be driven by an external voltage or can be programmed with a resistor to ground. An internal accurate low drift 100µA current source times the external resistor sets the reference voltage.

V_{SENSE}^+ (Pin B3): V_{OUT} Positive Terminal Voltage Sense. The internal unity gain differential gain amplifier connects to the V_{OUT} positive terminal through this pin.

V_{SENSE}^- (Pin B4): V_{OUT} Negative Terminal Voltage Sense. The internal unity gain differential gain amplifier connects to the V_{OUT} negative terminal through this pin. Tying this pin to the $INTV_{CC}$ pin forces the IC to operate as a slave in a two-phase configuration.

RUN_STBY (Pin B5): Standby Mode Control Input. When forced below 0.7V, only the voltage regulator is shut off while the ADC and PMBus interface are still active. When shutoff, the ADC refresh rate is reduced to 1Hz and the IC quiescent current is reduced to 500µA. This pin sources 2.5µA. Do not pull up with a low impedance (<10kΩ).

SV_{IN} (Pin B6): Signal Input Supply. Decouple this pin to SGND with a capacitor. This pin powers the internal control circuitry. This pin is independent of V_{IN} and may be connected to the same voltage or to a higher supply voltage.

$INTV_{CC}$ (Pin B7): Internal Regulator 5V Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor. This regulator is mainly designed for internal circuits, not to be used as supply for the other ICs.

R_T (Pin C1): Oscillator Frequency. This pin provides two modes of setting the constant switching frequency. Connect a resistor from R_T pin to ground to program the switching frequency from 200kHz to 2MHz. Tying this pin to $INTV_{CC}$ enables the internal 500kHz oscillator frequency.

PIN FUNCTIONS

PGLIM (Pin C2): PGOOD Threshold Programming Pin. The voltage difference ΔV between this pin and SGND sets the V_{OUT} overvoltage threshold to V_{REF} + 0.4 • ΔV and the undervoltage threshold to V_{REF} – 0.4 • ΔV. Tying this pin to $INTV_{CC}$ sets the threshold to its default value of ±10%.

SGND (Pins C3, C4): Signal Ground. Reference setting resistor, slew rate control capacitor, and frequency setting resistor connections should return to SGND. For optimum load regulation, the SGND pin should be kelvin-connected to the PCB location between the negative terminals of the output capacitors and should not be connected through the PGND plane.

PGOOD (Pin C5): Power Good. This open-drain output is pulled down to SGND on start-up and while the output voltage is outside the power good window set by the PGLIM pin. If the output voltage increases and stays inside the power good window for more than the delay programmed at the PGFD pin, the PGOOD pin is released. If the output voltage leaves the power good window for more than 16 switching cycles the PGOOD pin is pulled down.

PGFD (Pin C6): PGOOD Deglitch Filter Delay Select. The voltage at this pin sets the delay that the output must be in regulation before the PGOOD flag is asserted. The delay can be programmed to one of eight discrete values where t_{DELAY} = 200µs • 2^N (N = 0 to 7).

ASEL (Pin D1): Serial Bus Address Configuration Input. Connect a ±1% resistor from this pin to ground in order to select the 4 LSBs of the serial bus interface address. (See Table 5).

MARGIN (Pin D2): Fast Margining Select. In the default mode when this pin is floating, the reference voltage margin offset is changed with MFR_VOUT_COMMAND through the serial interface. If this pin is pulled high, the reference voltage margin offset is immediately ramped to the value pre-stored in the MFR_VOUT_MARGIN_HIGH register. If this pin is pulled low, the reference voltage margin offset is immediately ramped to the value pre-stored in MFR_VOUT_MARGIN_LOW register.

WP (Pin D3): Write Protect Pin. An internal 10µA current source pulls the pin to 3.3V. If WP is high, the PMBus writes are restricted.

SCL (Pin D4): Serial Bus Clock Input. A pull-up resistor is required in the application.

SDA (Pin D5): Serial Bus Data Input and Output. A pull-up resistor is required in the application.

CLKOUT (Pin D6): Clock Out Signal for 2-Phase Operation. The phase of this clock is 180° with respect to the internal clock. Signal swing is from $INTV_{CC}$ to GND.

BOOST (Pin D7): Boosted Floating Driver Supplies. The (+) terminal of the booststrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

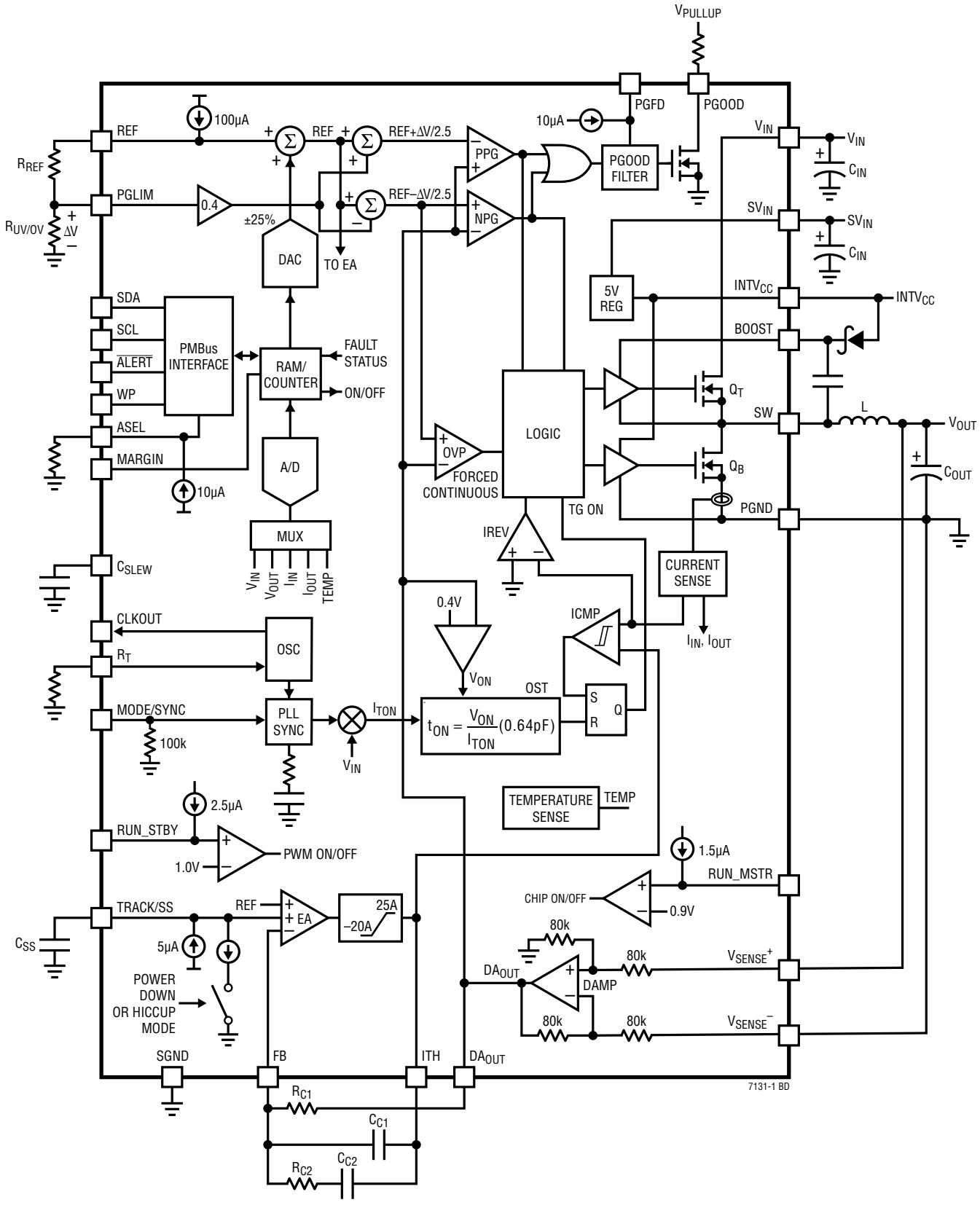
GND (Pins E1, E2, E3, E4, F1, F2, F3, F4, G1, G2, G3, G4): Power Ground. Must be soldered to PCB for electrical connection and rated thermal performance.

ALERT (Pin E5): Open Drain Digital Output. Connect the system SMBALERT interrupt signal to this pin. A pull-up resistor is required in the application.

SW (Pins E6, E7, F5, F6, F7, G5, G6, G7, H5, H6, H7, J5, J6, J7): Switching Node. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

V_{IN} (Pins H1, H2, H3, H4, J1, J2, J3, J4): Power Input Supply. V_{IN} connects to the drain of the internal N-channel power MOSFET. This pin is independent of SV_{IN} and may be connected to the same voltage or to a lower voltage supply.

BLOCK DIAGRAM



OPERATION

Table 1. LTC7131-1 Supported PMBus Commands

PMBUS COMMAND CODE	COMMAND NAME	PMBUS-DEFINED SMBUS TRANSACTION TYPE	SCALING	DATA BYTES	DESCRIPTION
0x01	OPERATION	R/W Byte		1	On/Off Command and Set Output to MFR_VOUT_MARGIN_HIGH or MFR_VOUT_MARGIN_LOW value
0x20	VOUT_MODE	Read Byte		1 or 2	Read Data Format for MFR_VOUT_COMMAND Hard-wired to VID format (0x3E), not writable
0x79	STATUS_WORD	R/W Word		2	Read Fault Status: Communication fault, PGOOD, V_{IN} UV, V_{OUT} OV, overtemperature, V_{IN} fault, V_{OUT} fault Individual faults are reset by writing a '1' to the bit position of the fault to be reset
0x88	READ_VIN	R Word	4mV/Bit	2	Read V_{IN}
0x89	READ_IIN	R Word	10mA/Bit	2	Read I_{IN}
0x8B	READ_VOUT	R Word	0.5mV/Bit	2	Read V_{OUT}
0x8C	READ_IOUT	R Word	10mA/Bit	2	Read I_{OUT}
0x8D	READ_TEMPERATURE_1	R Word	1°C/Bit	2	Read Die Temperature (°C)
0x98	PMBUS_REVISION	Read Byte		1 or 2	Read PMBus Revision = 0x22 for Rev 1.2
0xD7	MFR_IOUT_PEAK	R/W Word	10mA/Bit	2	Read highest output current observed since last restart Write will restart peak monitor routine
0xDD	MFR_VOUT_PEAK	R/W Word	0.5mV/Bit	2	Read highest output voltage observed since last restart Write will restart peak monitor routine
0xDE	MFR_VIN_PEAK	R/W Word	4mV/Bit	2	Read highest input voltage observed since last restart Write will restart peak monitor routine
0xDF	MFR_TEMPERATURE1_PEAK	R/W Word	1°C/Bit	2	Read highest temperature observed since last restart Write will restart peak monitor routine
0xE1	MFR_IIN_PEAK	R/W Word	10mA/Bit	2	Read highest input current observed since last restart Write will restart peak monitor routine
0xE3	MFR_CLEAR_PEAKS	W Byte		0, 1 or 2	Clear all peak values, write data is ignored
0xE5	MFR_VOUT_MARGIN_HIGH	R/W Word	0.1%/Bit	2	Same format as MFR_VOUT_COMMAND
0xE7	MFR_SPECIAL_ID	R Word		2	Read 16-bit value (0x40E0) that GUI will recognize as LTC7131-1
0xE8	MFR_VOUT_COMMAND	R/W Word	0.1%/Bit	2	V_{OUT} Margining Command ±25% range at 0.1%/bit in 2's compliment. Defaults to 0% at power-up
0xED	MFR_VOUT_MARGIN_LOW	R/W Word	0.1%/Bit	2	Same format as MFR_VOUT_COMMAND
0xFA	MFR_RAIL_ADDRESS	R/W Byte		1 or 2	Set Common PMBus Address (B6-B0), Clear B7 to enable. Set B7 to disable. Valid addresses are 0x00 to 0x7F.
0xFD	MFR_RESET	W Byte		0, 1 or 2	Reset PMBus Interface and ADC to Power-On State Write data is ignored
0xE9	MFR_FAULT_RESPONSE	R/W Byte		1 or 2	Set response to overvoltage and overcurrent faults: (ignore and retry).

OPERATION

Main Control Loop

The LTC7131-1 is a 25A current mode monolithic step-down regulator with PMBus Interface. The accurate 100µA current source on the REF pin allows the user to use just one external resistor to program the output voltage. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a one-shot timer, OST. When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator, ICMP, trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the bottom power MOSFET's V_{DS}. The voltage on the I_{TH} pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts this I_{TH} voltage by comparing the feedback signal, FB, from the output voltage with that of voltage on the REF pin. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference. The I_{TH} voltage then rises until the average inductor current matches that of the load current.

At low load current, the inductor current can drop to zero and become negative. This is detected by current reversal comparator, IREV, which then shuts off the bottom power MOSFET, resulting in discontinuous operation. Both power MOSFETs will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current level (~0.6V) to initiate another cycle. Discontinuous mode operation is enabled by tying the MODE pin to $INTV_{CC}$, which forces continuous synchronous operation regardless of output load.

The operating frequency is determined by the value of the R_T resistor, which programs the current for the internal oscillator. The internal phase-lock loop servos the switching regulator on-time to track the internal oscillator to force constant switching frequency. If an external clock signal is detected on the MODE/SYNC pin, the phase-lock loop will servo the on-time to track the external clock signal instead.

V_{OUT} Margining

The LTC7131-1 has an internal 9-bit DAC that provides up to ±25% adjustment at 0.1%/bit resolution around the reference voltage set at the REF pin. The digital offset value is changed with the MFR_VOUT_COMMAND command through the PMBus interface. When a change in the reference is detected, the reference is ramped (0.1%/step) from its current value to the new value at a rate set by the capacitor value connected to the C_{SLEW} pin, thus providing programmable slew rate of the V_{OUT} transition. To eliminate the latency of the PMBus transaction when faster changes are required, the LTC7131-1 can be pre-loaded with two additional offsets with the MFR_VOUT_MARGIN_HIGH and MFR_VOUT_MARGIN_LOW commands. The reference offset can then be switched between any of these three register values with the 3-state MARGIN pin. When using the MARGIN pin, the latency of the V_{OUT} transition is limited only by the chosen C_{SLEW} capacitor and the loop bandwidth of the power supply. Changes to these registers are prevented by pulling the write protect (WP) pin high.

Telemetry Readback

The LTC7131-1 has an integrated 13-bit ADC that monitors and performs conversions on the input and output voltage, input and output current, and die temperature. The values are refreshed at a 25Hz rate and are readable through the PMBus interface.

A peak monitor is also available for each of these telemetry measurements to provide that highest value measured since the start of the monitor. The monitor is reset by the MFR_CLEAR_PEAKS command, writing to the individual peak register, or de-asserting RUN_MSTR.

$INTV_{CC}$ Regulator

Power for the top and bottom MOSFET and most other internal circuitry is derived from the $INTV_{CC}$ pin. The regulated 5.0V on this pin is generated from an internal low dropout regulator. The top MOSFET driver is biased from the floating bootstrap capacitor, CB, which normally recharges during the off cycle through an external diode when the top MOSFET turns off.

Output Voltage Tracking and Soft-Start

The LTC7131-1 allows the user to program its output voltage ramp rate by means of the TRACK/SS pin. An internal 5µA pulls up the TRACK/SS pin to $INTV_{CC}$. Putting an external capacitor on TRACK/SS enables soft starting the output to prevent current surge on the input supply. If no

OPERATION

capacitor is connected or TRACK/SS pin is connected to $INTV_{CC}$, the ramp rate defaults to 1V/ms. For output tracking applications, TRACK/SS can be externally driven by another voltage source. For TRACK/SS less than the output voltage reference (set by the I_{REF} resistor and margin register), the TRACK/SS voltage will override the reference input to the error amplifier, thus regulating the feedback voltage to that of TRACK/SS pin. During this start-up time, the LTC7131-1 will operate in discontinuous mode. When TRACK/SS is above the reference voltage, tracking is disabled and the feedback voltage will regulate to the reference voltage. Either concurrent or ratiometric tracking can be implemented by connecting the track voltage to either the I_{REF} pin or the TRACK/SS pin as described in the applications section.

Output Power Good

When the LTC7131-1's output voltage is within the its power good window of the regulation point, the output voltage is good and the PGOOD pin is pulled high with an external resistor. Otherwise, an internal open-drain pull-down device (40Ω) will pull the PGOOD pin low. This window is programmed by the PGLIM pin by connecting it to a resistive divider to the REF pin. This allows the PGOOD window to be programmed as a percentage of the output voltage reference. If PGLIM is tied to $INTV_{CC}$, the PGOOD window defaults to ±10%.

The PGOOD Filter Delay pin provides a user programmable delay from output voltage good to the rising edge of PGOOD. A wide range of delays from 200µs to 25ms can be user programmed by a configuration resistor connected to the PGFD pin. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC7131-1's PGOOD falling edge includes a blanking delay of approximately 16 switching cycles.

Continuous operation is forced during OV and UV condition except during start-up when the TRACK/SS pin is ramping up to the internal reference voltage.

Master Shutdown and Standby Modes

There are three different ways to shut down the LTC7131-1: RUN_MSTR pin, RUN_STBY pin, and the ON bit of the OPERATION command.

Pulling the RUN_MSTR pin low forces the LTC7131-1 into a master shutdown state, turning off both power MOSFETs, the internal control circuitry, the ADC converter, and the PMBus interface. Also, all data written to the internal registers, such as the margin register, will be reset to the power-on state. Supply current in this mode is typically 125µA.

Pulling RUN_STBY pin low or clearing the ON bit in the OPERATION register puts the LTC7131-1 in a standby mode where the regulator is off but the ADC and PMBus are still active. In standby mode the LTC7131-1 will still respond to the PMBus host but will only refresh the telemetry data at 1Hz rate instead of 25Hz. In standby mode the supply current is 500µA. Exiting standby mode with the rising edge of the ON bit resets all faults and the $\overline{ALERT}$ pin. All data written to the internal registers, such as the margin registers, is not affected by this shutdown mode, so when RUN_STBY is re-asserted, the V_{OUT} will power back up to the last value written prior.

For the switcher to run and provide output regulation all three must be asserted, i.e. RUN_MSTR and RUN_STBY pins high and OPERATION ON bit set. At power on or master shutdown, the ON bit is automatically set in the OPERATION register. Pulling RUN_MSTR low overrides the standby controls and puts the LTC7131-1 in master shutdown.

Table 2. Shutdown Modes

INPUT CONDITIONS			ON/OFF STATES			
RUN_MSTR	RUN_STBY	ON BIT	V_{OUT}	PMBus	ADC	I_Q
High	X	0	OFF	ON	1Hz Refresh (see Note)	500µA
Low	X	X	OFF	OFF	OFF	125µA
High	High	1	ON	ON	25Hz Refresh	5mA
High	Low	X	OFF	ON	1Hz Refresh (see Note)	500µA

Note: Only V_{IN}, V_{OUT} and temperature telemetry are refreshed.

Soft Power Down

The LTC7131-1 provides the choice of two power down modes: soft off or immediate off. The desired mode is programmed with the SOFT OFF bit of the OPERATION command. If SOFT OFF bit is high when the LTC7131-1 is turned off by either the RUN_MSTR pin, RUN_STBY pin or the ON bit, the LTC7131-1 will ramp the output voltage down

OPERATION

slowly at a rate determined by the soft-start capacitor value. The SS/V_{OUT} ramp-down rate is calculated by Equation 1.

$$dV/dt = 5\mu A/C_{SS} \quad (1)$$

When the output voltage has reached zero, the LTC7131-1 will turn the drivers off and shut down. Soft off is the default power down mode.

Immediate off mode is selected if the SOFT OFF bit is low when the LTC7131-1 is turned off. In this mode, the LTC7131-1 turns its drivers off immediately and the output voltage discharge rate is a function of the output capacitor value and the load.

Short-Circuit Protection

The LTC7131-1 has a precision cycle-by-cycle current limit to prevent inductor saturation in a short-circuit condition. The valley of the inductor current is guaranteed to not exceed I_{MAX} ±10% where I_{MAX} is set by the I_{LIM} pin. The maximum cycle-by-cycle inductor current is therefore limited to I_{MAX} + 10% + ΔI_L, where ΔI_L depends on the inductor valley and operating frequency but is typically 40% of I_{MAX}. Internal control circuitry also guarantees smooth recovery with no output voltage overshoot once the short is removed.

25MHz Error Amplifier and Remote Sense Differential Amplifier

The LTC7131-1 utilizes a 25MHz error amplifier and differential amplifier for fast and accurate output voltage regulation. The operational amplifier style error amplifier allows precision tuning of the system poles and zeros for optimal transient response. The remote sense differential amplifier allows output voltage sensing at the point-of-load and thus provides very accurate regulation of the output voltage and telemetry readback regardless of load current. The sensed output voltage is available at the DA_{OUT} pin (referenced to SGND). This pin is typically connected to the FB pin which is the error amplifier "-" input. See Figure 1.

Using Separate SV_{IN}/V_{IN} Supplies

The LTC7131-1 has two supply pins: SV_{IN} that supplies the control circuitry and gate drivers and V_{IN} that supplies the power switches. SV_{IN} requires a minimum of 4.7V, while V_{IN} may be able to supply power to the load at lower voltages. To maximize the lower operating range of the supply voltage, two separate supplies can be used – a SV_{IN} supply that is > 4.7V and rated at 50mA or higher and a V_{IN} supply, rated for the load, that can be run all the way into dropout.

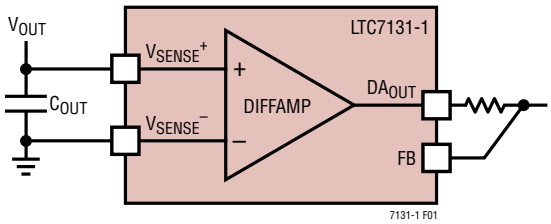


Figure 1. Differential Amplifier Connection

Thermal Warning and Thermal Shutdown

The LTC7131-1 has two levels of thermal thresholds and two levels of responses. When the internal die temperature exceeds 150°C, the overtemperature bit in the STATUS_WORD is set and the $\overline{ALERT}$ pin pulls low to alert the PMBus master. If the temperature continues to rise and exceeds 170°C, the LTC7131-1 shuts down all circuitry, including output regulation, and will no longer respond to the PMBus host. Both temperature monitors have about 20°C of hysteresis before the overtemperature condition is cleared. The temperature warning bit in the STATUS_WORD is latched and remains set until the host clears it.

2-Phase Operation

For output loads that demand more than 25A of current, two LTC7131-1's can be paralleled to run out-of-phase to provide up to 50A output current. To configure a 2-phase system, one LTC7131-1 will act as a master and the other a slave (see the schematic in the Typical Applications section). Connecting the V_{SENSE}^- pin to $INTV_{CC}$ puts the LTC7131-1 in slave mode by tri-stating its error amplifier and remote sense amplifier. The I_{TH} pins of both IC's are connected together so that both are regulating the inductor current based on the master's I_{TH} voltage. The master's CLKOUT pin is a clock waveform that is 180° out-of-phase to its internal clock. This CLKOUT can be connected to the MODE/SYNC pin of the slave to force the slave's PLL to lock onto this clock input and run out-of-phase

OPERATION

with the master. The RUN_STBY pins are also connected together as a handshaking signal between the two so that both will shutoff together in case of a fault in only one of the phases, such as overtemperature condition.

See the Applications Information section for further details regarding 2-phase operation.

Discontinuous/Forced Continuous Operation

The LTC7131-1 can operate in one of two modes selectable with the MODE/SYNC pin: discontinuous mode or forced continuous mode. Connecting the MODE/SYNC pin to $INTV_{CC}$ selects discontinuous mode. Discontinuous mode is selected when high efficiency at very light loads is desired. In this mode, when the inductor current reverses, the bottom MOSFET turns off to minimize the efficiency loss due to reverse current flow. This reduces the conduction loss and slightly improves the efficiency. As the load reduces, the driver switching frequency drops in proportion to the load, which further improves efficiency by minimizing gate charge losses.

Forcing the MODE/SYNC pin low enables forced continuous mode operation. In forced continuous mode, the bottom MOSFET is always on when the top MOSFET is off, allowing the inductor current to reverse at low currents. This mode is less efficient due to conduction and switching losses, but has the advantage of better transient response at low currents, constant frequency operation, and the ability to maintain regulation when sinking current.

During soft-start, the LTC7131-1 forces the controller to operate in discontinuous mode until the soft-start voltage reaches the internal reference to guarantee smooth startup into a precharged output capacitor. During margining transitions and overvoltage conditions, however, the LTC7131-1 always operates in forced continuous mode to allow the switcher to sink current.

Fault Response Programming

When an output overvoltage or overcurrent condition occurs, the LTC7131-1's response to the fault can be programmed using the MFR_FAULT_RESPONSE command. Two fault response modes are available: (1) ignore or (2) hiccup mode. The response can be independently programmed for each type of fault.

If ignore option is chosen, the LTC7131-1 will attempt to correct the fault using the control loop as it would any time the output goes out of regulation.

If hiccup mode is chosen, a fault timer is started when the fault is detected. During this time, the control loop tries to correct the fault. If the fault is still present after the 100µs timer delay, the drivers are turned off for a period equal to about 10× the soft-start time (set by the soft-start capacitor) before turning the drivers back on and attempting to regulate again (see timing diagram in Figure 2). The LTC7131-1 will continue these restart cycles indefinitely until the fault is removed.

An overvoltage fault response is initiated when the output voltage exceeds the upper PGOOD threshold. An overcurrent fault is initiated when the ITH voltage reached the clamp set by the ILIM pin.

Undervoltage Lockout

The LTC7131-1 has two functions that help protect the controller in case of undervoltage conditions. A precision

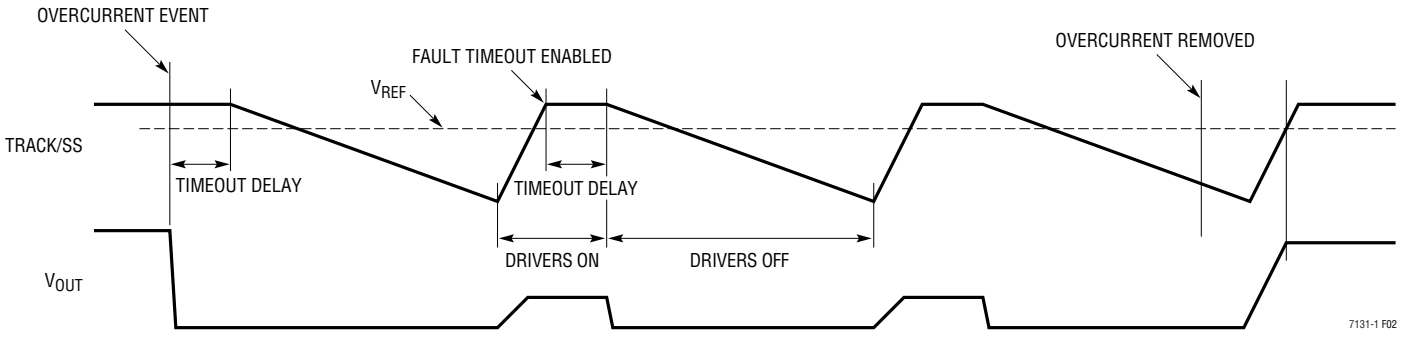


Figure 2. Fault Response Timing to Overcurrent Event

OPERATION

UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.9V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 0.32V of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 0.9V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. The RUN comparator itself has about 80mV of hysteresis. For accurate V_{IN} undervoltage detection, V_{IN} needs to be higher than 4.75V.

SERIAL INTERFACE

The LTC7131-1 serial interface is a PMBus compliant slave device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using an external resistor. In addition the LTC7131-1 always responds to the global broadcast address of 0x5A or 0x5B (7 bit). The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte and 6) read word. The PMBus write operations are not acted upon until a complete valid message is received by the LTC7131-1 including the STOP bit.

Communication Failure

Attempts to access unsupported commands or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_WORD command and the $\overline{\text{ALERT}}$ pin is pulled low.

Device Addressing

The LTC7131-1 offers four different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

Global addressing provides a means of the PMBus master to address all LTC7131-1 devices on the bus. The LTC7131-1 global address is fixed 0x5A or 0x5B (7 bit) or 0xB4 or 0xB6 (8 bit) and cannot be disabled.

Device addressing provides the standard means of the PMBus master communicating with a single instance of an LTC7131-1. The value of the device address is set by the ASEL configuration pin. Rail addressing provides a means of the PMBus master addressing a set of channels connected to the same output rail, simultaneously. This is similar to global addressing, however, the PMBus address can be dynamically assigned by using the MFR_RAIL_ADDRESS command. It is recommended that rail addressing should be limited to command write operations.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts.

Fault Status

The STATUS_WORD and $\overline{\text{ALERT}}$ pin provide fault status information of the LTC7131-1 to the host.

Bus Timeout Failure

The LTC7131-1 implements a timeout feature to avoid hanging the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 25ms or the LTC7131-1 will tri-state the bus and ignore the given data packet. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), and all data bytes.

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTC7131-1 supports the full PMBus frequency range from 10kHz to 400kHz.

Similarity Between PMBus, SMBus and I^2C 2-Wire Interface

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I^2C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I^2C byte commands because PMBus/SMBus provide time-outs to prevent bus hangs and optional packet error

OPERATION

checking (PEC) to ensure data integrity. In general, a master device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general purpose I²C controller is used, check that repeat start is supported.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.2: Paragraph 5: Transport.

For a description of the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I²C.

PMBus Serial Interface

The LTC7131-1 communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram, Figure 3, shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC7131-1 is a slave device. The master can communicate with the LTC7131-1 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following PMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word
- Alert Response Address

Figure 5 through Figure 8 illustrate the aforementioned PMBus protocols. All transactions support GCP (group command protocol).

Figure 4 is a key to the protocol diagrams in this section.

A value shown below a field in the following figures is a mandatory value for that field.

The data formats implemented by PMBus are:

- Master transmitter transmits to slave receiver. The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte. At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format. During a change of direction within a transfer, the master repeats both a start condition and the slave address but with the R/$\overline{W}$ bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

Examples of these formats are shown in Figure 5 through Figure 9.

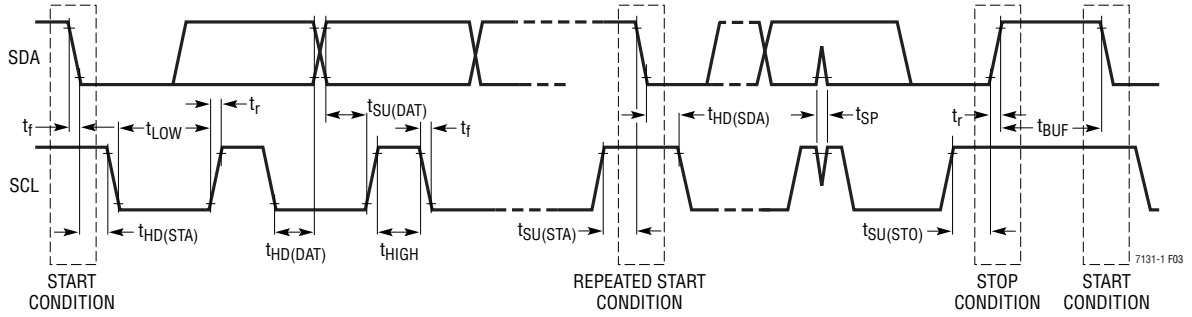


Figure 3. Timing Diagram

OPERATION

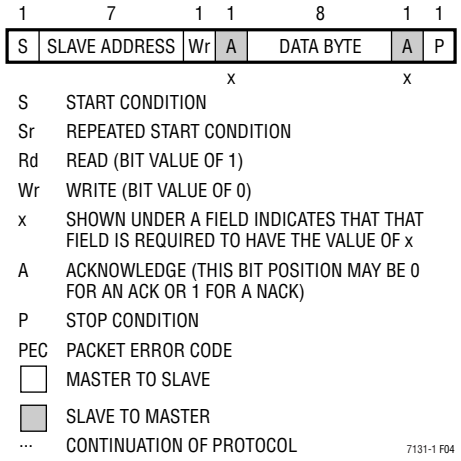


Figure 4. PMBus Packet Protocol Diagram Element Key

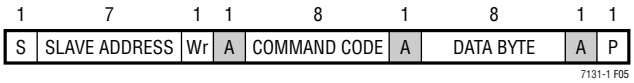


Figure 5. Write Byte Protocol

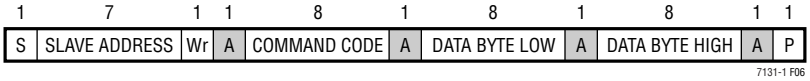


Figure 6. Write Word Protocol

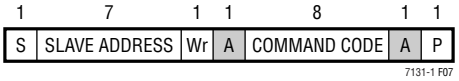


Figure 7. Send Byte Protocol

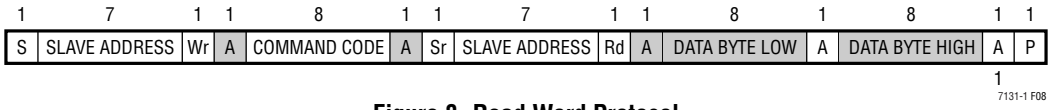


Figure 8. Read Word Protocol

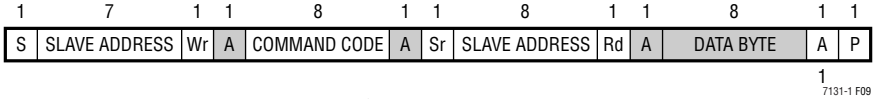


Figure 9. Read Byte Protocol

APPLICATIONS INFORMATION

The basic LTC7131-1 application circuit is shown in Figure 10.

Current Limit Programming

The maximum current limit for the controller can be set to any value in the range of 10A to 25A by the ILIM pin. For a 25A limit, tie ILIM to $INTV_{CC}$. For a 15A limit, tie ILIM to SGND. For other limits, use Equation 2 to choose the required ILIM voltage

$$\text{Valley Current Limit (A)} = 20 \bullet V_{ILIM} + 1 \quad (2)$$

Then use a resistive divider connected to $INTV_{CC}$ to set ILIM to the chosen voltage.

Note that this current limit corresponds to the valley of the inductor ripple so the maximum load current will be higher by ΔI/2.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage. The operating frequency of the LTC7131-1 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by Equation 3.

$$R_T(\Omega) = \frac{1.235 \bullet 10^{10}}{f_{OSC}} - 950 \quad (3)$$

Frequencies as high as 2MHz are possible, as long as the minimum on-time requirement is met (see next section). Tying the RT pin to $INTV_{CC}$ sets the default internal operating frequency to 480kHz ±15%.

The LTC7131-1's internal oscillator can be synchronized to an external frequency by applying a square wave clock signal to the MODE/SYNC pin. During synchronization, the top switch turn-on is locked to the rising edge of the external frequency source. The synchronization frequency range is 250kHz to 2MHz. During synchronization, discontinuous operation is disabled.

The internal PLL has a synchronization range of ±30% around its programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the R_T programmed frequency.

When using the R_T pin to program the oscillator frequency, a square wave clock that is running 180° out-of-phase with the internal oscillator is available at the CLKOUT pin for connection to a second LTC7131-1 for 2-phase operation (see the 2-Phase section).

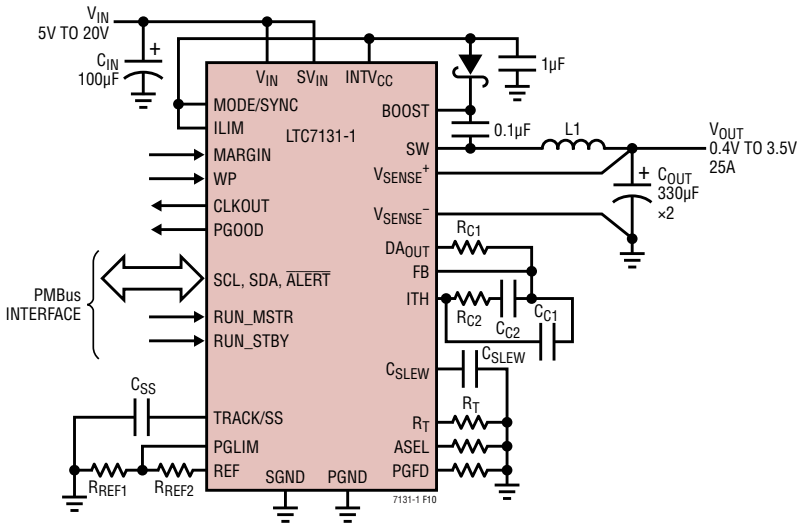


Figure 10. 25A Step-Down Regulator

APPLICATIONS INFORMATION

Minimum Off-Time and Minimum On-Time Considerations

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the LTC7131-1 is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 100ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is given by Equation 4.

$$V_{IN(MIN)} = V_{OUT} \bullet \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}} \quad (4)$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 75ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of Equation 5.

$$DC_{MIN} = f \bullet t_{ON(MIN)} \quad (5)$$

where $t_{ON(MIN)}$ is the minimum on-time. As the Equation 5 shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of severe consequences. As the sections on inductor and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current given by Equation 6.

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 30-40% of $I_{OUT(MAX)}$. This is especially important at low V_{OUT} operation where V_{OUT} is 1.8V or below. Care must be given to choose an inductance value that will generate a big enough current ripple so that the chip's valley current comparator has enough signal-to-noise ratio to force constant switching frequency. Meanwhile, also note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to Equation 7.

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (7)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that LTC7131-1 inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements

APPLICATIONS INFORMATION

and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, TDK, Wurth Elektronik and Coilcraft. Refer to Table 3 for more details.

Table 3. Representative Surface Mount Inductors

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
EATON FP1007 R3 Series				
0.15	0.29	76	10.2 x 7.8	7.3
0.17	0.29	66	10.2 x 7.8	7.3
0.22	0.29	50	10.2 x 7.8	7.3
Wurth 744308 Series				
0.15	0.18	79	10.2x8.10	8
0.17	0.18	68	10.2x8.10	8
0.18	0.18	63	10.2x8.10	8

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by Equation 8.

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1} \quad (8)$$

Equation 8 has a maximum at $V_{IN} = 2V_{OUT}$, where

$$I_{RMS} \cong I_{OUT}/2$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by Equation 9.

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \bullet f \bullet C_{OUT}} + ESR \right) \quad (9)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints. Their relatively low value of bulk capacitance may require multiples in parallel.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

APPLICATIONS INFORMATION

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2 to 3 times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately given by Equation 10.

$$C_{OUT} \approx 2.5 \frac{\Delta I_{OUT}}{f_O \bullet V_{DROOP}} \quad (10)$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 22µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the V_{IN} pins as possible.

Thermal Considerations

In some applications where the LTC7131-1 is operated at high ambient temperature, high V_{IN}, high switching frequency and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part.

To avoid the LTC7131-1 from exceeding the maximum junction temperature, current rating shall be derated in accordance to Ambient Temperature vs Maximum Load Current in the Typical Performance Characteristics.

The junction to ambient thermal resistance will vary depending on the size amount of heat sinking copper on the PCB board where the part is mounted, as well as the amount of air flow on the device. Figure 11 and Figure 12 show temperature derating with both heat sink and airflow. Use the READ_TEMPERATURE_1 command to check the die temperature at worst-case operating conditions as a final check.

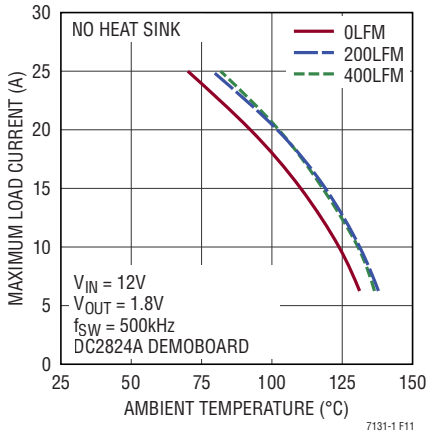


Figure 11. Temperature Derating Curve Based on the DC2824A Demo Board

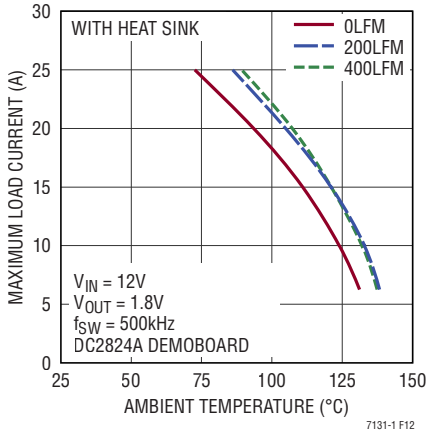


Figure 12. Temperature Derating Curve Based on the DC2824A Demo Board

Table 4 and Table 5 provide heat sink and thermal conductive adhesive tape information.

Table 4. Heat Sink Manufacturer (Thermally Conductive Adhesive Tape Pre-Attached)

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Cool Innovations	03-0202035U	www.coolinnovations.com

Table 5. Thermally Conductive Adhesive Tape Vendor

THERMALLY CONDUCTIVE ADHESIVE TAPE MANUFACTURER	PART NUMBER	WEBSITE
Chomerics	T411	www.chomerics.com

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its LTC7131-1 steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of output capacitors. The availability of the I_{TH} pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The I_{TH} external components (R_{C1}, C_{C1}, C_{C2}) shown in the Figure 10 circuit provides an adequate starting point for most applications. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft-starting.

Calculating Compensation Values

If the “trial and error” approach described in the previous section doesn’t result in adequate transient performance, the procedure described in this section can be used to calculate more precise compensation component values to achieve a desired bandwidth and phase margin. This procedure is also helpful if the output capacitor type is very different than the one specified in the application circuits or if a Type 3 compensation network is required. A Type 3 compensation network includes the additional components R_{C3} and C_{C3} shown in Figure 13.

1. Choose the crossover frequency. For best performance, the crossover frequency should be as high as possible but not greater than about 20% of the switching frequency.
2. Plot Gain and Phase of the modulator and output filter. The modulator and output filter is the portion of the loop from the error amp output (I_{TH}) to the regulator output (V_{OUT}). To do this, insert a 10Ω to

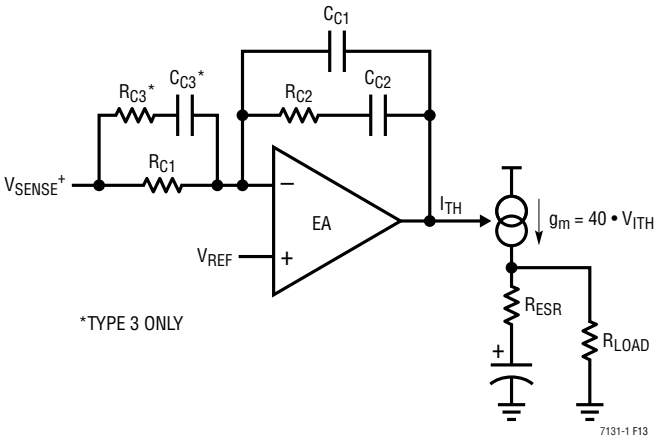


Figure 13. PSPICE Model of a LTC7131-1 Current Mode Regulator

APPLICATIONS INFORMATION

50Ω resistor between the output capacitor and the V_{SENSE}^+ pin (this is R7 on the DC2824 demo board). Then use a network analyzer to inject an AC signal across this resistor and plot the Gain and Phase. If a network analyzer is not available, a close approximation can obtained with a PSPICE simulator using the LTC7131-1 power supply model shown in Figure 13. The error amplifier EA can be modeled as an ideal op amp (for crossover frequencies < 200kHz) and the inductor as a voltage controlled current source. The gain/phase plot should look similar to Figure 14.

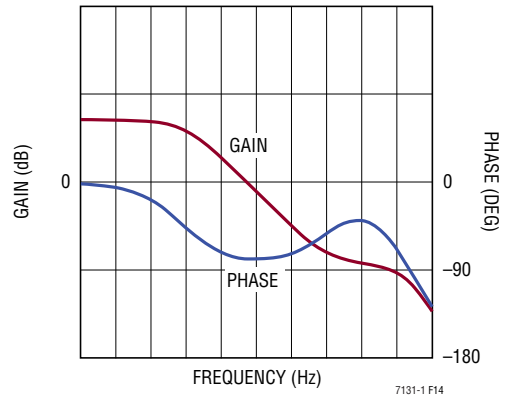


Figure 14. Transfer Function of Buck Modulator

3. Calculate the component values. Once the gain and phase are known, note the gain (GAIN, in dB) and phase (PHASE, in degrees) at the crossover frequency. The compensation components can then be calculated to make the loop gain (V_{SENSE}^+ to V_{OUT}) equal to 0dB and the phase margin equal to 60° at this frequency. Use Equation 11 and Equation 12 to calculate the component values. Normally Equation 11 (the Type 2 Loop) will provide the required BOOST for 60° phase margin. If not, use Equation 12 (the Type 3 Loop).

4. Add the calculated components to the LTC7131-1 circuit and check the load step response. If not adequate, the components values may need to be tweaked further or recalculated with a lower crossover frequency until the desired response is obtained.

   R_{C1} = A convenient resistor value ~1kΩ.

   f = chosen crossover frequency

   $G = 10^{(GAIN/20)}$ (this converts GAIN in dB to G in absolute gain)

   BOOST = –(PHASE + 30°)

Type 2 Loop:

$$k = \tan\left(\frac{BOOST}{2} + 45^\circ\right)$$
$$C_{C1} = \frac{1}{2\pi \bullet f \bullet G \bullet K \bullet R_{C1}}$$
$$C_{C2} = C_{C1}\left(K^2 - 1\right) \quad (11)$$
$$R_{C2} = \frac{K}{2\pi \bullet f \bullet C_{C2}}$$

Type 3 Loop:

$$k = \tan\left(\frac{BOOST}{4} + 45^\circ\right)$$
$$C_{C1} = \frac{1}{2\pi \bullet f \bullet G \bullet RC1}$$
$$C_{C2} = C_{C1}(K - 1)$$
$$R_{C2} = \frac{\sqrt{K}}{2\pi \bullet f \bullet C_{C2}} \quad (12)$$
$$R_{C3} = \frac{R_{C1}}{K - 1}$$
$$C3 = \frac{1}{2\pi f\sqrt{K} \bullet R_{C3}}$$

APPLICATIONS INFORMATION

Output Voltage Programming

The output voltage is set by an external resistor according to Equation 13.

$$V_{OUT} = 100\mu A \bullet R_{REF} \quad (13)$$

where R_{REF} is the total resistance between REF pin and SGND. A capacitor (0.1µF max) connected from REF to SGND is recommended for noise filtering. For accurate PGOOD reporting at startup, choose $C_{REF} < 10C_{SS}$.

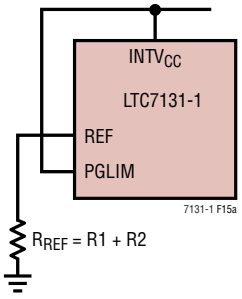
Programming PGOOD Threshold and Filter Delay

The upper and lower Power Good threshold default to ±10% when the PGLIM pin is tied to $INTV_{CC}$ (see Figure 15a). However, if a narrower or wider window is desired, these windows can be programmed to any desired value in the range of 5% to 40%.

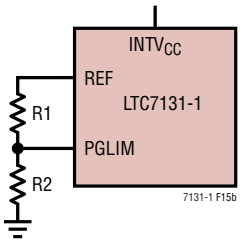
The PGOOD upper/lower threshold is programmed by replacing the single resistor on the REF pin with a resistor divider as follows (see Figure 15b):

Reference Voltage = 100µA • (R1+R2)

PGOOD Window = ±40% • R2/(R1+R2)



(a) PGOOD Window Set to ±10% Default



(b) PGOOD Window Set by R1/R2

Figure 15. PGOOD Window

The PGOOD window is always centered on the DAC adjusted reference voltage, thus the center will move to the new reference voltage when margined up or down.

The falling PGOOD (power good to power bad) is filtered and delayed by 16 clock cycles, thus giving the loop 16 switching cycles to recover from the power bad condition before pulling the PGOOD pin low.

The rising PGOOD (power bad to power good) filter delay is user programmable by a configuration resistor at the PGFD pin and is programmable to one of 8 possible delays from 200µs to 25.6ms as shown in Table 6. Minimum delay of 200µs can be set by grounding the PGLIM pin and maximum delay of 25.6ms can be set by tying PGLIM to $INTV_{CC}$.

The PGFD pin is sampled only at power on and at initialization after the rising edge of RUN_MSTR, RUN_STBY or the OPERATION register ON bit. Changes to PGFD will not take effect until one of these events occur.

Table 6. PGFD Resistor Selection

PGFD RESISTOR	PGOOD DELAY
0Ω	200µs
28kΩ	400µs
46.4kΩ	800µs
64.9kΩ	1.6ms
84.5kΩ	3.2ms
102kΩ	6.4ms
121kΩ	12.8ms
Open or Short to $INTV_{CC}$	25.6ms

Address Selection (ASEL pin)

The LTC7131-1 slave address is selected by the ASEL pin. The upper four bits of the address are hardwired internally to 0100 and the lower three bits are programmed by a resistor connected between the ASEL and SGND (see Table 7). This allows up to 8 different LTC7131-1's on a single board. The LTC7131-1 will also respond to the Global Address 0x5A and the 7-bit address stored in the MFR_RAIL_ADDRESS register.

The ASEL pin is sampled only at power on and at initialization after the rising edge of RUN_MSTR, RUN_STBY or OPERATION register ON bit. Changes to ASEL will not take affect until one of these events occur.

APPLICATIONS INFORMATION

Table 7. ASEL Resistor Selection

ASEL RESISTOR	SLAVE ADDRESS
0Ω	0100000
28kΩ	0100001
46.4kΩ	0100010
64.9kΩ	0100011
84.5kΩ	0100100
102kΩ	0100101
121kΩ	0100110
Open or short to $INTV_{CC}$	0100111

Margining/C_{SLEW} Selection/Margin Pin

Writing to the MFR_VOUT_COMMAND register via the PMBus allows the adjustment of the V_{OUT} reference up to ±25% around the voltage at the REF pin. This voltage can be adjusted in 0.1% increments by writing the appropriate 9-bit two's complement value to the register. The MFR_VOUT_MARGIN_HIGH and MFR_VOUT_MARGIN_LOW register can also be used to adjust the V_{OUT} reference value by selecting the desired register with the MARGIN pin or the OPERATION command as specified in Table 8.

Table 8. V_{OUT} Margining with the MARGIN Pin and OPERATION Command

MARGIN PIN	OPERATION BITS [5:4]		V_{OUT} REFERENCE
	BIT 5	BIT 4	
<0.4V	X	X	= [1 + MFR_VOUT_MARGIN_LOW(%)] • V_{REF}
>1.2V	X	X	= [1 + MFR_VOUT_MARGIN_HIGH(%)] • V_{REF}
Hi-Z	0	0	= [1 + MFR_VOUT_COMMAND(%)] • V_{REF}
Hi-Z	0	1	= [1 + MFR_VOUT_MARGIN_LOW(%)] • V_{REF}
Hi-Z	1	0	= [1 + MFR_VOUT_MARGIN_HIGH(%)] • V_{REF}
Hi-Z	1*	1*	= [1 + MFR_VOUT_COMMAND(%)] • V_{REF}

* Setting both bits 4 and 5 high at the same time is illegal and will be ignored.

Pre-loading the registers and using the MARGIN pin provides fast margining by eliminating the latency inherent to serial bus communication. Once the registers are loaded the output voltage change is limited only by the loop bandwidth and the slew rate capacitor (C_{SLEW}).

The C_{SLEW} pin provides slew rate limiting during reference voltage changes. When the reference is changed by either the MARGIN pin, OPERATION command, or writing new values to the register, the LTC7131-1 counts up or down from the current value in the register to the new value at 0.1% per step. The step duration is set by the C_{SLEW} capacitor. The slew rate during the transition is given by Equation 14.

$$SR = \frac{0.1}{C_{SLEW}(nF) + 0.0043} \%/ms \quad (14)$$

If the C_{SLEW} pin is left open, SR defaults to 23%/ms. The slew rate limit can be disabled if desired by tying the C_{SLEW} pin to $INTV_{CC}$. When disabled, the reference is immediately stepped from old value to new value in <100ns.

Differential Amplifier

The LTC7131-1 has true remote voltage sense capability. The sense connections, V_{SENSE}^+ and V_{SENSE}^-, should be returned from the load, back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PC traces as well as ground loop disturbances. However, it is still important to avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, the V_{SENSE}^+ and V_{SENSE}^- traces should be shielded by a low impedance ground plane to maintain signal integrity.

The LTC7131-1 differential amplifier has 160kΩ input impedance on V_{SENSE}^+. It is designed to be connected directly to the output. The output of the differential amplifier, DA_{OUT}, connects to the FB pin to set the output voltage.

Soft-Start

After the LTC7131-1 is turned on or power applied and finishes its ~500µs initialization sequence, the chip enters a soft start-up state. The type of soft startup behavior is set by the TRACK/SS pin:

1. Floating the TRACK/SS selects the internal soft-start circuit. This circuit ramps the output voltage to the final value within 1ms.
2. If a longer soft-start period is desired, it can be set externally with a capacitor on the TRACK/SS pin. The TRACK/SS pin reduces the value of the internal

APPLICATIONS INFORMATION

reference at FB until TRACK/SS charges above the REF pin voltage. The external soft-start duration can be calculated by Equation 15.

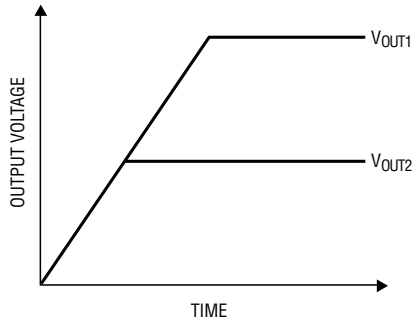
$$t_{SS} = \frac{V_{REF} \bullet C_{SS}}{5\mu A} \quad (15)$$

3. The TRACK/SS pin can be used to track the output voltage of another supply. Using the TRACK/SS pin for tracking is only allowed when the hiccup mode is disabled (see Fault Response Programming section) since the TRACK/SS pin is used for fault response timing.

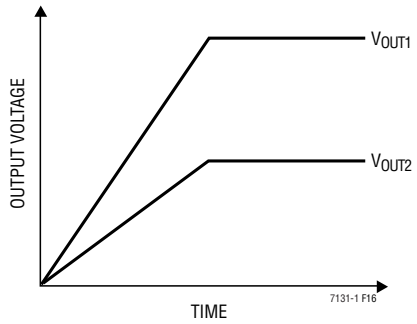
Regardless of either internal or external soft-start state, the MODE pin is ignored and soft-start will always be in discontinuous mode until SS voltage reaches the programmed V_{OUT} reference voltage for the first time.

TRACKING

Using the TRACK/SS or the REF pin, two types of tracking/sequencing can be used for the LTC7131-1 (see Figure 16). For ratiometric tracking, V_{OUT} will always track a ratio of the input tracking voltage. In coincident tracking, V_{OUT} will track a ratio of the input tracking voltage until $V_{OUT} \geq V_{REF}$, then V_{OUT} is regulated to V_{REF}. Also, with ratiometric tracking, the V_{OUT} can be adjusted with the margin commands and MARGIN pin relative to the tracking voltage. With coincident tracking, V_{OUT} can only be adjusted relative to V_{REF} when $V_{MASTER} \geq V_{REF}$.



(a) Coincident Tracking



(b) Ratiometric Tracking

Figure 16. Two Different Modes of Output Voltage Tracking

For coincident tracking, be aware that the PGOOD window is always centered around the DAC adjusted REF pin voltage, not the TRACK/SS pin voltage.

Ratiometric Tracking

To implement ratiometric tracking (Figure 17a and Figure 17b) the controlling voltage, V_{MASTER} is connected to the REF pin. This source must be able to sink the 100µA I_{REF} current. Using the REF pin allows V_{OUT} to be adjusted with the margining commands and MARGIN pin. For $V_{MASTER} > V_{SLAVE}$ connect V_{MASTER} to the REF pin thru a resistive divider. The relationship of V_{MASTER} to V_{SLAVE} is given by Equation 16.

$$V_{MASTER} = V_{SLAVE} \bullet \left(1 + \frac{R1}{R2}\right) - R1 \bullet 100\mu A \quad (16)$$

Note that the 100µA I_{REF} current requires $V_{MASTER} > R1 \bullet 100\mu A$ before V_{SLAVE} starts rising above 0V. Choose a low value for R1 to minimize this offset.

For $V_{MASTER} < V_{SLAVE}$ connect V_{MASTER} directly to REF pin. The ratio of V_{MASTER} to V_{SLAVE} is given by Equation 17.

$$\frac{V_{MASTER}}{V_{SLAVE}} = \frac{R1}{R1+R2} \quad (17)$$

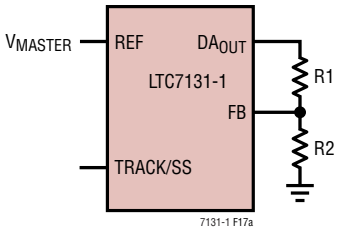
Coincident Tracking

To implement coincident tracking with $V_{MASTER} \geq V_{SLAVE}$ (Figure 17c) connect V_{MASTER} to the TRACK/SS pin directly or with a resistive divider given by Equation 18.

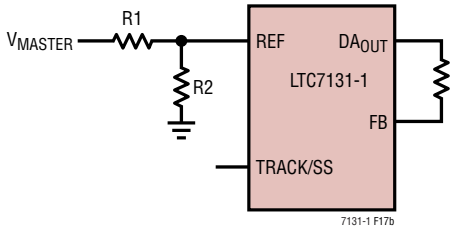
$$\frac{V_{MASTER}}{V_{SLAVE}} = \frac{R1}{R1+R2} \quad (18)$$

V_{OUT} will follow V_{MASTER} (or a ratio of it as set by R1/R2) until $V_{MASTER} > V_{REF}$ at which time V_{OUT} is regulated to V_{REF}. Do not let TRACK/SS pin exceed V_{REF} + 0.3V due to internal clamp.

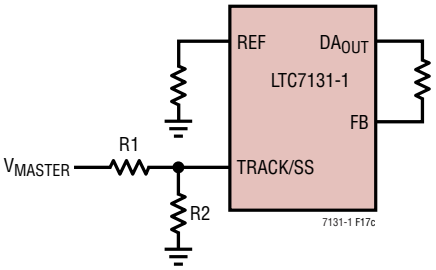
APPLICATIONS INFORMATION



(a) Slave IC Circuit for Ratiometric Tracking and $V_{MASTER} \leq V_{SLAVE}$



(b) Slave IC Circuit for Ratiometric Tracking and $V_{MASTER} \geq V_{SLAVE}$



(c) Slave IC Circuit for Coincident Tracking and $V_{MASTER} \geq V_{SLAVE}$

Figure 17. Slave IC Circuits

DDR Mode

The LTC7131-1 can both sink and source current if the MODE/SYNC pin is set to forced continuous mode. Current sinking is limited to $-20A+\Delta I_L/2$. An external reference voltage connected to the REF pin can be used to set the output voltage. The output voltage can be margined by ±25% in the same way as a resistor programmed reference.

$INTV_{CC}$ (LDO)

The LTC7131-1 features a true PMOS LDO that supplies power to $INTV_{CC}$ from the SV_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC7131-1's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5V when SV_{IN} is greater than 5.5V. $INTV_{CC}$ can supply a peak current of 100mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers. High input voltage applications in which the internal MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7131-1 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, also known as the driver current, is supplied by the 5V LDO. The gate charge current is dependent on operating frequency as discussed on Efficiency Considerations section. The power dissipation for the IC in this case is equal to SV_{IN} • ($INTV_{CC}$ current). For example, the LTC7131-1 $INTV_{CC}$ current is about 27.5mA from a 20V supply at 500kHz in the BGA package given by Equation 19.

$$P_D = 20V \bullet 27.5mA = 0.55W \quad (19)$$

For applications where the main input power is 5V, tie the SV_{IN}, V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 18 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds 4.5V to prevent excessive dissipation in the internal Power MOSFETs due to high $R_{DS(ON)}$.

APPLICATIONS INFORMATION

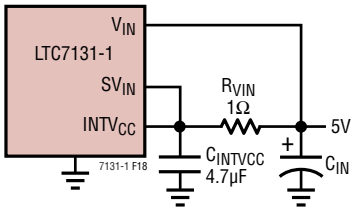


Figure 18. Setup for a 5V Input

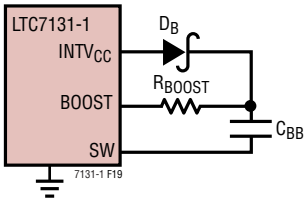


Figure 19. Using Boost Resistor

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltages for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged through external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply given by Equation 20.

$$V_{BOOST} = V_{IN} + V_{INTVCC} - V_{DB} \quad (20)$$

The value of the boost capacitor, C_B, needs to store approximately 100 times the gate charge required by the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

For applications that require high V_{IN} and high output current, in order to minimize SW node ringing and EMI, connect a 2Ω to 10Ω resistor R_{BOOST} in series with the BOOST pin. Make the C_B and D_B connections on the other side of the resistor. This series resistor helps to slow down the SW node rise time, limiting the high d_I/d_t current through the top MOSFET that causes SW node ringing (see Figure 19).

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%.

It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed by Equation 21.

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots) \quad (21)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC7131-1 circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) is given by Equation 22.

   $$R_{SW} = (R_{DS(ON)}TOP)(DC) + (R_{DS(ON)}BOT)(1\text{-}DC) \quad (22)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Electrical Characteristics section. Thus to obtain I^2R losses use Equation 23

   $$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L) \quad (23)$$

2. The $INTV_{CC}$ current is the sum of the power MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode,

APPLICATIONS INFORMATION

$I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. Since $INTV_{CC}$ is a low dropout regulator output powered by SV_{IN}, its power loss equals to Equation 24.

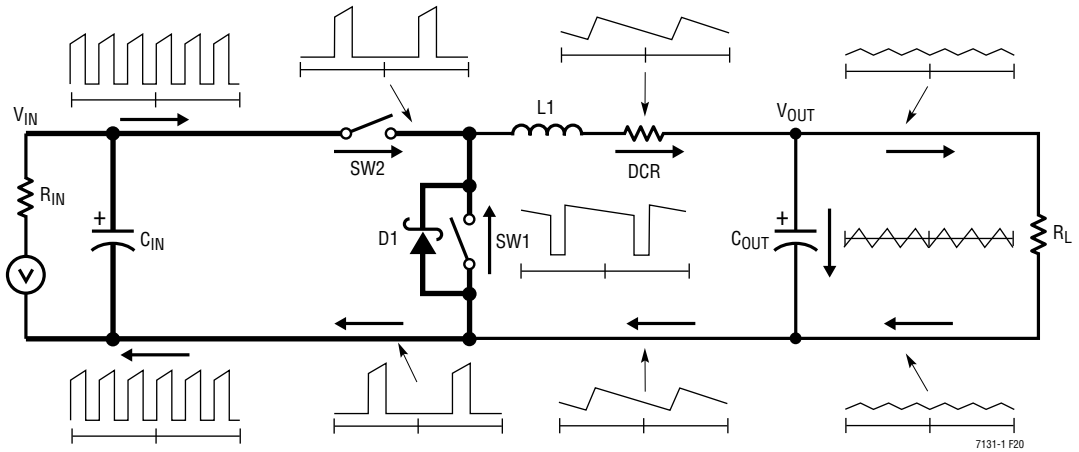
$$P_{LDO} = SV_{IN} \bullet I_{INTVCC} \quad (24)$$

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. Other losses including diode conduction losses during dead-time and inductor core losses which generally account for less than 2% total additional loss.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 20. Check the following in the PC layout:

1. The $INTV_{CC}$ decoupling capacitor should be placed immediately adjacent to the IC between the $INTV_{CC}$ pin and PGND plane. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the bottom MOSFETs. An additional 4.7µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet.
2. Connect the remote sense pins, V_{SENSE}^+ and V_{SENSE}^-, directly to the point where maximum V_{OUT} accuracy is desired. The two traces should be routed as close together as possible.
3. Do the (+) plates of C_{IN} connect to the drain of the topside MOSFET as closely as possible? This capacitor provides the pulsed current to the MOSFET.
4. Keep the switching nodes, SW, BOOST away from sensitive small-signal nodes (REF, DA_{OUT}, V_{SENSE}^+, V_{SENSE}^-, FB). Ideally the SW, and BOOST printed circuit traces should be routed away and separated from the IC and especially the *quiet* side of the IC. Separate the high d_V/d_t traces from sensitive small-signal nodes with ground traces or ground planes.
5. Use a low impedance source such as a logic gate to drive the MODE/SYNC pin and keep the lead as short as possible.
6. Figure 20 illustrates all branch currents in a switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these



BOLD LINES INDICATE HIGH, SWITCHING CURRENTS. KEEP LINES TO A MINIMUM LENGTH

Figure 20. Branch Current Waveforms

APPLICATIONS INFORMATION

loops just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the *noise* generated by a switching regulator. The GND terminations and Schottky diode should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. External OPTI-LOOP® compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

7. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The FB and ITH traces should be as short as possible. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
8. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

Design Example

As a design example of the front page circuit for a single channel high current regulator, assume V_{IN} = 12V(nominal), V_{IN} = 20V(maximum), V_{OUT} = 1.5V, I_{MAX} = 25A, and f = 500kHz (see front page schematic).

The value of R_{REF} can be determined by solving Equation 25.

$$R_{REF} = \frac{1.5V}{100\mu A} = 15k \quad (25)$$

A value of 15k, 0.5% will be selected for R_{REF}. Calculate the timing resistor using Equation 26.

$$R_T = \frac{1.235 \bullet 10^{10}}{500000} - 950 = 23.8k \quad (26)$$

Connect the ILIM pin to $INTV_{CC}$ to choose the 25A current limit setting.

The inductance value is based on a 40% maximum ripple current assumption (10A). The highest value of ripple current occurs at the maximum input voltage calculated by Equation 27.

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (27)$$

This design will require 0.25µH. The Würth 744308025, 0.25µH inductor is chosen. At the nominal input voltage (12V), the ripple current is given by Equation 28.

$$\Delta I_{L(NOM)} = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right) \quad (28)$$

It will have 10.5A (42%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current, or around 30A.

The minimum on-time occurs at the maximum V_{IN}, and should not be less than 90ns (Equation 29).

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}f} = \frac{1.5V}{20V(500kHz)} = 150ns \quad (29)$$

C_{OUT} is chosen with an equivalent ESR of 4.5mΩ for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately given by Equation 30.

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) \approx 0.0045\Omega \bullet 10A = 45mV_{P\text{-}P} \quad (30)$$

Further reductions in output voltage ripple can be made by placing a 100µF ceramic capacitor across C_{OUT}.

APPLICATIONS INFORMATION

Assuming worst-case conditions of V_{IN} = 12V, C_{IN} should be selected for a maximum current rating of Equation 31.

$$I_{RMS} = 25A \bullet \frac{1.5V}{12V} \bullet \sqrt{\left(\frac{20V}{1.5V} - 1\right)} = 8.25A_{RMS} \quad (31)$$

Finally, define the soft start-up time choosing the proper value for the capacitor and the resistor connected to TRACK/SS. If we set minimum t_{SS} = 5ms, Equation 32 can be solved.

$$C_{SS} = \frac{5\mu A \bullet 5ms}{1.5V} = 16.7nF \quad (32)$$

The standard value of 18nF guarantees the minimum soft-start up time of 5ms.

2-Phase Operation

Using two LTC7131-1's as a 2-phase regulator to supply 50A loads was discussed in the Operation section. A few more details need to be brought to the user's attention to ensure correct operation:

1. PMBus connection and READ_IIN/IOUT: Although the 2-phase regulator will operate fine with the PMBus interface connected to the master only, the READ_IOUT and READ_IIN measured values will only be available for the phase(s) that are connected. Since each phase's LTC7131-1 supplies half the load in a 2-phase converter, the value read (if from the master only) needs to be doubled to obtain the total I_{OUT} or I_{IN} value. Because of slight differences in tracking between phases due to IC and inductor tolerances, a more accurate reading will be obtained by connecting to both phases so that total I_{OUT} and I_{IN} can be computed by summing each phase's contribution.
2. Slave PGOOD/ALERT status and margining: When the master and slave are monitoring the same output, it is sufficient to monitor the master's PGOOD and ALERT pins only. The PGOOD/ALERT pins from both master and slave can also be wire OR'ed if desired. However, if the output voltage is margined with the PMBus interface, the PGOOD/ALERT status of the slave will only be valid if the slave knows what the new margined reference is, i.e. the margin change needs to be sent to both the master and the slave. This can be done easily by using the MFR_RAIL_ADDRESS to assign the same rail address to both the master and slave so that the margin change can be done with a single write. Be aware that PMBus reads from a common address need to be done separately to avoid bus contentions.
3. Using the Master's CLKOUT: The CLKOUT pin provides an 180° out-of-phase clock that can be connected to the slaves MODE/SYNC pin as a simple way to run the phases out-of-phase with each other. However, be aware that the master's CLKOUT pin only provides this out-of-phase clock when the master is using its internal oscillator programmed from the RT pin. If the master is externally clocked, the slave's anti-phase clock will need to be obtained from another source.

High Duty Cycle Applications

The internal power MOSFETs of the LTC7131-1 have a top-to-bottom $R_{DS(ON)}$ ratio of 3.5 to optimize power dissipation for low duty-cycle applications. For some applications, such as using a 5V supply (Figure 19) or using a separate low voltage supply connected to V_{IN} pin (see Using Separate SV_{IN}/V_{IN} Supplies section), the duty cycle may be high enough that the top MOSFET power dissipation becomes significant at higher loads. It is important in these types of applications to estimate power loss and die temperature rise to make sure the maximum die temperature is not exceeded. Once a prototype is built, this can be easily verified using the READ_TEMPERATURE command.

Another consideration for high duty cycles is the upper limit of how high the duty cycle can go. The bottom MOSFET has a minimum on-time of 150ns (worst case) to sense inductor current and refresh the BOOST capacitor. These means that the maximum achievable duty cycle is given by Equation 33.

$$\text{Max \% Duty Cycle} = (1 - f_{SW} \bullet 150 \bullet 10^{-9}) \bullet 100\% \quad (33)$$

The maximum duty cycle will limit the maximum allowable output voltage at the minimum supply voltage.

APPLICATIONS INFORMATION

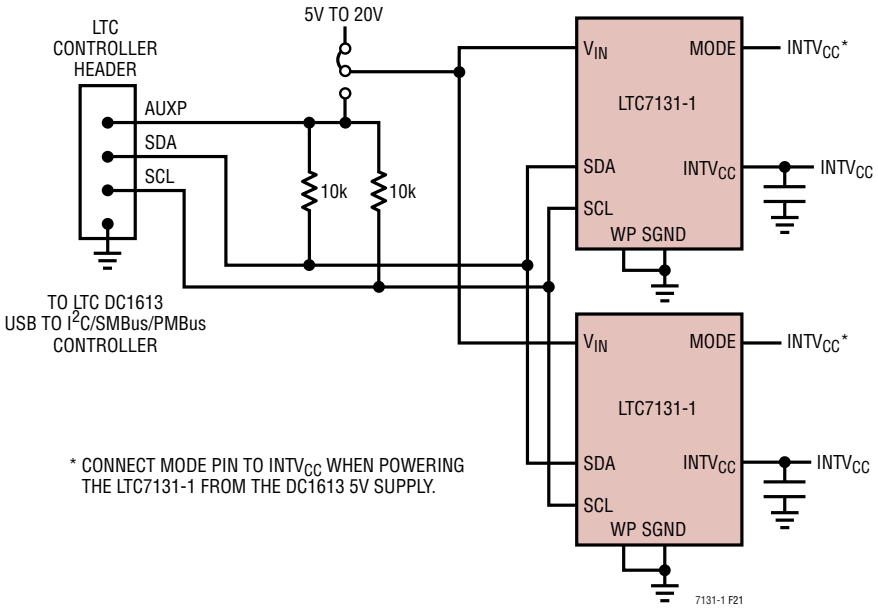


Figure 21. ADI Controller Connection

CONNECTING THE USB TO THE I²C/SMBus/PMBus CONTROLLER TO THE LTC7131-1 IN SYSTEM

The ADI USB to I²C/SMBus/PMBus controller can be interfaced to the LTC7131-1 on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system.

Figure 21 illustrates the application schematic for powering, programming and communication with one or more LTC7131s via the ADI I²C/SMBus/PMBus controller regardless of whether or not system power is present. If system power is not present, the LTC7131-1 can be powered directly from the DC1613's 5V supply. Since the current sourcing ability of this 5V supply is limited, the LTC7131-1 should be lightly loaded (<10mA) and operating in discontinuous mode (MODE/SYNC tied to $INTV_{CC}$).

In addition any device sharing the I²C bus connections with the LTC7131-1 should not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication in the absence of system power.

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER

LTpowerPlay (Figure 22) is a powerful Windows-based development environment that supports Analog Devices power system management ICs and other digital power IC's like the LTC7131-1. The software supports a variety of different tasks. LTpowerPlay can be used to evaluate Analog Devices ICs by connecting to a demo board or the user application. LTpowerPlay can also be used in an off-line mode (with no hardware present) in order to build multiple IC configuration files that can be saved and reloaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bring up rails. LTpowerPlay utilizes Analog Devices' USB-to-I²C/SMBus/PMBus controller to communication with one of the many potential targets including the DC1590B-A/DC1590B-B demo board, the DC1709A socketed programming board, or a customer target system. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation. A great deal of context sensitive help is available with LTpowerPlay along with several tutorial demos. Complete information is available here.

APPLICATIONS INFORMATION

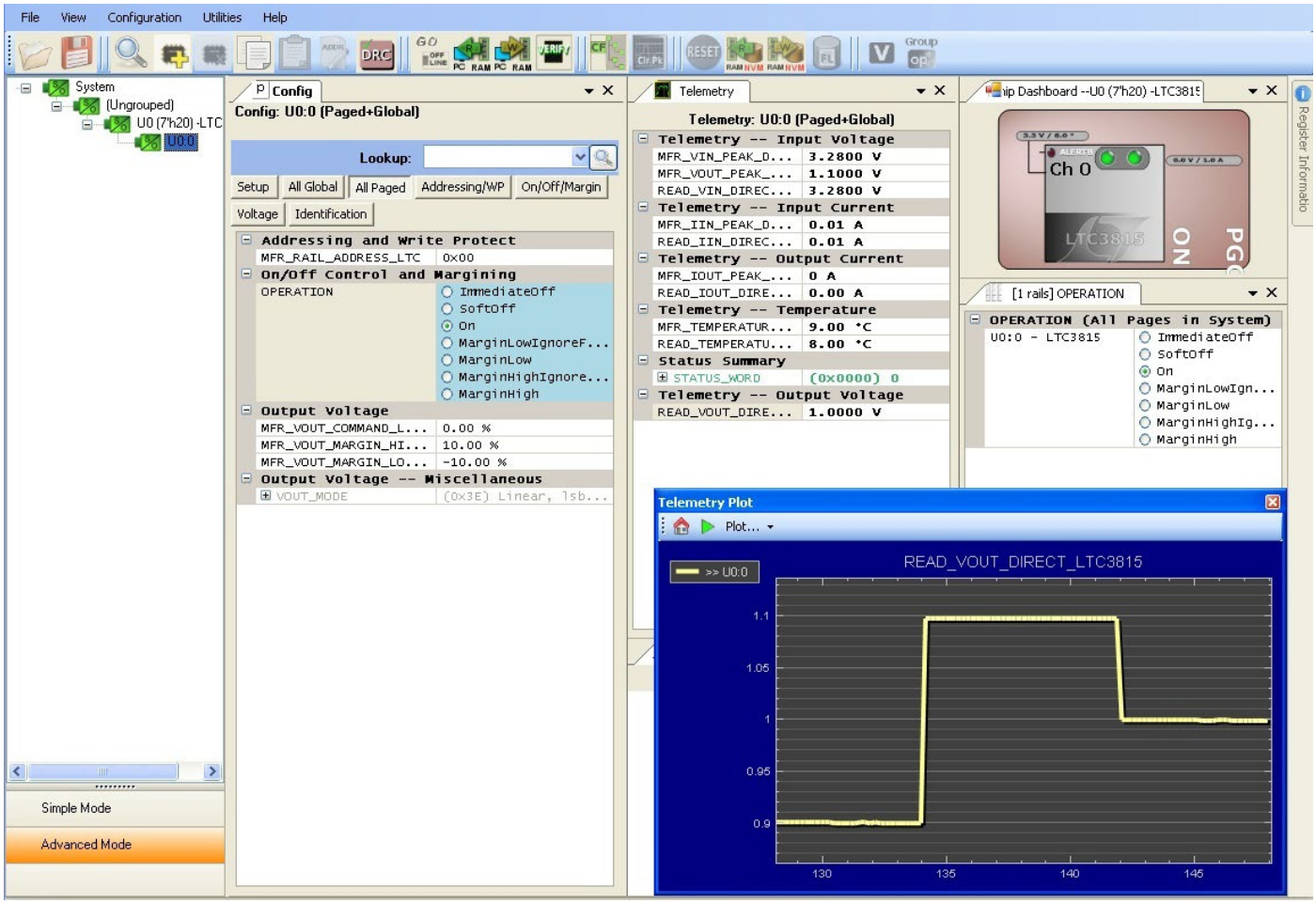


Figure 22. LTpowerPlay

PMBus COMMAND DETAILS

MFR_RESET

This command provides a means by which the user can perform a reset of the LTC7131-1. All latched faults ($\overline{\text{ALERT}}$ and status register) and register (telemetry, margin, etc) contents will be reset to a power-on condition by this command. V_{OUT} will remain in regulation but may change due to the reset of the margin registers. ASEL and PGFD config resistors are re-measured.

This write-only command accepts zero, one, or two data bytes but ignores them.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command allows all devices to share a common address, such as all devices attached to a single power supply rail. The desired 7-bit address value is written to the 7 bits of the data byte.

The MSB (bit B7) must be set low to enable communication using the MFR_RAIL_ADDRESS address. Setting this bit disables this address.

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value,

PMBus COMMAND DETAILS

the LTC7131-1 will detect bus contention and set a CML communications fault.

This command accepts one or two data bytes but the second is ignored.

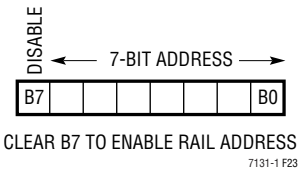


Figure 23. MFR_RAIL_ADDRESS Data Byte

OPERATION

The OPERATION command is used to turn the unit on/off and for margining the output voltage.

The ON bit has the same function as the RUN_STBY pin, i.e. clearing it turns off the output voltage with PMBus interface still active and telemetry data refreshed at a slower 1Hz rate to minimize supply current. Either RUN_STBY pin or ON bit can be cleared/deasserted to put the LTC7131-1 into this standby mode. The ON bit is automatically reset to ON after a master shutdown (RUN_MSTR = 0V), power cycle, or MFR_RESET command.

If the SOFT OFF bit is asserted when the LTC7131-1 is turned off (by RUN_STBY, RUN_MSTR or the ON bit), the output will be ramped down slowly at the rate set by the soft-start capacitor (Equation 34).

$$dV/dt = 5\mu A/C_{SS} \quad (34)$$

The MARGIN_LOW/HIGH bits command the V_{OUT} reference to the offset value stored in either the MFR_VOUT_MARGIN_HIGH or MFR_VOUT_MARGIN_LOW, resp. at the slew rate set by the C_{SLEW} capacitor. These bits are identical in function to margin high/low from the MARGIN pin. However, the MARGIN pin has precedence over the MARGIN_LOW/HIGH bits when there is a conflict. Cycling the RUN_STBY pin has no affect on the margin bits and thus when re-asserting RUN_STBY, V_{OUT} will return to the state it was in prior to the shutdown.

Margin high (ignore faults) and margin low (ignore faults) operations are not supported by the LTC7131-1.

This command has one data byte. It will accept one or two but ignore the second byte.

Table 9. Supported OPERATION Command Register Values

ACTION	VALUE
Turn off immediately	0x00
Turn on	0x80
Margin Low	0x98
Margin High	0xA8
Soft Off	0x40

VOUT_MODE

VOUT_MODE command specifies the formatting for reading output voltage. The data byte always reads 0x3E for VID data format and cannot be changed. Attempts to write to VOUT_MODE will set a CML fault.

This read-only command has one data byte.

MFR_VOUT_COMMAND

The MFR_VOUT_COMMAND consists of a value (%) used to offset the output reference voltage at the REF pin. The C_{SLEW} capacitor sets the slew rate limit of the output voltage if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted as a 9-bit 2's complement number with 0.1%/bit scaling.

The range of MFR_VOUT_COMMAND value is limited to ±25%.

Do not attempt to write values outside of this range or unpredictable behavior may result. Writes to this register are inhibited when the WP pin is high.

MFR_ VOUT_MARGIN_LOW

The MFR_VOUT_MARGIN_LOW command loads the LTC7131-1 with the value to which the output is changed, in percent, when the OPERATION command is set to margin low or the fast margining pin, MARGIN, is pulled below 0.4V. Slew rate limiting is same as MFR_VOUT_COMMAND.

This command has two data bytes and is formatted as a 9-bit 2's complement number with 0.1%/bit scaling.

PMBus COMMAND DETAILS

The range of MFR_VOUT_MARGIN_LOW value is limited to ±25%. There is no restriction on the value relative to VOUT_COMMAND and MFR_VOUT_MARGIN_HIGH, i.e. the value is not required to be lower.

Do not attempt to write values outside of this range or unpredictable behavior may result. Writes to this register are inhibited when the WP pin is high.

MFR_VOUT_MARGIN_HIGH

The MFR_VOUT_MARGIN_HIGH command loads the LTC7131-1 with the value to which the output is changed, in percent, when the OPERATION command is set to margin high or the fast margining pin, MARGIN, is pulled above 1.1V. Slew rate limiting is same as MFR_VOUT_COMMAND.

This command has two data bytes and is formatted as a 9-bit 2's complement number with 0.1%/bit scaling.

The range of MFR_VOUT_MARGIN_HIGH value is limited to ±25%. There is no restriction on the value relative to MFR_VOUT_COMMAND and MFR_VOUT_MARGIN_LOW, i.e. the value is not required to be higher.

Do not attempt to write values outside of this range or unpredictable behavior may result. Writes to this register are inhibited when the WP pin is high.

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTC7131-1 is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte.

MFR_SPECIAL_ID

The 16-bit word representing the part name and revision. The 0x40E prefix denotes the part is an LTC7131-1. The LSB is adjustable by the manufacturer.

This read-only command has 2 data bytes.

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values and restarts the peak monitor routine.

This write-only command requires no data bytes, but will accept (and ignore) up to two.

STATUS_WORD

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition.

See Table 11 for a list of the status bits that are supported and the conditions in which each bit is set. Certain bits when set in the STATUS_WORD also cause the $\overline{\text{ALERT}}$ pin to be asserted.

Writing a "1" to a particular bit in the status word will attempt to reset that fault in the status word and the $\overline{\text{ALERT}}$ pin. If the fault is still present the status word bit and $\overline{\text{ALERT}}$ will remain asserted. If the $\overline{\text{ALERT}}$ has previously been cleared by an ARA message, the $\overline{\text{ALERT}}$ will be re-asserted. If the fault is no longer present, the $\overline{\text{ALERT}}$ pin will be de-asserted and the fault bit in the status word will be cleared.

All bits in the status word are also cleared by toggling the RUN_MSTR pin or the ON bit in OPERATION. The bit will immediately be set again if the fault remains.

This command has two data bytes.

MFR_FAULT_RESPONSE

The MFR_FAULT_RESPONSE command enables or disables hiccup mode operation when an overvoltage or overcurrent fault is detected as described in Fault Response Programming section.

Both bits are initialized to disable (0x00) at power on, MFR_RESET, and master shutdown (RUN_MSTR).

This command accepts one or two data bytes but the second is ignored.

Table 10. MFR_FAULT_RESPONSE Data Byte

BIT(S)	DESCRIPTION	OPERATION
0	Overcurrent Fault Hiccup Mode Enable	0: Disable 1: Enable
1	Overvoltage Fault Hiccup Mode Enable	0: Disable 1: Enable
7:2	Reserved	

PMBus COMMAND DETAILS

Table 11. Status Word Bit Descriptions and Conditions

BIT	DESCRIPTION	CONDITION	SET ALERT?	CLEARABLE BY WRITING '1' TO BIT?
0 (LSB)	None of the Above	If b[15] set due to V_{OUT} undervoltage	Yes	No
1	Communication Failure	(See Note 1)	Yes	Yes
2	Temperature Fault	Temp > 150°C	Yes	Yes
3	V_{IN} Undervoltage Fault	Not Implemented		
4	Output Overcurrent Fault	Not Implemented		
5	Output Overvoltage Fault	V_{OUT} > PGOOD High Threshold	Yes	Yes
6	OFF	No Power to the Output (Note 2)	No	No
7	Busy	Not Implemented		
8	Unknown	Not Implemented		
9	Other	Not Implemented		
10	Fans	Not Implemented		
11	$\overline{PGOOD}$	Inverted state of PGOOD pin	No	No
12	Manufacturer Specific	Not Implemented		
13	Input Voltage/ Current/Power Fault	Not Implemented	Yes	Yes
14	Output Current/Power Fault	Not Implemented		
15 (MSB)	Output Voltage Fault	V_{OUT} outside PGOOD window (Note 3)	Yes	Yes

Note 1: Communication failure is one of following faults: host sends too few bits, host reads too few bits, host writes too few bytes, host reads too many bytes, improper R/W bit set, unsupported command code, attempt to write to a read-only command. See PMBus Specification v1.2, Part II, Sections 10.8 and 10.9 for more information.

Note 2: Power may be off due to any one of the following conditions: RUN_STBY low, OPERATION ON cleared, V_{IN} undervoltage or overtemperature warning. When the power is off due to RUN_MSTR low or due to a more serious fault conditions such as V_{IN} low or overtemperature fault, the PMBus interface is turned off instead of asserting the OFF bit.

Note 3: This bit is disabled when drivers are off for any reason, soft-start not complete, or the V_{OUT} has not reached the PGOOD window for the first time.

All of the following telemetry registers are initialized to 0x8000 when cycling power, cycling RUN_MSTR pin or sending a MFR_RESET command. The register will remain at this value until its first conversion is complete—typically within 50ms of the initialization event.

READ_VIN

The READ_VIN command returns the measured input voltage, in volts, at the V_{IN} pin.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 4mV/bit.

READ_VOUT

The READ_VOUT command returns the measured output voltage, in volts as specified by the VOUT_MODE command.

The output voltage is sensed at the V_{SENSE}^+ and V_{SENSE}^- pins.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 0.5mV/bit.

READ_IIN

The READ_IIN command returns the input current in Amperes. The input current is derived from READ_IOUT current and the measured duty cycle with an offset term added to account for quiescent current and driver current. For accurate values at light load currents the part must be in continuous conduction mode.

This register is reset to 0x8000 is standby mode when the drivers are off.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 10mA/bit.

PMBus COMMAND DETAILS

READ_IOUT

The READ_IOUT command returns the average output current in amperes. The LTC7131-1 senses and measures the currents through its bottom power switches to derive I_{OUT} current. For accurate values at light load currents the part must be in continuous conduction mode.

This register is reset to 0x8000 is standby mode when the drivers are off.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 10mA/bit.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the internal die temperature, in degrees Celsius, of the LTC7131-1.

This read-only command has two data bytes and is formatted as a 16-bit 2's complement value scaled 1°C/bit.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_VOUT_PEAK. When writing to MFR_VOUT_PEAK, zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 0.5mV/bit.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_VIN_PEAK. When writing to MFR_VIN_PEAK zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 4mV/bit.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_TEMPERATURE_1_PEAK. When writing to MFR_TEMPERATURE_1__PEAK zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 1°C/bit.

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_IOUT_PEAK. When writing to MFR_IOUT_PEAK, zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 10mA/bit.

MFR_IIN_PEAK

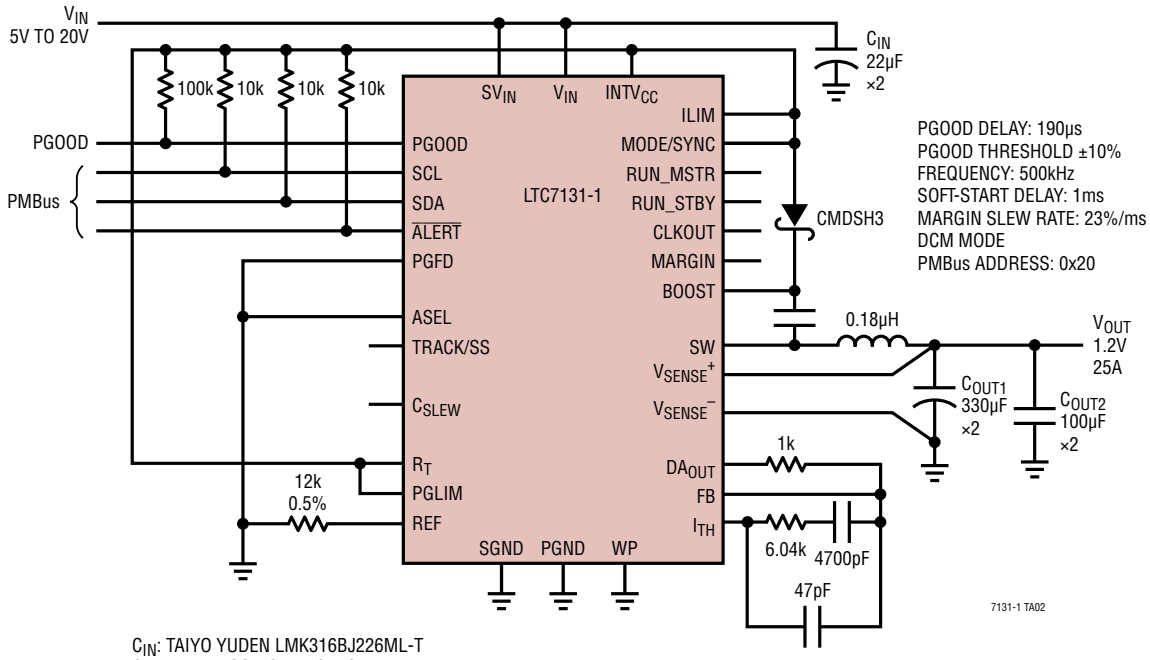
The MFR_IIN_PEAK command reports the highest current, in amperes, reported by the READ_IIN measurement.

To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command or write to the MFR_IIN_PEAK. When writing to MFR_IIN_PEAK, zero, one or two data bytes are accepted but the data is ignored.

This command has two data bytes and is formatted as a 16-bit 2's complement value scaled 10mA/bit.

TYPICAL APPLICATIONS

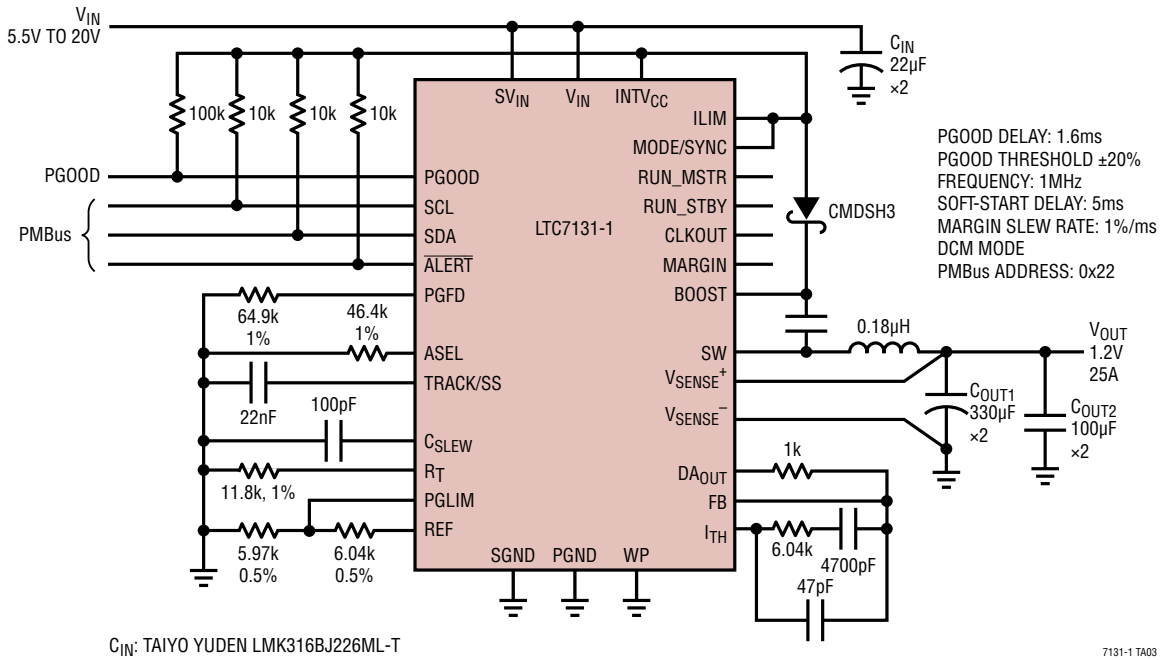
1.2V/25A 500kHz Buck Regulator with Minimum External Components



C_{IN}: TAIYO YUDEN LMK316BJ226ML-T
C_{OUT1}: PANASONIC EEF-SX0G331XE
C_{OUT2}: MURATA GRM32ER60J107ME20L
L: COILCRAFT XAL6030-331MEB

TYPICAL APPLICATIONS

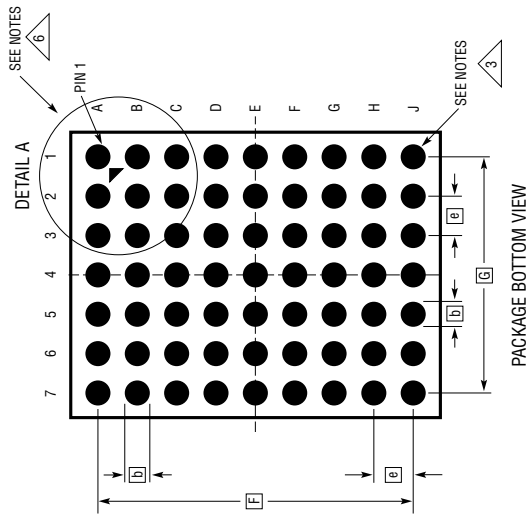
1.2V/25A 1MHz Buck Regulator



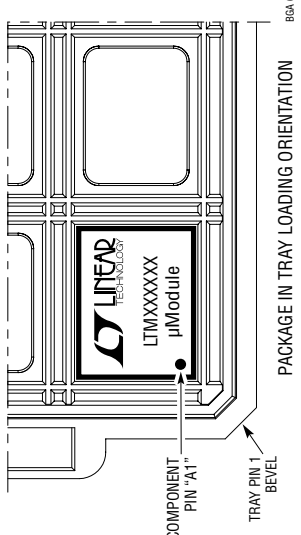
C_{IN}: TAIYO YUDEN LMK316BJ226ML-T
C_{OUT1}: PANASONIC EEF-SX0G331XE
C_{OUT2}: MURATA GRM32ER60J107ME20L
L: COILCRAFT XAL6030-181MEB

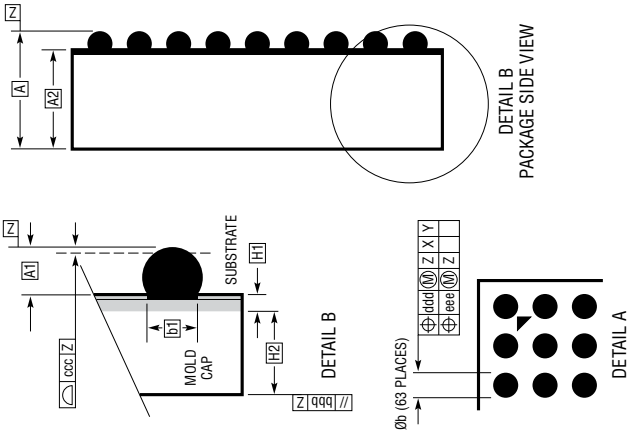
PACKAGE DESCRIPTION

BGA Package
63-Lead (7.5mm × 6.25mm × 2.22mm)
(Reference LTC DWG # 05-08-1988 Rev A)



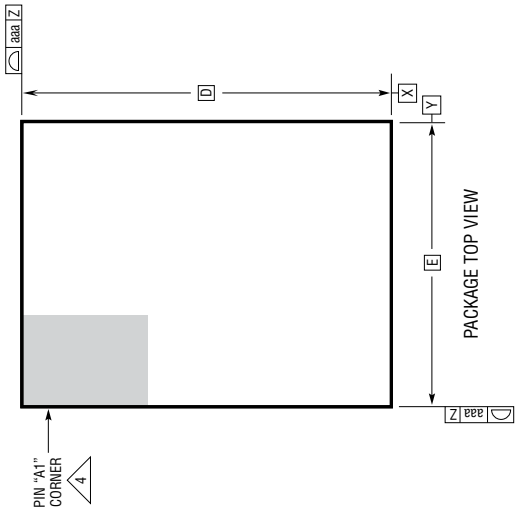
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

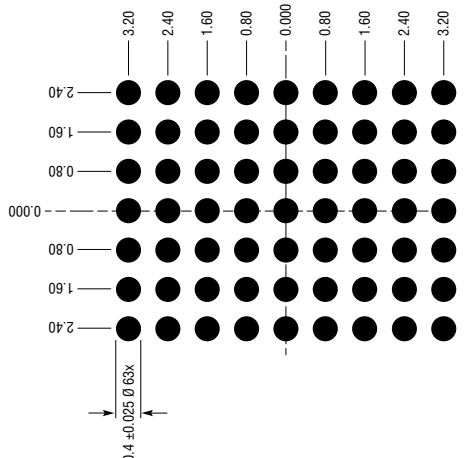




DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.07	2.22	2.37	
A1	0.35	0.40	0.45	BALL HT
A2	1.72	1.82	1.92	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		7.50		
E		6.25		
e		0.80		
F		6.40		
G		4.80		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	1.45	1.50	1.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.12	
ddd			0.15	
eee			0.08	

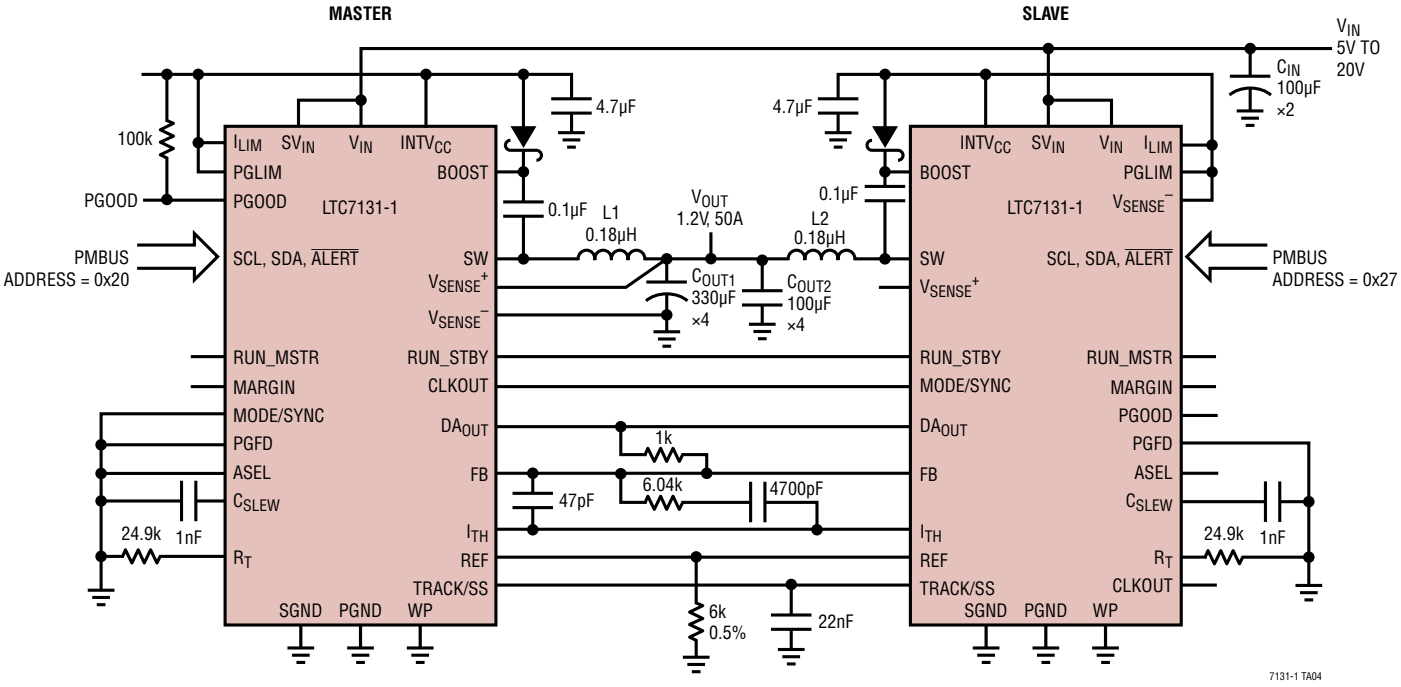
TOTAL NUMBER OF BALLS: 63





TYPICAL APPLICATION

1.2V/50A 2-Phase Buck Regulator



C_{IN}: TAIYO YUDEN LMK316BJ226ML-T
C_{OUT1}: PANASONIC EEF-SX0G331XE
C_{OUT2}: MURATA GRM32ER60J107ME20L
L1, L2: COILCRAFT XAL6030-331MEB

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7130	20V, 20A Monolithic Buck	$4.5V \le V_{IN} \le 20V$, $0.8V \le V_{OUT} \le 5.5V$, 6.25mm × 7.5mm × 2.2mm BGA
LTC3605/ LTC3605A	20V, 5A Synchronous Step-Down Regulator	$4V < V_{IN} < 20V$, $0.6V < V_{OUT} < 20V$, 96% Max Efficiency, 4mm × 4mm QFN-24 Package
LTC3633A LTC3633A-1	Dual Channel 3A, 20V Monolithic Synchronous Step-Down Regulator	$3.6V < V_{IN} < 20V$, $0.6V < V_{OUT} < V_{IN}$, 95% Max Efficiency, 4mm × 5mm QFN-28 and TSSOP-28 Package
LTC3622	17V, Dual 1A Synchronous Step-Down Regulator with Ultralow Quiescent Current	$2.7V < V_{IN} < 17V$, $0.6V < V_{OUT} < V_{IN}$, 95% Max Efficiency, 3mm × 4mm DFN-14 and MSOP-16 Package
LTC3613	24V, 15A Monolithic Step-Down Regulator with Differential Output Sensing	$4.5V < V_{IN} < 24V$, $0.6V < V_{OUT} < 5.5V$, 0.67% Output Voltage Accuracy, Valley Current Mode, Programmable from 200kHz to 1MHz, Current Sensing, 7mm × 9mm QFN-56 Package
LTC3624	17V, 2A Synchronous Step-Down Regulator with 3.5µA Quiescent Current	$2.7V < V_{IN} < 17V$, $0.6V < V_{OUT} < V_{IN}$, 95% Max Efficiency, 3.5µA I_Q, Zero-Current Shutdown, 3mm × 3mm DFN-8 Package
LTM®4639	Low V_{IN} 20A DC/DC µModule® Step-Down Regulator	Complete 20A Switch Mode Power Supply, $2.375V < V_{IN} < 7V$, $0.6V < V_{OUT} < 5.5V$, 1.5% Max Total DC Output Voltage Error, Differential Remote Sense Amp, 15mm × 15mm BGA Package
LTM4637	20A DC/DC µModule Step-Down Regulator	Complete 20A Switch Mode Power Supply, $4.5V < V_{IN} < 20V$, $0.6V < V_{OUT} < 5.5V$, 1.5% Max Total DC Output Voltage Error, Differential Remote Sense Amp, 15mm × 15mm BGA or LGA Package