40V Low I_Q, 3MHz Synchronous Step-Down Controller with Spread Spectrum

FEATURES

- **Low Operating I_Q: 12µA (14V V_{IN} to 3.3V V_{OUT})**
- **Wide Input Voltage Range: 4.5V to 40V**
- **Fixed 3.3V Regulated Output Voltage**
- **Spread Spectrum Operation**
- **R_{SENSE} or DCR Current Sensing**
- Programmable Fixed Frequency (100kHz to 3MHz)
- Phase-Lockable Frequency (100kHz to 3MHz)
- Selectable Continuous, Pulse-Skipping, or Low Ripple Burst Mode® Operation at Light Loads
- Low Shutdown I_Q: 1.2µA
- Thermally Enhanced 16-Lead 3mm × 3mm QFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive and Transportation
- Industrial
- Military/Avionics
- Telecommunications

DESCRIPTION

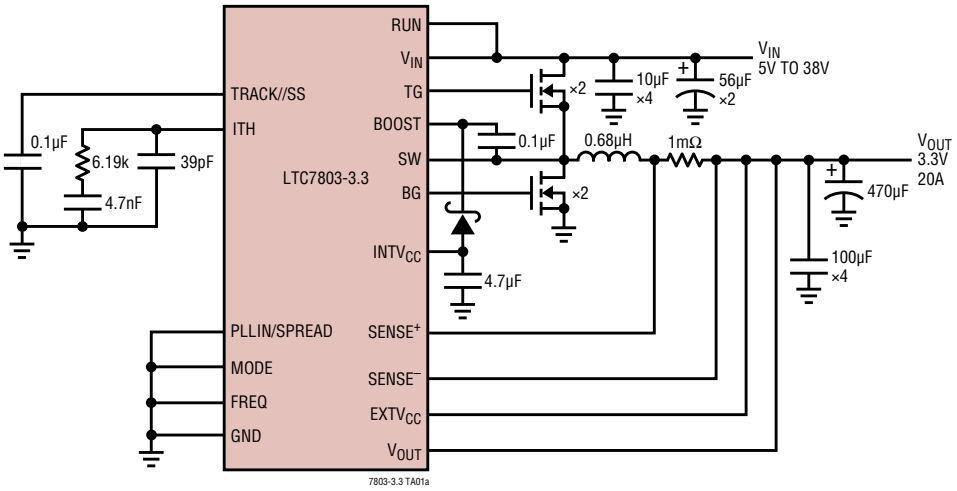
The LTC®7803-3.3 is a high performance synchronous step-down DC/DC switching regulator controller that drives an all N-channel power MOSFET stage. Synchronous rectification increases efficiency, reduces power losses and eases thermal requirements. A constant frequency current mode architecture allows a phase-lockable switching frequency of up to 3MHz. The LTC7803-3.3 operates from a wide 4.5V to 40V input supply range and regulates the output to a fixed 3.3V voltage using an internal feedback resistor divider.

The very low no-load quiescent current extends operating runtime in battery powered systems. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The MODE pin selects among Burst Mode operation, pulse-skipping mode, or continuous inductor current mode at light loads.

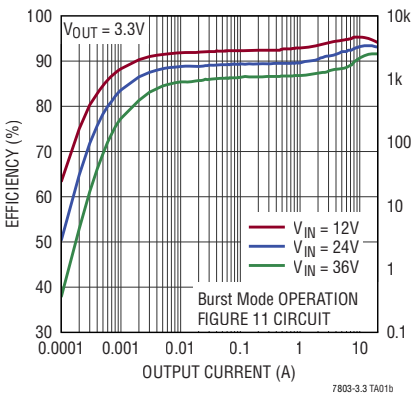
The LTC7803-3.3 additionally features spread spectrum operation which significantly reduces the peak radiated and conducted noise on both the input and output supplies, making it easier to comply with electromagnetic interference (EMI) standards.

TYPICAL APPLICATION

High Efficiency Wide Input Range 375kHz 3.3V/20A Step-Down Regulator



Efficiency vs Output Current

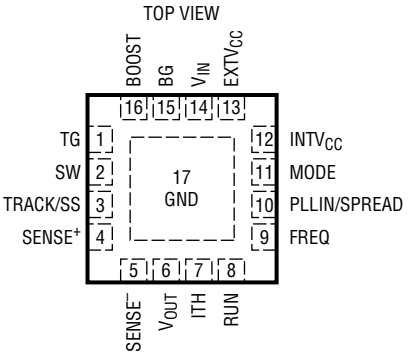


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 40V
BOOST ..... –0.3V to 46V
SW ..... –5V to 40V
RUN ..... –0.3V to 40V
SENSE+, SENSE– ..... –0.3V to 40V
$EXTV_{CC}$ Voltage ..... –0.3V to 30V
$INTV_{CC}$, (BOOST-SW) ..... –0.3V to 6V
TRACK/SS, FREQ ..... –0.3V to 6V
ITH ..... –0.3V to 2V
PLLIN/SPREAD, MODE, V_{OUT} ..... –0.3V to 6V
BG, TG ..... (Note 9)
Operating Junction Temperature Range (Note 2,8)
LTC7803R-3.3, LTC7803J-3.3 ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7803RUD-3.3#PBF	LTC7803RUD-3.3#TRPBF	LHPW	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LTC7803JUD-3.3#WPBF	LTC7803JUD-3.3#WTRPBF	LHPW	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, RUN = 12V, $EXTV_{CC}$ = 0V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{IN}	Input Supply Operating Range			4.5		40	V
I_{VIN}	V_{IN} Current in Regulation	Front Page Circuit, 14V to 3.3V No Load			12		µA
Controller Operation							
V_{OUT}	Regulated Output Voltage	(Note 4) V_{IN} = 4.5V to 40V, ITH Voltage = 0.6V to 1.2V	●	3.25	3.30	3.35	V
	Feedback Current	(Note 4)			1	1.3	µA
	Feedback Overvoltage Protection Threshold	Measured at V_{OUT} Relative to Regulated V_{OUT}		7	10	13	%
g_m	Transconductance Amplifier g_m	(Note 4) ITH = 1.2V, Sink/Source = 5µA			2		mmho
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{OUT} = 2.9V, V_{SENSE^-} = 3.3V	●	45	50	55	mV
I_{SENSE^+}	$SENSE^+$ Pin Current	V_{SENSE^+} = 3.3V				±1	µA
I_{SENSE^-}	$SENSE1^-$ Pin Current	V_{SENSE^-} = 3.3V			30		µA
	Soft-Start Charge Current	$V_{TRACK/SS}$ = 0V		10	12.5	15	µA
	RUN Pin ON Threshold	V_{RUN} Rising	●	1.15	1.2	1.25	V
	RUN Pin Hysteresis	V_{RUN} Falling			100		mV
DC Supply Current (Note 5)							
	V_{IN} Shutdown Current	RUN = 0V			1.2		µA
	V_{IN} Sleep Mode Current	V_{IN} Current, $EXTV_{CC}$ = 0V V_{IN} Current, $EXTV_{CC} \geq$ 4.8V $EXTV_{CC}$ Current, $EXTV_{CC} \geq$ 4.8V $SENSE^-$ Current			5 1 4 9		µA µA µA µA
	Pulse-Skipping or Forced Continuous Mode V_{IN} or $EXTV_{CC}$ Current (Note 3)				2		mA
Gate Drivers							
	TG or BG On-Resistance	Pull-up Pull-down			3 1.5		Ω Ω
	TG or BG Transition Time Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 15		 ns ns
	TG Off to BG On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			15		ns
	BG Off to TG On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			15		ns
$t_{ON(MIN)}$	TG Minimum On-Time	(Note 7)			40		ns
	Maximum Duty Factor for TG	FREQ = 0V			100		%
	Maximum Duty Factor for BG	Output Overvoltage			100		%
	BOOST Charge Pump Available Output Current	V_{BOOST} = 16V, V_{SW} = 12V, FREQ = 0V, Forced Continuous Mode		30	65		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, RUN = 12V, $EXTV_{CC}$ = 0V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Low Dropout (LDO) Linear Regulator							
	$INTV_{CC}$ Regulation Point			4.95	5.15	5.35	V
	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, $V_{IN} \geq$ 6V I_{CC} = 0mA to 50mA, $V_{EXTVCC} \geq$ 6V			1 1	2 2	% %
	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Rising		4.6	4.7	4.8	V
	$EXTV_{CC}$ Switchover Hysteresis	$EXTV_{CC}$ Falling			250		mV
UVLO	Undervoltage Lockout	$INTV_{CC}$ Rising	●	4.13	4.25	4.37	V
		$INTV_{CC}$ Falling	●	3.75	3.85	3.95	V
Spread Spectrum Oscillator and Phase-Locked Loop							
f_{OSC}	Low Fixed Frequency	V_{FREQ} = 0V, PLLIN/SPREAD = 0V		330	375	420	kHz
	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$, PLLIN/SPREAD = 0V	●	2.0	2.25	2.5	MHz
	Programmable Frequency	R_{FREQ} = 374kΩ, PLLIN/SPREAD = 0V R_{FREQ} =75kΩ, PLLIN/SPREAD = 0V R_{FREQ} = 12.5kΩ, PLLIN/SPREAD = 0V		 440	100 500 3	 560	kHz kHz MHz
f_{SYNC}	Synchronizable Frequency Range	PLLIN/SPREAD = External Clock	●	0.1		3	MHz
	PLLIN Input High Level PLLIN Input Low Level		● ●	2.2		 0.5	V V
	Spread Spectrum Frequency Range (Relative to f_{OSC})	PLLIN/SPREAD = $INTV_{CC}$ Minimum Frequency Maximum Frequency			 0 20		 % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7803-3.3R is specified over the –40°C to 150°C operating junction temperature range, and the LTC7803-3.3J is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (PD, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: When $EXTV_{CC} \geq$ 4.8V, V_{IN} supply current is transferred to these pins to reduce the total input supply quiescent current. $SENSE^-$ bias current is reflected to the input supply by the formula $I_{VIN} = I_{SENSE^-} \bullet V_{OUT}/(V_{IN} \bullet \eta)$, where η is the efficiency. $EXTV_{CC}$ bias current is similarly reflected to the input supply when biased by an output greater than the $EXTV_{CC}$ LDO Switchover Voltage (4.7V typical).

Note 4: The LTC7803-3.3 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{OUT}. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

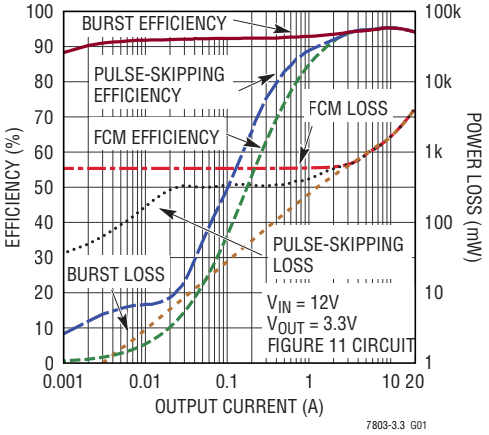
Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of I_{MAX} (See Minimum On-Time Considerations in the Applications Information section).

Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

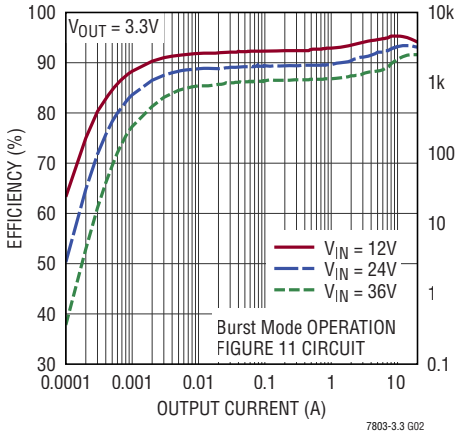
Note 9: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

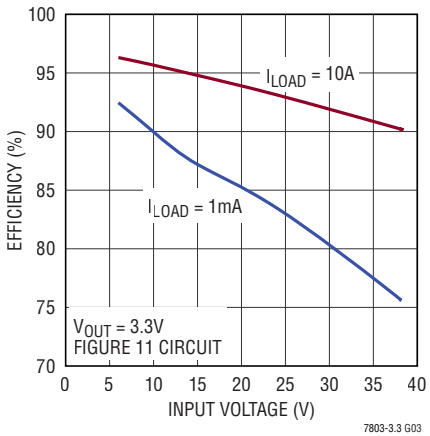
Efficiency and Power Loss vs Output Current



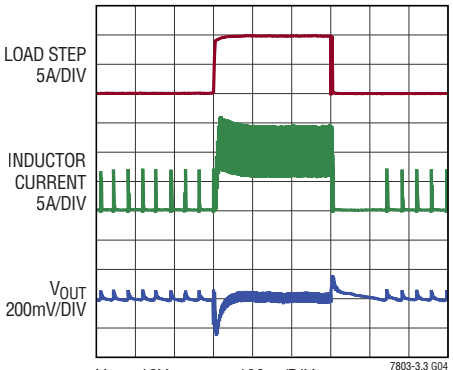
Efficiency vs Output Current



Efficiency vs Input Voltage

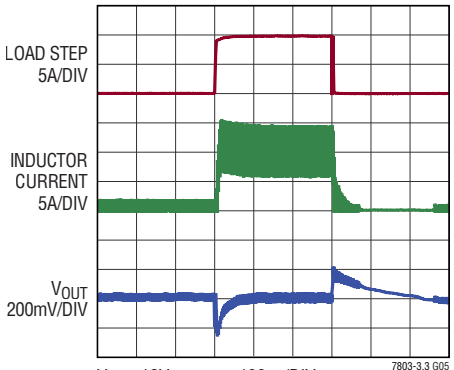


Load Step Burst Mode Operation



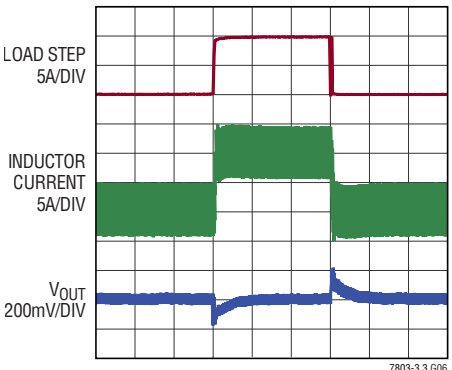
VIN = 12V 100µs/DIV
VOUT = 3.3V
200mA TO 10A LOAD STEP
FIGURE 11 CIRCUIT

Load Step Pulse-Skipping Mode



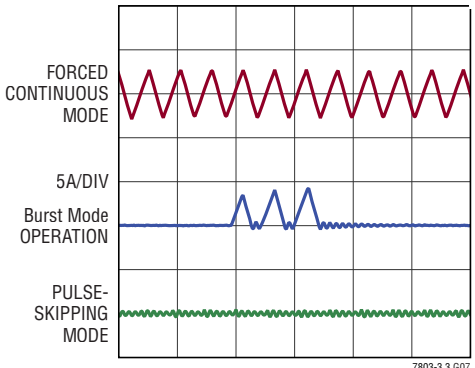
VIN = 12V 100µs/DIV
VOUT = 3.3V
200mA TO 10A LOAD STEP
FIGURE 11 CIRCUIT

Load Step Forced Continuous Mode



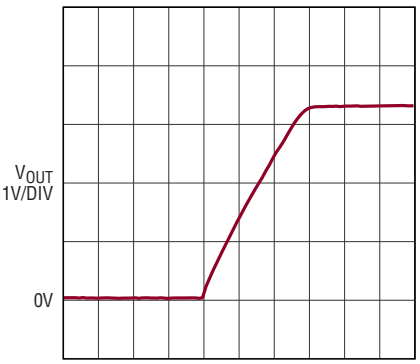
VIN = 12V 100µs/DIV
VOUT = 3.3V
200mA TO 10A LOAD STEP
FIGURE 11 CIRCUIT

Inductor Current at Light Load



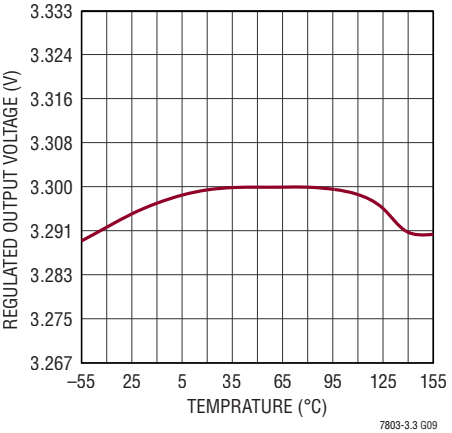
VIN = 6V 5µs/DIV
VOUT = 3.3V
ILOAD = 200µA
FIGURE 11 CIRCUIT

Soft Start-Up



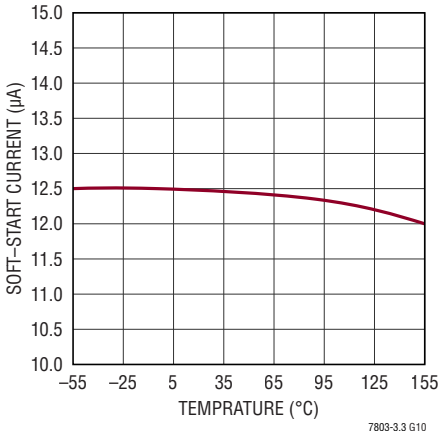
VIN = 12V 2ms/DIV
VOUT=3.3V
FIGURE 11 CIRCUIT

Regulated Output Voltage vs Temperature

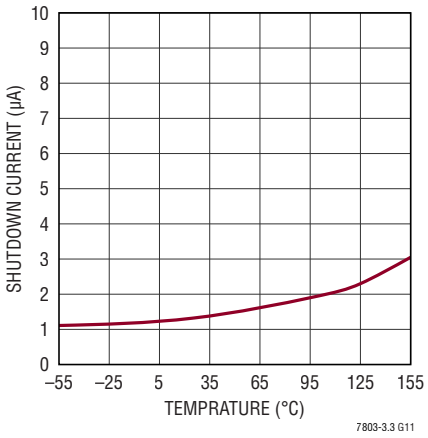


TYPICAL PERFORMANCE CHARACTERISTICS

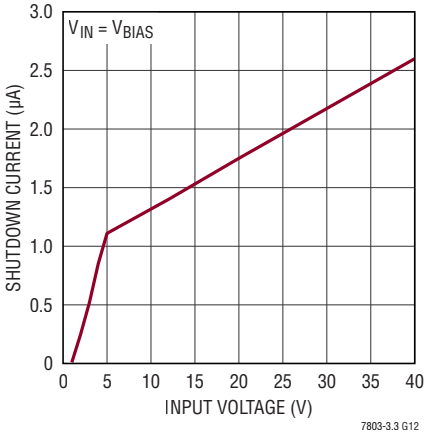
Soft-Start Pull-Up Current vs Temperature



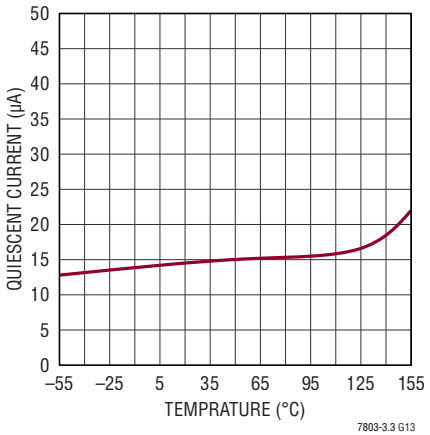
Shutdown Current vs Temperature



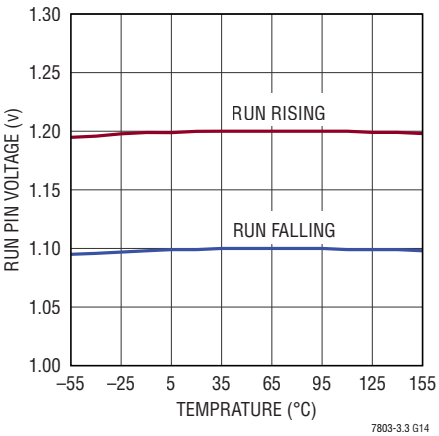
Shutdown Current vs Input Voltage



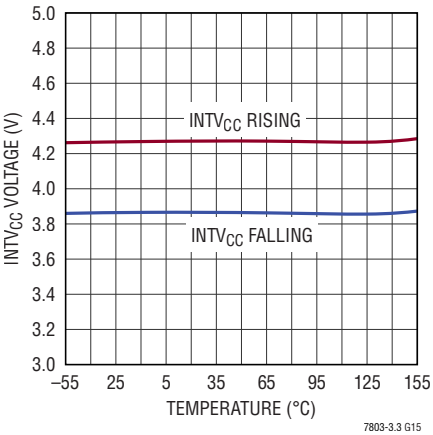
Quiescent Current vs Temperature



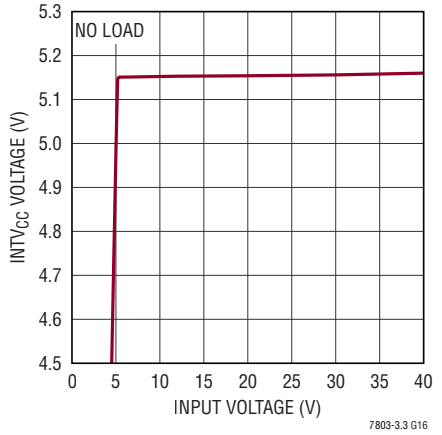
RUN Pin Thresholds vs Temperature



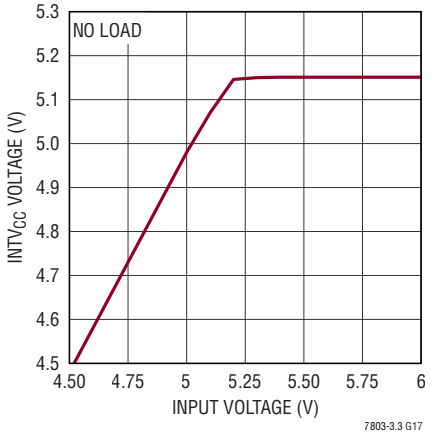
Undervoltage Lockout Threshold vs Temperature



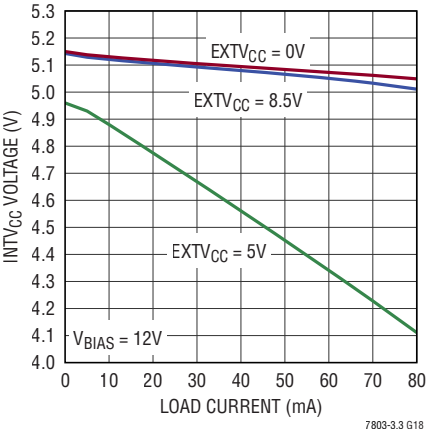
$INTV_{CC}$ Line Regulation



$INTV_{CC}$ Line Regulation

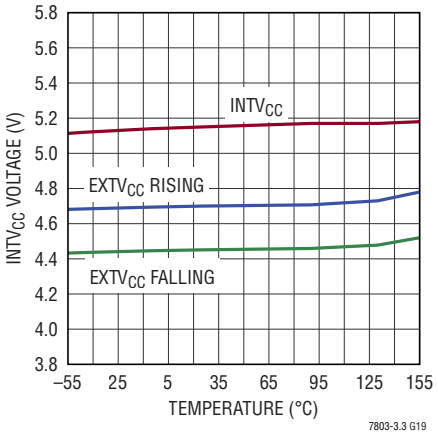


$INTV_{CC}$ and $EXTV_{CC}$ vs Load Current

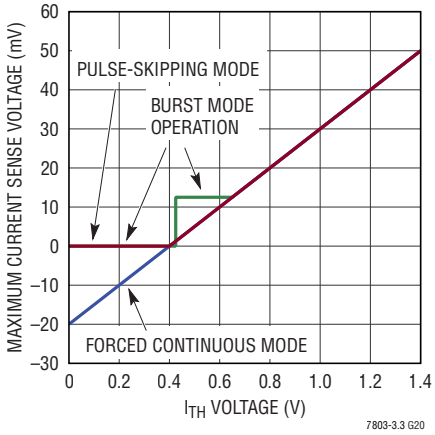


TYPICAL PERFORMANCE CHARACTERISTICS

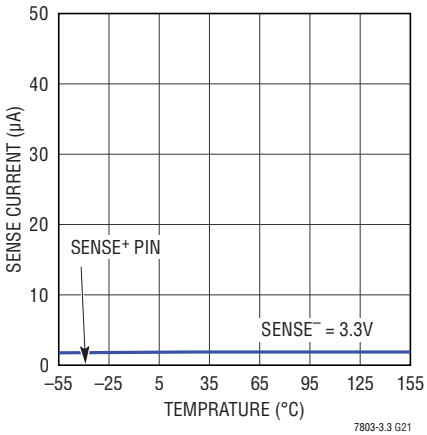
$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltage vs Temperature



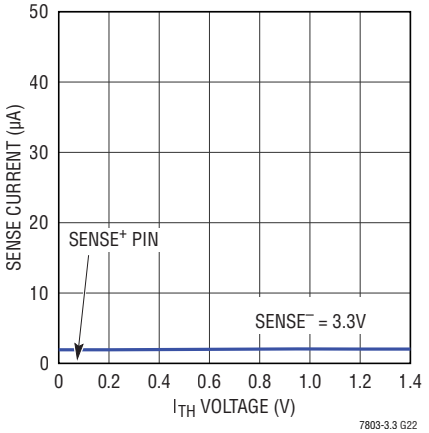
Maximum Current Sense Threshold vs I_{TH} Voltage



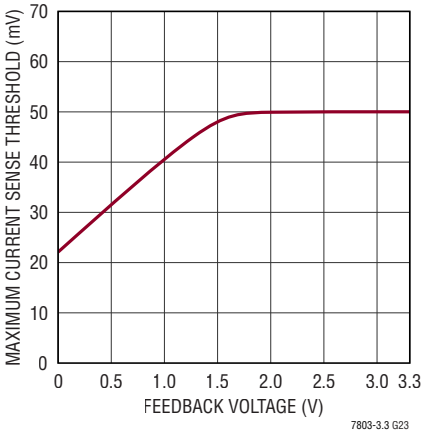
SENSE Pin Input Current vs Temperature



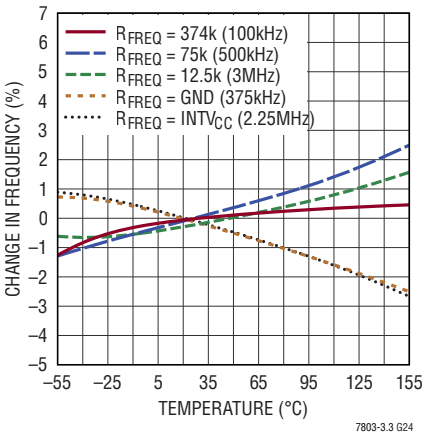
SENSE Pin Input Current vs I_{TH} Voltage



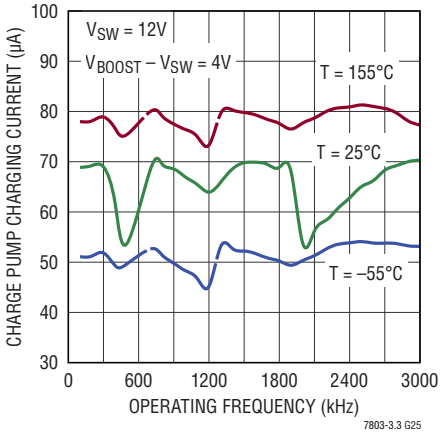
Foldback Current Limit



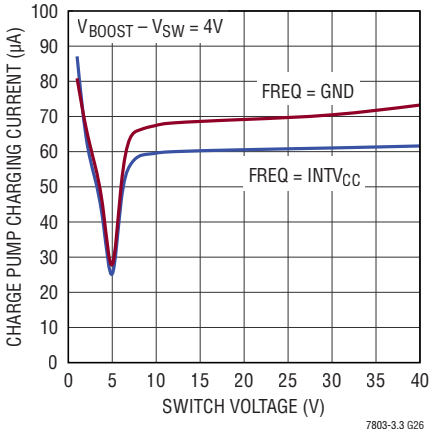
Oscillator Frequency vs Temperature



Charge Pump Charging Current vs Operating Frequency



Charge Pump Charging Current vs Switch Voltage



PIN FUNCTIONS

TG(Pin 1): High Current Gate Drive for the Top N-Channel MOSFET. This is the output of floating driver with a voltage swing of $INTV_{CC}$ superimposed on the switch node voltage SW.

SW(Pin 2): Switch Node Connection to the Inductor.

TRACK/SS (Pin 3): External Tracking and Soft-Start Input. The LTC7803-3.3 regulates the negative input of the error amplifier (EA^-) voltage to the lesser of 0.8V or the voltage on the TRACK/SS pin. An internal 12.5µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. The ramp time is equal to 0.65ms for every 10nF of capacitance. Alternatively, a resistor divider on another voltage supply connected to the TRACK/SS pin allows the LTC7803-3.3 output to track the other supply during start-up.

$SENSE^+$ (Pin 4): The Positive (+) Input to the Differential Current Comparators. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

$SENSE^-$ (Pin 5): The Negative (–) Input to the Differential Current Comparators. When $SENSE^-$ is 3.2V or greater, it supplies the majority of the sleep mode quiescent current instead of V_{IN}, further reducing the input-referred quiescent current.

V_{OUT} (Pin 6): Error Amplifier Feedback Input. Connect V_{OUT} directly to the output voltage.

ITH (Pin 7): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage. Place compensation components between the ITH pin and GND.

RUN (Pin 8): Run Control Input. Forcing this pin below 1.2V disables switching of the corresponding controller. Forcing this pin below 0.7V shuts down the LTC7803-3.3, reducing quiescent current to approximately 1.2µA. This pin can be tied to V_{IN} for always-on operation.

FREQ (Pin 9): Frequency Control pin for the internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 375kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 2.25MHz. Frequencies between 100kHz and 3MHz can be programmed using a resistor between FREQ and GND. Minimize the capacitance on this pin.

PLLIN/SPREAD (Pin 10): External Synchronization Input and Spread Spectrum Selection. When an external clock is applied to this pin, the phase-locked loop will force the rising TG signal to be synchronized with the rising edge of the external clock. When an external clock is present, the regulators operate in pulse-skipping mode if it is selected by the MODE pin, or in forced continuous mode otherwise. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator or to ground to disable spread spectrum.

MODE (Pin 11): Mode Select Input. This input determines how the LTC7803-3.3 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floating. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to $INTV_{CC}$ through a 100k resistor selects pulse-skipping operation.

$INTV_{CC}$ (Pin 12): Output of the Internal 5.15V Low Dropout Regulator (LDO). The driver and control circuits are powered by this supply. Must be decoupled to GND with a minimum of 4.7µF ceramic or tantalum capacitor.

$EXTV_{CC}$ (Pin 13): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 4.7V. See $INTV_{CC}$ Regulators in the Applications Information section. Do not exceed 30V on this pin. Tie this pin to GND if the $EXTV_{CC}$ LDO is not used.

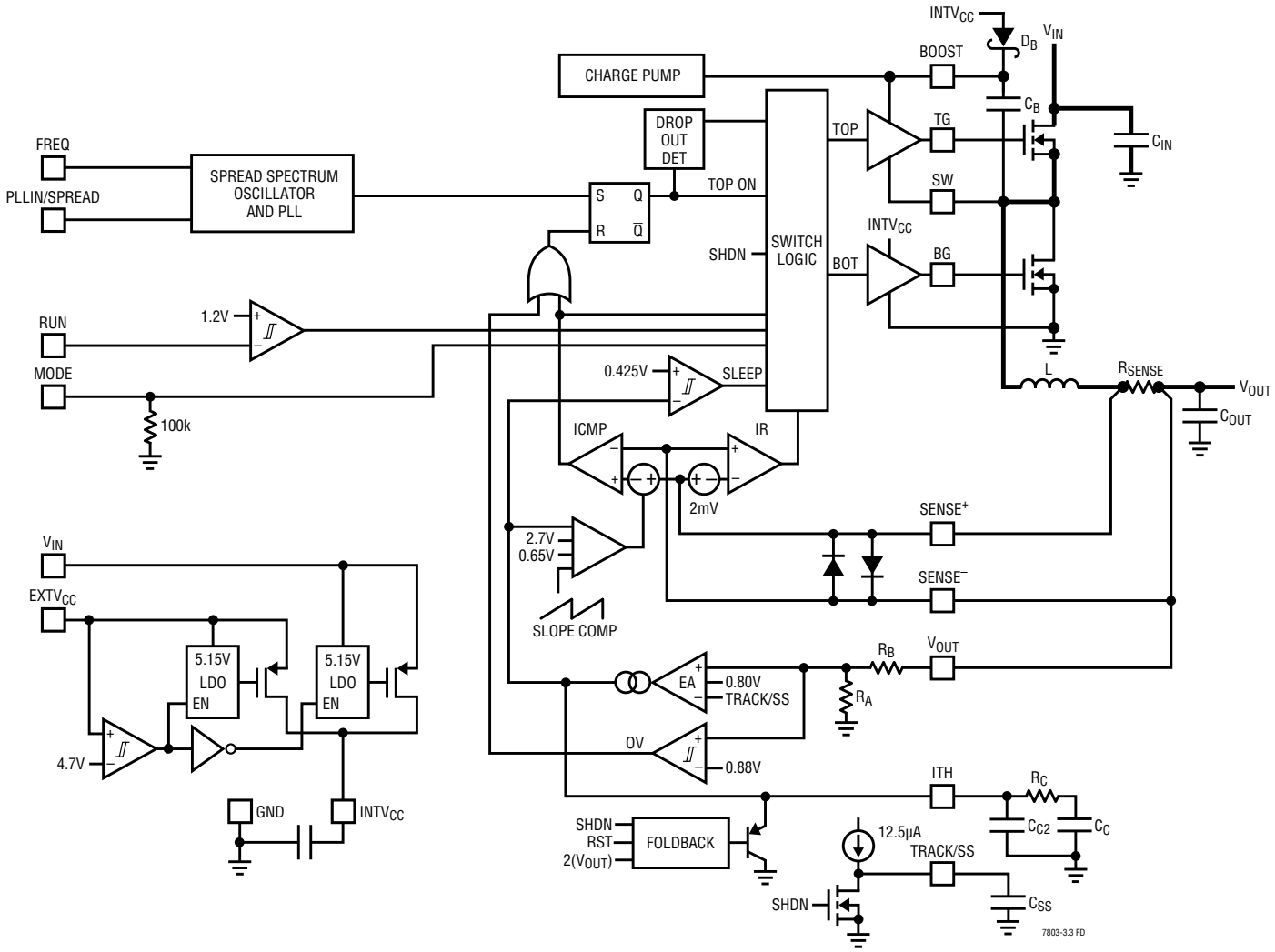
V_{IN} (Pin 14): Main Bias Input Supply Pin. A bypass capacitor should be tied between this pin and GND.

BG (Pin 15): High Current Gate Drive for Bottom (Synchronous) N-Channel MOSFET. Voltage swing at this pin is from GND to $INTV_{CC}$.

BOOST(Pin 16): Bootstrapped Supply to the Top Side Floating Driver. Connect a capacitor between the BOOST and SW pin. Also connect a low leakage Schottky diode between the BOOST and $INTV_{CC}$ pins.

GND (Exposed Pad Pin 17): Ground. Connects to the source of the bottom (main) N-channel MOSFET and the (–) terminal(s) of C_{IN} and C_{OUT}. All small-signal components and compensation components should also connect to this ground. The exposed pad must be soldered to the PCB for rated thermal performance.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC7803-3.3 uses a constant frequency, peak current mode step-down architecture. During normal operation, the external top MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal (which is generated with an internal resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in V_{OUT} relative to the regulated voltage, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current goes to far negative (or starts to reverse in Burst or pulse skipping mode as indicated by the current comparator IR) or the beginning of the next clock cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is tied to a voltage less than 4.7V, the V_{IN} LDO (low dropout linear regulator) supplies 5.15V from V_{IN} to $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.7V, the V_{IN} LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies 5.15V from $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source.

Boost Supply and Dropout (BOOST and SW pins)

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an external low leakage Schottky diode or PN Junction diode, D_B, diode when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The LTC7803-3.3 has an internal charge pump that allows the top MOSFET to be turned on continuously at 100% duty cycle.

Shutdown and Start-Up (RUN, TRACK/SS Pins)

The LTC7803-3.3 can be shutdown using the RUN pin. Pulling this pin below 1.1V shuts down the main control loop. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC7803-3.3 draws only 1µA of quiescent current.

The RUN pin needs to be externally pulled up or driven directly by logic. It can also be implemented as an undervoltage lockout (UVLO) by connecting it to the output of an external resistor divider network off V_{IN} (see Applications Information section).

The start-up of the controller's output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference, the LTC7803-3.3 regulates the negative input of the EA voltage to the TRACK/SS pin voltage instead of the 0.8V reference. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to SGND. An internal 12.5µA pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively the TRACK/SS pin can be used to cause the start-up of V_{OUT} to track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see Applications Information section).

Light Load Current Operation: Burst Mode Operation, Pulse-Skipping or Forced Continuous Mode (MODE Pin)

The LTC7803-3.3 can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at low load currents.

OPERATION

To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V. An internal 100k resistor to GND invokes Burst Mode operation when the MODE pin is floating and pulse-skipping mode when the MODE pin is tied to $INTV_{CC}$ through an external 100k resistor.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.45V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC7803-3.3 draws to only 14µA. When V_{OUT} is 3.2V or higher, the majority of this quiescent current is supplied by the $SENSE^-$ pin, which further reduces the input-referred quiescent current by the ratio of V_{IN}/V_{OUT} multiplied by the efficiency.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, IR, turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation or clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7803-3.3 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Unlike forced continuous mode and pulse-skipping mode, Burst Mode cannot be synchronized to an external clock. Therefore, if Burst Mode is selected and PLLIN/SPREAD pin is clocked to use the phase-locked loop, the LTC7803-3.3 switches from Burst Mode to forced continuous mode.

Frequency Selection, Spread Spectrum and Phase-Locked Loop (FREQ and PLLIN/SPREAD Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

OPERATION

The free running switching frequency of the LTC7803-3.3 is selected using the FREQ pin. If the PLLIN/SPREAD pin is not being driven by an external clock source, the FREQ pin can be tied to GND, tied to $INTV_{CC}$ or programmed through an external resistor. Tying FREQ to GND selects 375kHz while tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 100kHz and 3MHz, as shown in Figure 8.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7803-3.3 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency with typical boundaries of 0% to +20% of the frequency set by the FREQ pin.

A phase-locked loop (PLL) is available on the LTC7803-3.3 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/SPREAD pin. The LTC7803-3.3's phase detector (PFD) and low pass filter adjust the voltage) of the VCO input to align the turn-on of the controller's external top MOSFET to the rising edge of the synchronizing signal.

The VCO input voltage is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock to the rising edge of TG. For more rapid lock-in to the external clock, use the FREQ pin to set the internal oscillator to approximately the frequency of the external clock. The LTC7803-3.3's PLL is guaranteed to lock to an external clock source whose frequency is between 100kHz and 3MHz.

The PLLIN/SPREAD pin is TTL compatible with thresholds of 1.6V (rising) and 1.1V (falling) and is guaranteed to operate with a clock signal swing of 0.5V to 2.5V.

Output Overvoltage Protection

An overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{OUT} pin rises by more than 10% above its regulation point of 3.3V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Foldback Current

When the output voltage falls to less than 50% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the negative input of the EA voltage is keeping up with the TRACK/SS voltage).

BOOST Supply Refresh and Internal Charge Pump

The top MOSFET driver is biased from the floating bootstrap capacitor, CB, which normally recharges during each cycle through an external diode when the bottom MOSFET turns on. There is an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can normally supply a charging current of 65µA.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC7803-3.3 application circuit. LTC7803-3.3 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode voltage range on these pins is 0V to 40V (abs max), enabling the LTC7803-3.3 to regulate output voltages up to a maximum of 40V.

The SENSE+ pin is high impedance, drawing less than ≈ 1µA. This high impedance allows the current comparators to be used in inductor DCR sensing.

The impedance of the SENSE– pin changes depending on the common mode voltage. When SENSE– is less than 2.9V, it is relatively high impedance, drawing about 2µA. When SENSE– is greater than 3.2V but is less than $INTV_{CC}$ – 0.5V, the pin draws about 30µA to bias internal circuitry from V_{OUT}, thereby reducing the effective input supply current.

Filter components mutual to the sense lines should be placed close to the LTC7803-3.3, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If inductor DCR sensing is used (Figure 2b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

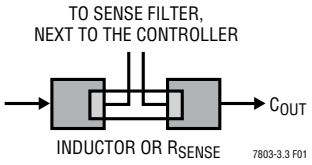
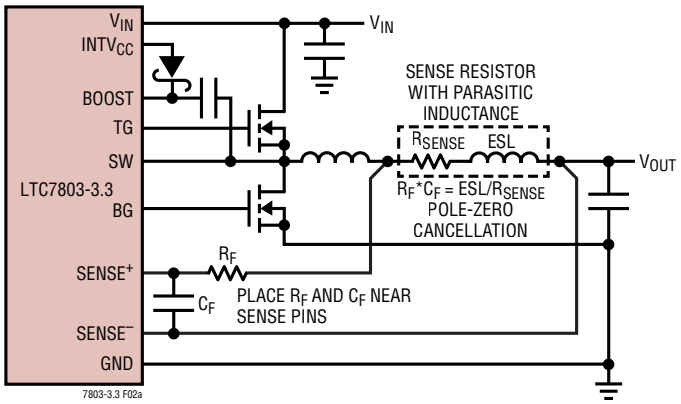


Figure 1. Sense Lines Placement with Inductor or Sense Resistor

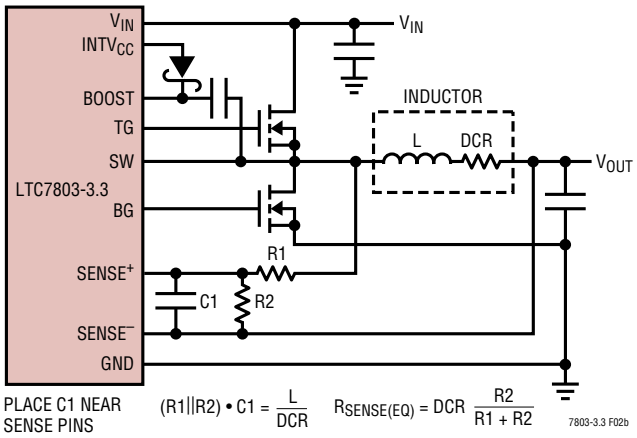
The maximum current limit threshold voltage of the current comparator is programmed to be 50mV.

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Current Sensing Methods

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The current comparator has a maximum threshold $V_{SENSE(MAX)}$ of 50mV. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table and account for tolerances in switching frequency, inductance, and RSENSE resistance, as well as applicable voltage ranges.

To avoid potential jitter or instability due to PCB noise coupling into the current sense signal, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ should also be checked to ensure a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a target V_{SENSE} AC ripple range of 10mV to 20mV at 50% duty cycle is recommended for both R_{SENSE} and DCR sensing applications.

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal, particularly for lower inductor value (< 3µH) or higher current (> 5A) applications. This error may be compensated for with an RC filter into the sense pins as shown in Figure 2a. Set the RC filter time constant $R_F \bullet C_F = ESL/R_{SENSE}$ for optimal cancellation of the ESL. Surface mount sense resistors in low ESL wide footprint geometries are recommended to minimize this error. If not specified on the manufacturer's data sheet, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint and 0.2nH for a 1225 footprint.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7803-3.3 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC resistance of the copper wire, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value (R_D), use the divider ratio:

$$R_D = \frac{V_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1 || R2 to around 2k, reducing

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error that might have been caused by the SENSE+ pin's ±1µA current.

The target equivalent resistance R1 || R2 is calculated from the nominal inductance, C1 value, and DCR:

The equivalent resistance R1 || R2 is scaled to the temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\ R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R_1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The maximum average inductor current $I_{L(MAX)}$ is equal to the maximum output current. The peak current is equal to the average inductor current plus half of the inductor ripple current, ΔI_L, which decreases with higher inductance or higher frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

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Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for the LTC7803-3.3 controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.15V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

Selection criteria for the power MOSFETs include the on resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR}+R_G)(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC}-V_{THMIN}}+\frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN}-V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$, R_G is the internal gate resistance of the MOSFET and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages and high switching frequencies. For $V_{IN} < 20V$ and frequencies less than 500KHz the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ and frequencies above 500KHz the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1+\delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

A Schottky diode can be inserted in parallel with the bottom MOSFET to conduct during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is usually based off the worst-case RMS input current. The highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 1 to determine the maximum RMS capacitor current requirement.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the

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maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7803-3.3, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC7803-3.3, is also suggested. A small (≤10Ω) resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting Output Voltage

Directly connect the LTC7803-3.3's V_{OUT} pin to the output to regulate the output voltage to 3.3V.

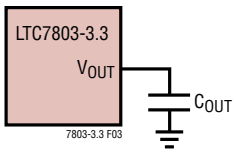

Figure 3. Setting Output Voltage

RUN Pin

The LTC7803-3.3 is enabled using the RUN pin. It has a rising threshold of 1.2V with 50mV of hysteresis. Pulling the RUN pin below 1.1V shuts down the main control loop. Pulling it below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC7803-3.3 draws only 1.2µA of quiescent current.

The RUN pin is high impedance and must be externally pulled up/down or driven directly by logic. The RUN pin can tolerate up to 40V (abs max), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down. Do not float the RUN pin.

The RUN pin can be implemented as a UVLO by connecting it to the output of an external resistor divider network off V_{IN}, as shown in Figure 4.

The rising and falling UVLO thresholds are calculated using the RUN pin thresholds:

$$V_{UVLO(RISING)} = 1.2V\left(1+\frac{R_B}{R_A}\right)$$

$$V_{UVLO(FALLING)} = 1.1V\left(1+\frac{R_B}{R_A}\right)$$

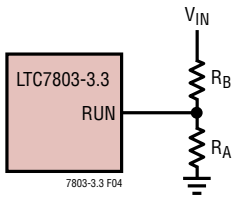

Figure 4. Using the RUN Pin as a UVLO

The resistor values should be carefully chosen such that the absolute maximum ratings of the RUN pin do not get violated over the entire V_{IN} voltage range.

For applications that do not require a precise UVLO the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited to the internal $INTV_{CC}$ UVLO threshold as shown in the Electrical Characteristics table.

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Tracking and Soft-Start (TRACK/SS Pin)

The start-up of V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LTC7803-3.3 regulates the V_{OUT} pin voltage to the voltage on the TRACK/SS pin instead of 0.8V. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 5. An internal 12.5µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC7803-3.3 will regulate the V_{OUT} according to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{12.5\mu A}$$

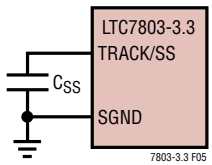


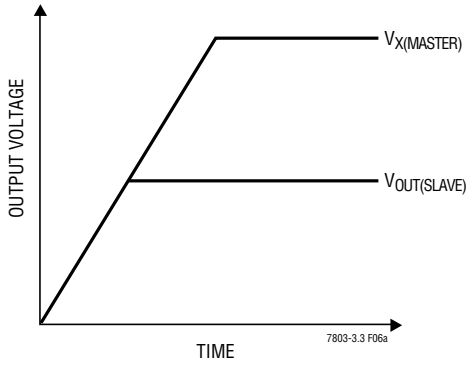
Figure 5. Using the TRACK/SS Pin to Program Soft-Start

Alternatively, the TRACK/SS pin can be used to track another supply during start-up, as shown qualitatively in Figures 6a and 6b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply (V_{OUT}), as shown in Figure 7. During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

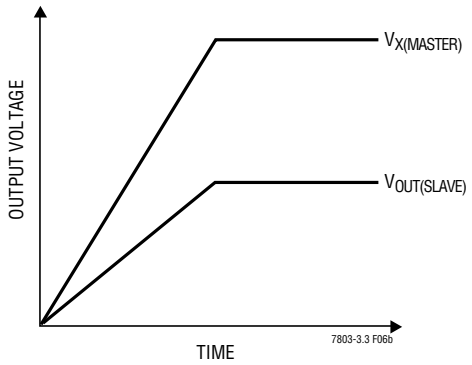
$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

For coincident tracking ($V_{OUT} = V_X$ during start-up):

$R_A = R_{TRACKA}$
$R_B = R_{TRACKB}$



(6a) Coincident Tracking



(6b) Ratiometric Tracking

Figure 6. Two Different Modes of Output Voltage Tracking

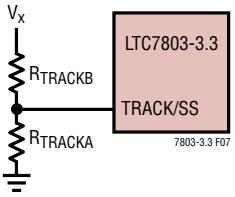


Figure 7. Using the TRACK/SS Pin for Tracking

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$INTV_{CC}$ Regulators

The LTC7803-3.3 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the $INTV_{CC}$ pin from either the V_{IN} supply pin or the $EXTV_{CC}$ pin depending on the connection of the $EXTV_{CC}$ pin. $INTV_{CC}$ powers the gate drivers and much of the LTC7803-3.3's internal circuitry. The V_{IN} LDO and the $EXTV_{CC}$ LDO regulate $INTV_{CC}$ to 5.15V. Each of these can supply a peak current of at least 100mA and must be bypassed to ground with a minimum of 2.2µF ceramic capacitor, placed as close as possible to the pin. No matter what type of bulk capacitor is used, an additional 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and GND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7803-3.3 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the V_{IN} LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than 4.7V, the V_{IN} LDO is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet INTV_{CC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC7803-3.3 $INTV_{CC}$ current is limited to less than 20mA from a 40V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature:

$T_J = 70°C + (20mA)(40V)(68°C/W \text{ for QFN}) = 125°C$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in forced continuous mode (MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. The $EXTV_{CC}$ LDO attempts to regulate the $INTV_{CC}$ voltage to 5.15V, so while $EXTV_{CC}$ is less than 5.15V, the LDO is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 5.15V, up to an absolute maximum of 30V, $INTV_{CC}$ is regulated to 5.15V.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from one of the LTC7803-3.3's switching regulator outputs ($4.7V \le V_{OUT} \le 30V$) during normal operation and from the V_{IN} LDO when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. In this case, do not apply more than 6V to the $EXTV_{CC}$ pin.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

This is accomplished by tying the $EXTV_{CC}$ pin directly to an output voltage that is greater than the $INTV_{CC}$ regulation point. $EXTV_{CC}$ may also be connected to any other supply in the system that is higher than the $INTV_{CC}$ regulation point and capable of providing the MOSFET gate drive current.

For the previous example, Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in the previous example from 125°C to:

$T_J = 70°C + (20mA)(8.5V)(68°C/W) = 82°C$

However, for 3.3V and other low voltage outputs, where the output is less than the $INTV_{CC}$ regulation point and no other supply available in the system, additional circuitry is required to derive $INTV_{CC}$ power from the output.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from the LTC7803-3.3's switching regulator output during normal operation and from the V_{IN} LDO when the output is out of regulation (e.g., start-up, short-circuit).

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The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Grounded. This will cause $INTV_{CC}$ to be powered from the internal 5.15V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ Connected Directly to V_{OUT}. This is the normal connection for a 5V to 30V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ Connected to an External Supply. If an external supply is available in the 5V to 30V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. The supply may be higher or lower than V_{IN}, however, a lower $EXTV_{CC}$ voltage results in higher efficiency.
4. $EXTV_{CC}$ Connected to an Output-Derived Boost Network. For regulators where the output is below 5V, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 5V.

Topside MOSFET Driver Supply C_B

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Block Diagram is charged through external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET. For a typical application, a value of $C_B = 0.1\mu F$ is generally sufficient.

The external diode D_B can be a Schottky diode or P-N Junction diode, but in either case it should have low leakage and fast recovery. Pay close attention to the reverse leakage at high temperatures, where it generally increases substantially.

The topside MOSFET driver includes an internal charge pump that delivers current to the bootstrap capacitor when the top MOSFET is on continuously, such as when the output is in dropout (100% duty cycle). The boost diode should have a reverse leakage less than the available output current the charge pump can supply. Curves displaying the available charge pump current under different operating conditions can be found in the Typical Performance Characteristics section.

Phase-Locked Loop and Frequency Synchronization

The LTC7803-3.3 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter, and a voltage-controlled oscillator (VCO). This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input.

If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, CLP, holds the voltage at the VCO input. Note that the LTC7803-3.3 can only be synchronized to an external clock whose frequency is within range of the LTC7803-3.3's internal VCO, which is nominally 100kHz to 3MHz.

This is guaranteed to be between 100kHz and 3MHz. Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.1V.

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Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the LTC7803-3.3 operates in forced continuous mode if the MODE pin is set to Burst Mode operation or forced continuous operation. If the MODE pin is set to pulse-skipping operation, the LTC7803-3.3 maintains pulse-skipping operation when synchronized.

Setting the Operating Frequency

The switching frequency is set using the FREQ and PLLIN/SPREAD pins as shown in Table 1.

Table 1.

FREQ PIN	PLLIN/SPREAD PIN	FREQUENCY
0V	0V	375kHz
$INTV_{CC}$	0V	2.25MHz
Resistor	0V	100kHz to 3MHz
Any of the Above	External Clock 100kHz to 3MHz	Phase Locked to External Clock
Any of the Above	$INTV_{CC}$	Spread Spectrum f_{OSC} modulated 0% to 20%

Tying the FREQ pin to ground selects 375kHz while tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and ground allows the frequency to be programmed anywhere between 100kHz and 3MHz. Choose a FREQ pin resistor from Figure 8 or the following equation:

$$R_{FREQ}\,(\text{in k}\Omega) = \frac{37\text{MHz}}{f_{OSC}}$$

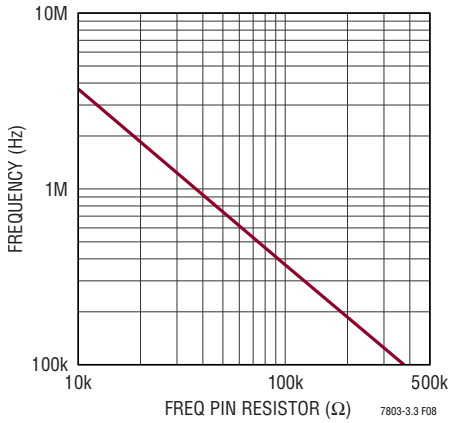

Figure 8. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, spread spectrum mode can optionally be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum in enabled, the switching frequency varies within 0% to +20% of the frequency selected by the FREQ pin. Spread spectrum may be used in any operating mode selected by the MODE pin (Burst Mode, pulse-skipping, or forced continuous mode).

Selecting the Light-Load Operating Mode

The LTC7803-3.3 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode at light load currents. To select Burst Mode operation, tie the MODE to ground. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to $INTV_{CC}$ through a 100k resistor. An internal 100k resistor from the MODE pin to ground selects Burst Mode if the pin is floating. When synchronized to an external clock through the PLLIN/SPREAD pin, the LTC7803-3.3 operates in pulse skipping mode if it is selected, or in forced continuous mode otherwise. Table 2 summarizes the use of the MODE pin to select the light load operating mode.

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Table 2.

MODE PIN	LIGHT-LOAD OPERATING MODE	MODE WHEN SYNCHRONIZED
0V or Floating	Burst Mode	Forced Continuous
100k to $INTV_{CC}$	Pulse-Skipping	Pulse-Skipping
$INTV_{CC}$	Forced Continuous	Forced Continuous

In general, the requirements of each application will dictate the appropriate choice for light-load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the regulator operates in discontinuous operation. In addition, when the load current is very light, the inductor current will begin bursting at frequencies lower than the switching frequency, and enter a low current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light load.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of load. In this mode, the efficiency at light loads is considerably lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher light load efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple and EMI.

In some applications, it may be desirable to change light load operating mode based on the conditions present in the system. For example, if a system is inactive, one might select high efficiency Burst Mode operation by keeping the MODE pin set to 0V. When the system wakes, one might send an external clock to PLLIN/SPREAD, or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. Such on-the-fly mode changes can allow an individual application to benefit from the advantages of each light load operating mode.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC7803-3.3 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \bullet f}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC7803-3.3 is approximately 40ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 60ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Fault Conditions: Current Limit and Current Foldback

The LTC7803-3.3 includes current foldback to help limit load current when the output is shorted to ground. If the output voltage falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100% to 40% of its maximum selected value. Under short-circuit conditions with very low duty cycles, the LTC7803-3.3 will begin cycle skipping in order to

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limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC7803-3.3 (≈40ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)}\left(\frac{V_{IN}}{L}\right)$$

The resulting average short-circuit current is:

$$I_{L(SC)} = 40\% \bullet I_{LIM(MAX)} - \frac{1}{2}\Delta I_{L(SC)}$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator detects faults greater than 10% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating on chip, the overtemperature shutdown circuitry will shut down the LTC7803-3.3. When the junction temperature exceeds approximately 180°C, the overtemperature circuitry disables the $INTV_{CC}$ LDO, causing the $INTV_{CC}$ supply to collapse and effectively shut down the entire LTC7803-3.3 chip. When the junction temperature drops back to approximately 160°C, the $INTV_{CC}$ LDO turns back on. Long-term overstress ($T_J > 125°C$) should be avoided as it can degrade the performance or shorten the life of the part.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7803-3.3 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where QT and QB are the gate charges of the topside and bottom side MOSFETs.

   Supplying $INTV_{CC}$ from an output-derived source power through $EXTV_{CC}$ will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

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3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 30mΩ, R_L = 50mΩ, R_{SENSE} = 10mΩ and R_{ESR} = 40mΩ (sum of both input and output capacitance losses), then the total resistance is 130mΩ. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. This percentage loss varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!
4. Transition losses apply only to the top MOSFET and become significant only when operating at higher output voltages (typically 15V or greater) or higher frequencies (typically in the MHz range). Transition losses can be estimated from the equation for the main switch power dissipation in the Power MOSFET Selection section.

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that CIN has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including body diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the first page circuit will provide an adequate starting point for most applications.

The ITH series RC-CC filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be

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used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing RC and the bandwidth of the loop will be increased by decreasing C_C. If RC is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 22V (Max), V_{OUT} = 3.3V, I_{MAX} = 20A, $V_{SENSE(MAX)}$ = 50mV and f = 1MHz.

The frequency is not one of the internal preset values, so a resistor from the FREQ pin to GND is required, with a value of:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{1\text{MHz}} = 37\text{k}\Omega$$

The inductance value is chosen based on a 30% ripple current target. The highest value of ripple current occurs at the maximum input voltage. The minimum inductance for 25% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

A 0.47µH inductor will produce 25% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 22.5A. Increasing the ripple current will also help ensure that the minimum on-time of 40ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{3.3\text{V}}{22\text{V}(1\text{MHz})} = 150\text{ns}$$

The equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (50mV):

$$R_{SENSE} \le \frac{45\text{mV}}{22.5\text{A}} = 0.002\Omega$$

To allow for additional margin, a lower value R_{SENSE} may be used (for example, 1.8mΩ); however, be sure that the inductor saturation current has sufficient margin above $V_{SENSE(MAX)}/R_{SENSE}$, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.

The best way to evaluate MOSFET performance in a particular application is to build and test the circuit on the bench, facilitated by an LTC7803-3.3 demo board. However, an educated guess about the application is helpful to initially select MOSFETs. Since this is a high current, low voltage application, I^2R losses will likely dominate over transition losses for the top MOSFET. Therefore, choose a MOSFET with lower $R_{DS(ON)}$ as opposed to lower gate charge to minimize the combined loss terms. The bottom MOSFET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the bottom MOSFET is typically chosen to be of lower $R_{DS(ON)}$ and subsequently higher gate charge than the top MOSFET.

Due to the high current in this application, two MOSFETs may needed in parallel to more evenly balance the dissipated power and to lower the $R_{DS(ON)}$. Be sure to select logic-level threshold MOSFETs, since the gate drive voltage is limited to 5.15V ($INTV_{CC}$).

APPLICATIONS INFORMATION

C_{IN} is chosen for an RMS current rating of at least 10A (I_{OUT}/2, with margin) at temperature. C_{OUT} is chosen with an ESR of 0.03Ω for low output ripple. Multiple capacitors connected in parallel may be required to reduce the ESR to this level. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.03\Omega(5A) = 15mV_{P-P}$$

On the 3.3V output, this is equal to 0.45% of peak to peak voltage ripple

Determine the bias supply components. Since the regulated output is not greater than the $EXTV_{CC}$ switchover threshold (4.7V), it cannot be used to bias $INTV_{CC}$. However, if another supply is available, connect that supply to $EXTV_{CC}$ to improve the efficiency. For an 8ms soft start, select a 0.1µF capacitor for the TRACK/SS pin. As a first pass estimate for the bias components, select C_{INTVCC} = 4.7µF, boost supply capacitor C_B = 0.1µF.

Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUN pin can be used to control the minimum input voltage for regulator operation or can be tied to V_{IN} for always-on operation. Use ITH compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 9. Figure 10 illustrates the current waveforms present in the various branches the synchronous regulator operating in the continuous mode.

Check the following in your layout:

1. Are the signal and power grounds kept separate? The LTC7803-3.3 ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The area of the "hot loop" formed by the top N-channel MOSFET, bottom N-channel MOSFET and the high-frequency (ceramic) input capacitors should be minimized with short leads, planar connections, and multiple paralleled vias where needed. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.
2. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
3. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the GND pin? This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance substantially. The boost diodes should have separate routes directly to the $INTV_{CC}$ capacitor near the IC, not shared with any signal connections to $INTV_{CC}$.
4. Keep the SW, TG, and BOOST nodes away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC7803-3.3 and occupy minimum external layer PC trace area. Minimize the inductance of the TG and BG gate drive traces and their respective return paths to the controller IC (SW and GND) by using short wide traces and multiple parallel vias.
5. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

For more detailed layout guidance, see Analog Devices Application Notes AN136 "PCB Layout Considerations for Non-Isolated Switching Power Supplies" and AN139 "Power Supply Layout and EMI".

APPLICATIONS INFORMATION

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

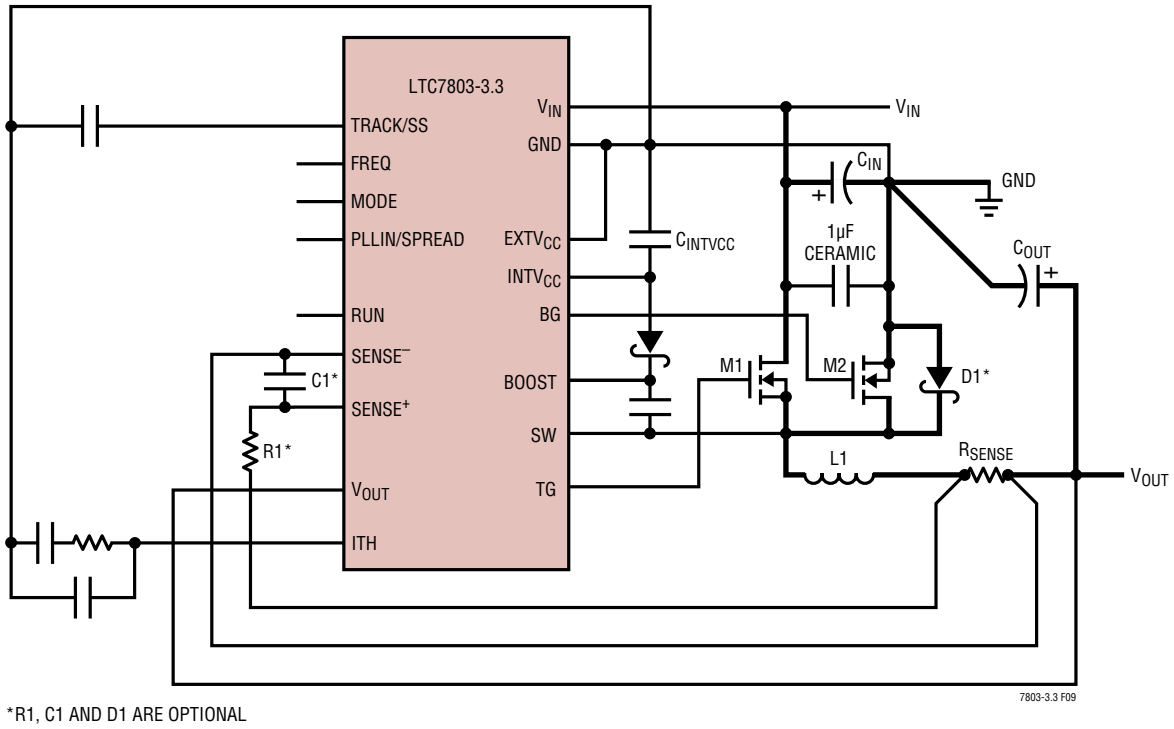
The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, top MOSFET and the bottom MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

APPLICATIONS INFORMATION



*R1, C1 AND D1 ARE OPTIONAL

Figure 9. Recommended Printed Circuit Layout Diagram

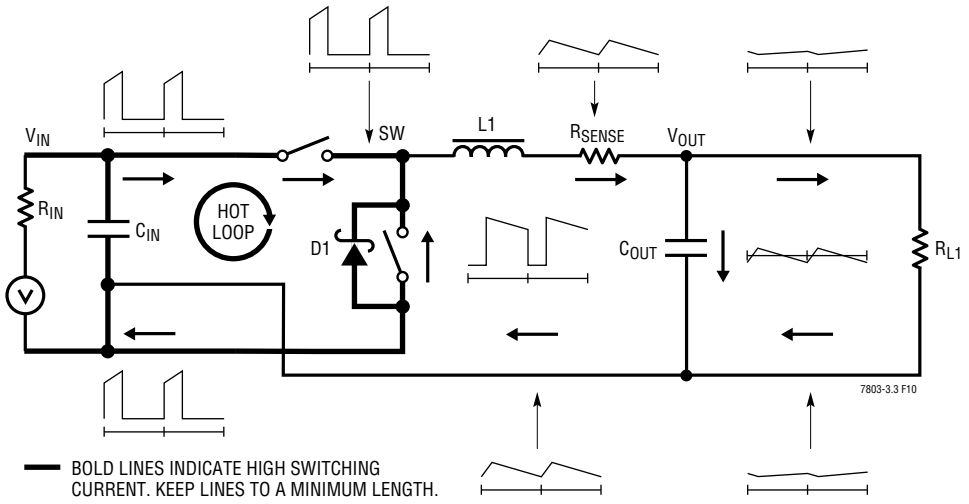
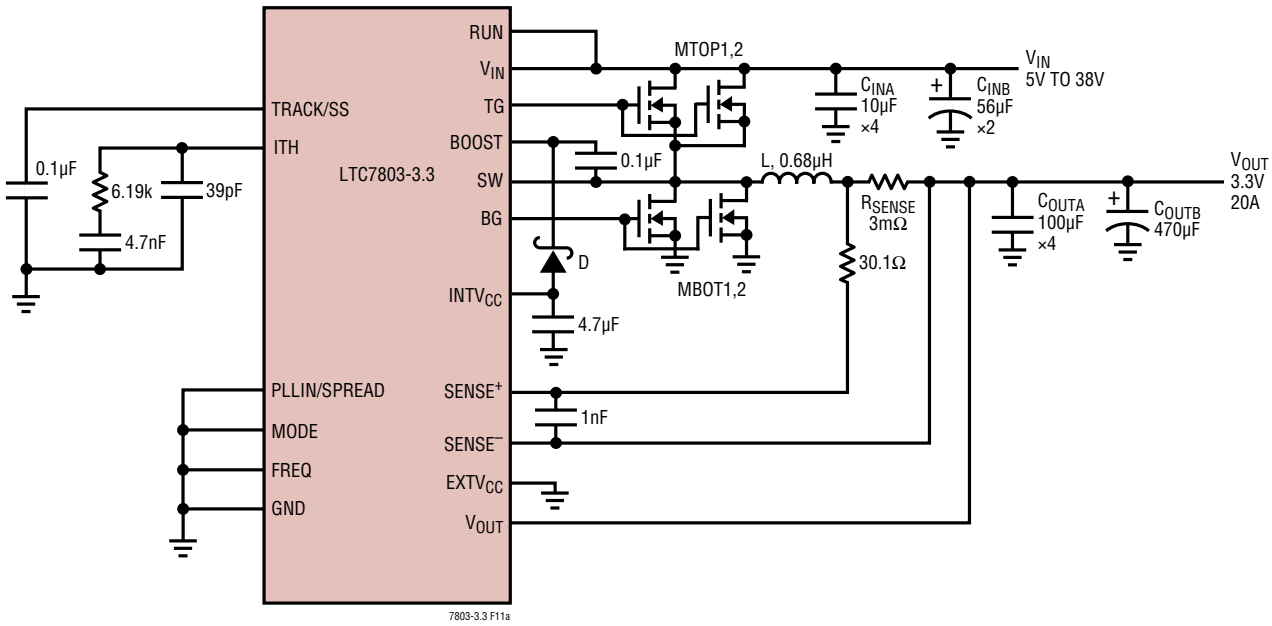


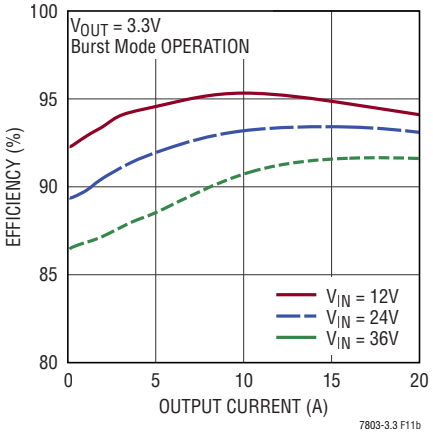
Figure 10. Branch Current Waveforms

TYPICAL APPLICATIONS



MTOP1,2: INFINEON BSC059N04LS6
MBOT1,2: INFINEON BSC022N04LS6
L: WURTH 7843320068
C_{INA}: SAMSUNG CL32B106KMVNNWE
C_{INB}: SUNCON 50HVH56M
C_{OUTA}: MURATA GRM31CR60J107ME39L
C_{OUTB}: PANASONIC 6TPE470MI
D: INFINEON BAS140W

Efficiency vs Output Current



No-Load Burst Mode Input Current vs Input Voltage

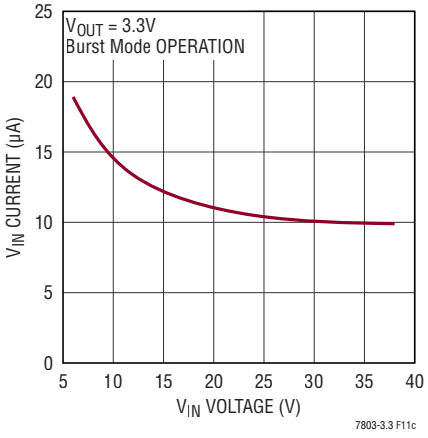
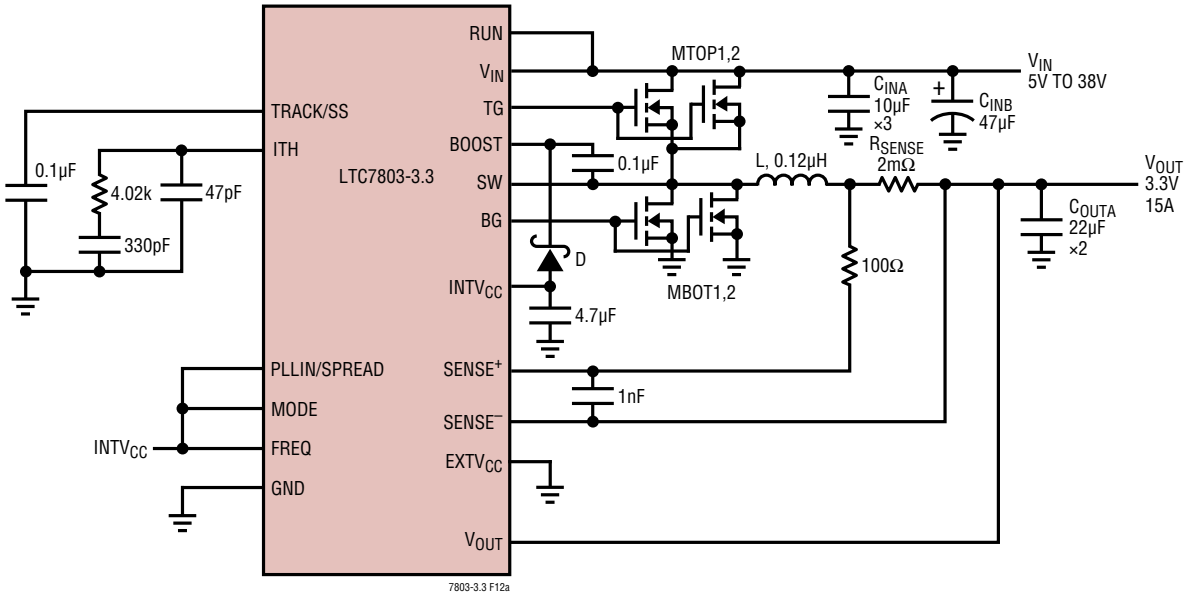
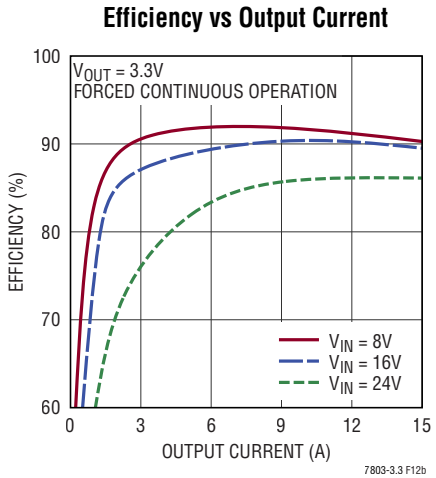


Figure 11. High Efficiency Wide Input Range 375kHz 3.3V/20A Step-Down Regulator

TYPICAL APPLICATIONS



MTOP1,2: ONSEMI NVMFS5C682NL
MBOT1,2: INFINEON BSC059N04LS6
L: COILCRAFT SLC1175-121
C_{INA}: SAMSUNG CL32B106KMVNNWE
C_{INB}: SUNCON 50CE47LX
C_{OUT}: KEMET C1206C226M9RAC
D: CENTRAL SEMI CMDSH-4E



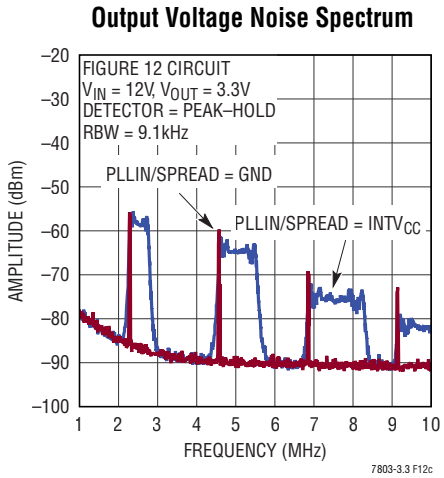
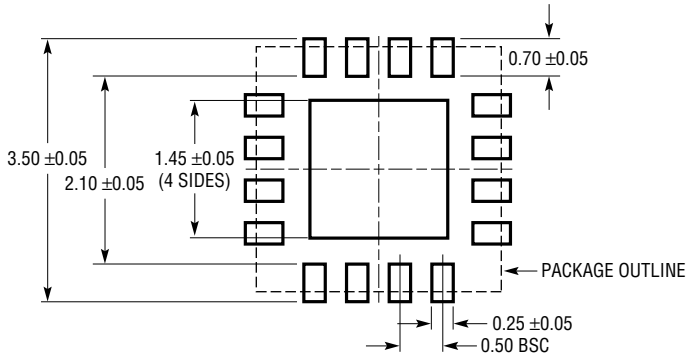


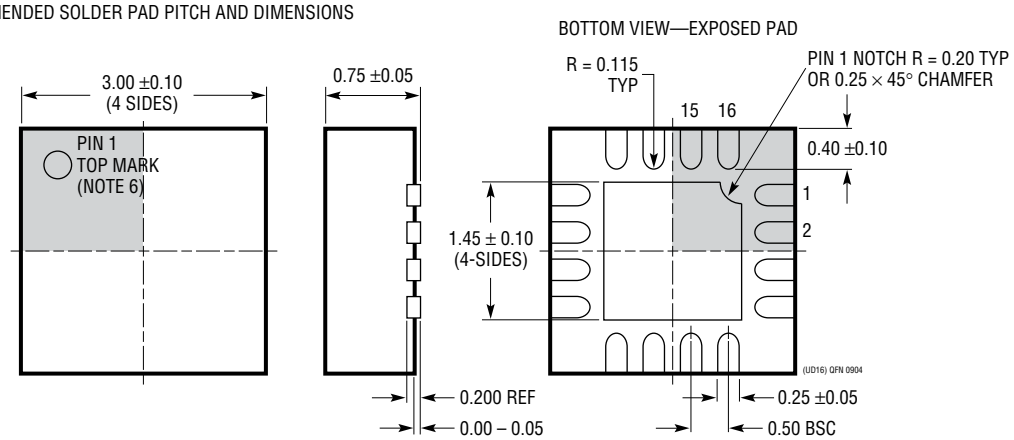
Figure 12. High Efficiency 2.25MHz Wide Input Range 3.3V/15A Step-Down Regulator with Spread Spectrum

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691 Rev Ø)



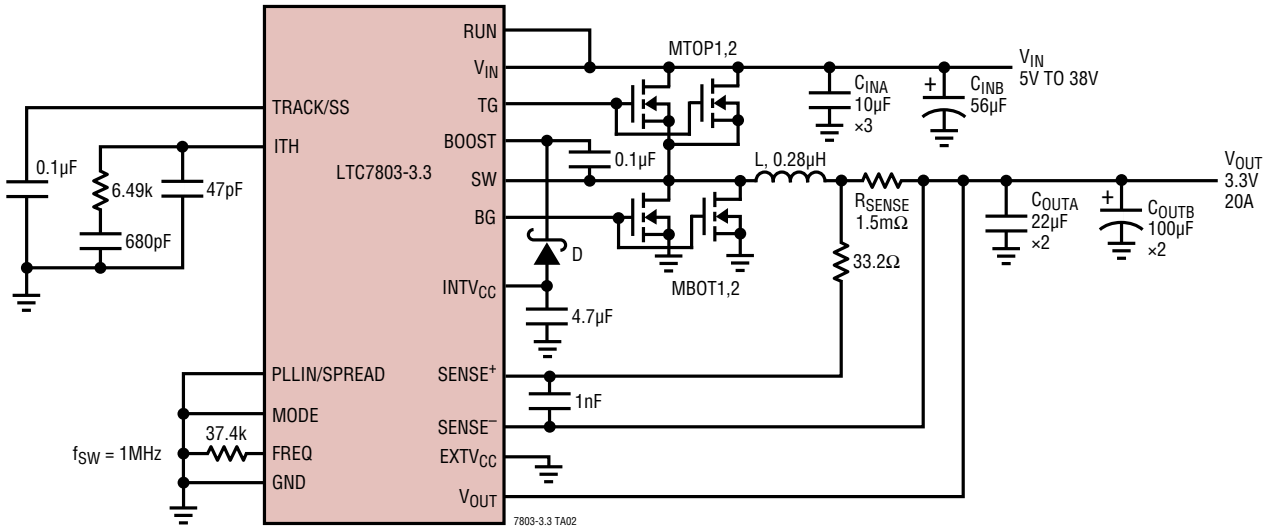
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

High Efficiency Wide Input Range 1MHz 3.3V/20A Step-Down Regulator



MTOP1,2: INFINEON BSC059N04LS6
MBOT1,2: INFINEON BSC022N04LS6
L: WURTH 7443082022
C_{INA}: SAMSUNG CL32B106KMVNNWE
C_{INB}: SUNCON 50HVH56M
C_{OUTA}: KEMET C1206C226M9RAC
C_{OUTB}: PANASONIC 6TPE100MPB
D: CENTRAL SEMI CMDSH-4E

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7800	60V Low I_Q, High Frequency Synchronous Step-Down Controller	$4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, $I_Q = 50\mu A$ PLL Fixed Frequency 320kHz to 2.25MHz, 3mm × 4mm QFN-20
LTC7818	40V, Low I_Q, 3MHz, Triple Output Buck/Buck/Boost Synchronous Controller with Spread Spectrum	$4.5V \le V_{IN} \le 40V$, $I_Q = 14\mu A$, 100% Duty Cycle Capable Boost Buck and Boost V_{OUT} Up to 40V, PLL Fixed Frequency 100kHZ to 3MHz
LTC7804	40V Low I_Q, 3MHz Synchronous Boost Controller 100% Duty Cycle Capable	4.5V(Down to 1V after Start-Up) $\le V_{IN} \le 40V$, V_{OUT} Up to 40V, $I_Q = 14\mu A$ PLL Fixed Frequency 100kHZ to 3MHz, 3mm × 3mm QFN-16, MSOP-16E
LTC3807	Low I_Q, Synchronous Step-Down Controller with 24V Output Voltage Capability	PLL Fixed Frequency 250kHz to 750kHz, $4V \le V_{IN} \le 38V$, $I_Q = 50\mu A$, $0.8V \le V_{OUT} \le 24V$, 3mm × 4mm QFN-20, TSSOP-20
LTC3851A/ LTC3851A-1	No R_{SENSE} Wide V_{IN} Range Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 250kHz to 750kHz, $4V \le V_{IN} \le 38V$, $0.8V \le V_{OUT} \le 5.25V$, MSOP-16E, 3mm × 3mm QFN-16, SSOP-16
LTC3878/ LTC3879	No R_{SENSE} Constant On-Time Synchronous Step-Down DC/DC Controller	Very Fast Transient Response, $t_{ON(MIN)}$ = 43ns, $4V \le V_{IN} \le 38V$, $0.6V \le V_{OUT} \le 0.9V_{IN}$, SSOP-16, MSOP-16E, 3mm × 3mm QFN-16
LTC3775	High Frequency Synchronous Voltage Mode Step-Down DC/DC Controller	Very Fast Transient Response, $t_{ON(MIN)}$ = 30ns, $4V \le V_{IN} \le 38V$, $0.6V \le V_{OUT} \le 0.8V_{IN}$, MSOP-16E, 3mm × 3mm QFN-16
LTC3854	Small Footprint Synchronous Step-Down DC/DC Controller	Fixed 400kHz Operating Frequency, $4.5V \le V_{IN} \le 38V$, $0.8V \le V_{OUT} \le 5.25V$, 2mm × 3mm QFN-12
LTC3866	Fast Accurate Step-Down DC/DC Controller with Differential Output Sensing	PLL Fixed Frequency 250kHz to 770kHz, Remote Sense, $4.5V \le V_{IN} \le 38V$, $0.6V \le V_{OUT} \le 3.5V$
LTC3833	2MHz Current Mode Synchronous Controller for Sub mΩ DCR Sensing	PLL Fixed Frequency 200kHz to 2MHz, $4.5V \le V_{IN} \le 38V$, $0.6V \le V_{OUT} \le 5.5V$
LTC3856	2-Phase, Single Output Synchronous Step-Down DC/DC Controller with Diff Amp and DCR Temp Compensation	PLL Fixed 250kHz to 770kHz Frequency, $4.5V \le V_{IN} \le 38V$, $0.6V \le V_{OUT} \le 5.25V$
LTC3850/ LTC3850-1	2-Phase, Dual Output Synchronous Step-Down DC/DC Controllers, R_{SENSE} or DCR Current Sensing	PLL Fixed Frequency 250kHz to 780kHz, $4V \le V_{IN} \le 30V$, $0.8V \le V_{OUT} \le 5.25V$, 4mm × 4mm QFN-28, 4mm × 5mm QFN-28, SSOP-28