

LTM4616

Dual 2.7V_{IN(MIN)}, 8A Step-Down μModule Regulator

DESCRIPTION

Demonstration circuit 1245A features the LTM[®]4616, the high efficiency, high density, dual output switch mode power module. The rated load current is 8A for each channel, while derating is necessary for certain V_{IN} , V_{OUT} , and thermal conditions. By applying a clock signal to the CLKIN pin, the module's switching frequency may be synchronized from 0.75MHz to 2.25MHz. The same clock frequency is available at the CLKOUT pin with the phase relationship between CLKIN and CLKOUT determined by the PHMODE pin. This feature can be used not only to reduce undesirable

frequency harmonics but also to parallel the two channels of LTM4616 or even multiple LTM4616s and LTM4608s to provide higher output currents. The LTM4616 data sheet must be read in conjunction with this demo manual prior to working on or modifying demo circuit DC1245A.

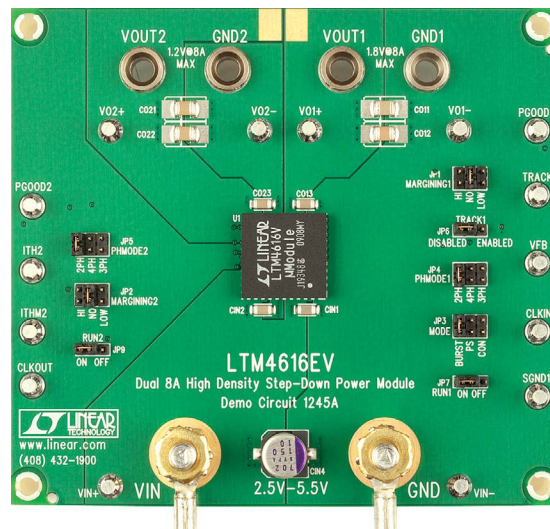
Design files for this circuit board are available at <http://www.linear.com/demo/DC1245A>

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PERFORMANCE SUMMARY (T_A = 25°C)

| PARAMETER | CONDITIONS | VALUE |
|---|---|--|
| Input Voltage Range | | 2.7V to 5.5V |
| Output Voltage V_{OUT1} V_{OUT2} | $V_{IN} = 3.3V$, $I_{OUT1} = 8A$ $I_{OUT2} = 8A$ | 1.8 ±2% 1.2 ±2% |
| Maximum Continuous Output Current | Derating Is Necessary for Certain V_{IN} , V_{OUT} , and Thermal Conditions, See Data Sheet for Details | 8A _{DC} Each Channel |
| Default Operating Frequency | | 1.5MHz |
| Efficiency | $V_{IN} = 5V$, $V_{OUT1} = 1.8V$, $V_{OUT2} = 1.2V$, 8A Per Channel | 77.5%, See Figure 3 for More Information |
| Load Transient | $V_{IN} = 3.3V$, $V_{OUT1} = 1.8V$; $V_{OUT2} = 1.2V$ | See Figures 4 and 5 for Details |

BOARD PHOTO



dc1245afa

DEMO MANUAL DC1245A

QUICK START PROCEDURE

Demonstration circuit 1245A is an easy way to evaluate the performance of the LTM4616. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions for a typical $1.8V_{OUT}$ and $1.2V_{OUT}$ application:

| PHMODE2 | MARGINING2 | RUN2 | MARGINING1 |
|---------|------------|------|------------|
| 2PH | NO | ON | NO |

| TRACK1 | PHMODE1 | MODE | RUN1 |
|----------|---------|-------|------|
| DISABLED | 2PH | BURST | ON |

2. With power off, connect the input power supply, load and meters as shown in Figure 1. Preset the load to 0A and V_{IN} supply within the 2.7V to 5.5V operating range.
3. Turn on the power at the input. The output voltage at $VO1^+$ and $VO1^-$ should be $1.8V \pm 2\%$ and the voltage at $VO2^+$ and $VO2^-$ should be $1.2V \pm 2\%$.

4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters. To measure input and output ripple, please refer to Figure 2 for proper setup.
5. To synchronize channel 1 to an external clock, please apply the desired clock signal to CLKIN and SGND1. The external clock signal should have amplitude of at least 2V but less than V_{IN} .
6. V_{OUT1} can track another supply connected at TP20 as determined by resistors R6 and R17. V_{OUT2} is set up to track V_{OUT1} in a manner determined by resistors R15 and R16. By default both resistor pairs have been selected to support coincident tracking. Please refer to Figure 6 for reference.

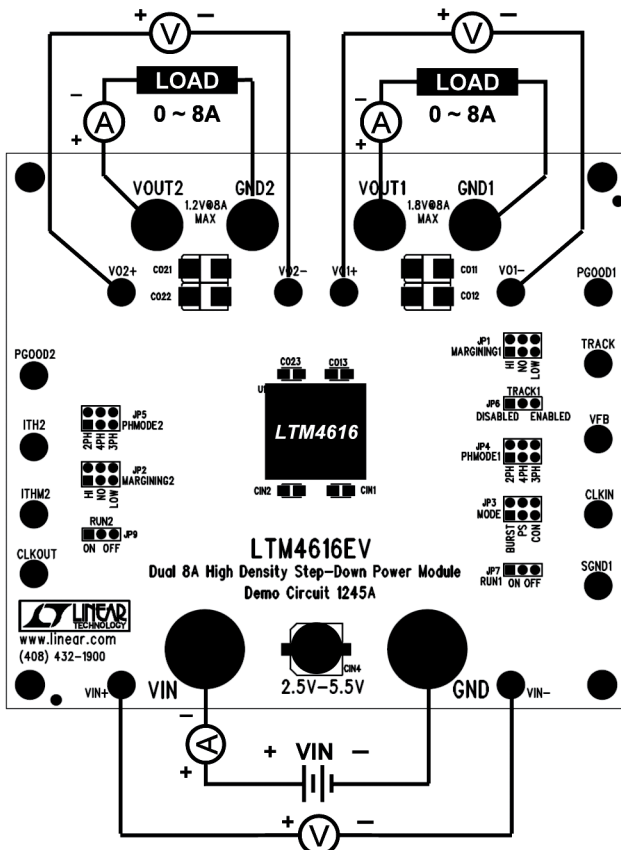


Figure 1. Test Setup of DC1245A

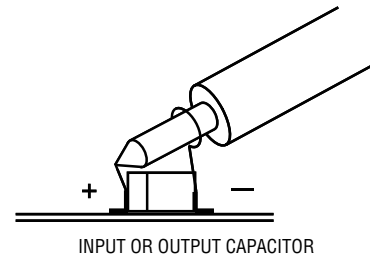


Figure 2. Proper Scope Probe Placement for Measuring Input or Output Ripple

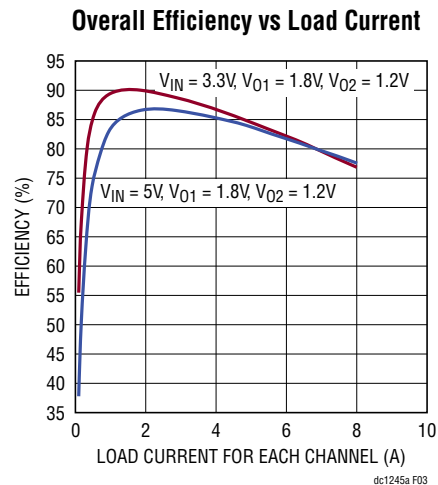
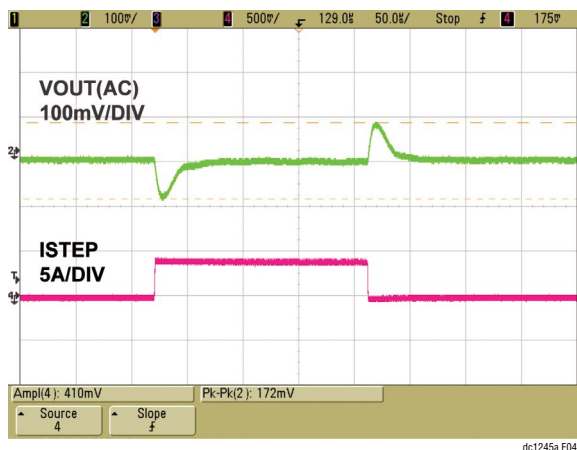


Figure 3. Measured Overall Supply Efficiency with Different V_{IN}

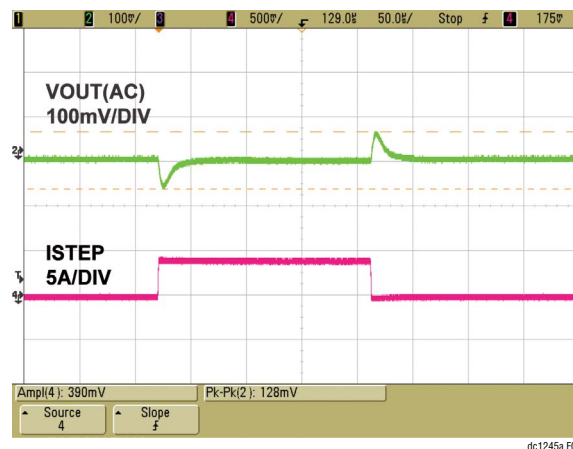
QUICK START PROCEDURE

- Channel 2 is set up to synchronize to the CLKOUT signal of channel 1. The default phase difference is 180°. Please refer to data sheet for how to set up PHMODE1 and PHMODE2 for paralleling more than 2 channels.



$V_{IN} = 3.3V$
 $V_{OUT} = 1.8V$
 CONTINUOUS CURRENT MODE (CCM)
 2A TO 6A LOAD STEP
 $C_{OUT} = \times 2 \text{ } 100\mu F \text{ CERAMIC (1210, X5R, 6.3V) + } 22\mu F \text{ CERAMIC (0805, X5R, 6.3V)}$
 $C_{FF1} = 47pF$
 $V_{OUT} \text{ OVERSHOOT AND UNDERSHOOT} = 172mV$

Figure 4. Measured Load Transient Response for 1.8V_{OUT} (4A Step, 25% to 75%)



$V_{IN} = 3.3V$
 $V_{OUT} = 1.2V$
 CONTINUOUS CURRENT MODE (CCM)
 2A TO 6A LOAD STEP
 $C_{OUT} = \times 2 \text{ } 100\mu F \text{ CERAMIC (1210, X5R, 6.3V) + } 22\mu F \text{ CERAMIC (0805, X5R, 6.3V)}$
 $C_{FF2} = 0pF$
 $V_{OUT} \text{ OVERSHOOT AND UNDERSHOOT} = 128mV$

Figure 5. Measured Load Transient Response for 1.2V_{OUT} (4A Step, 25% to 75%)

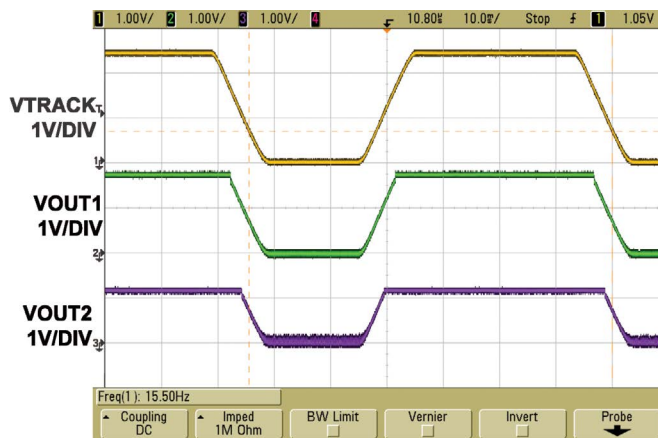


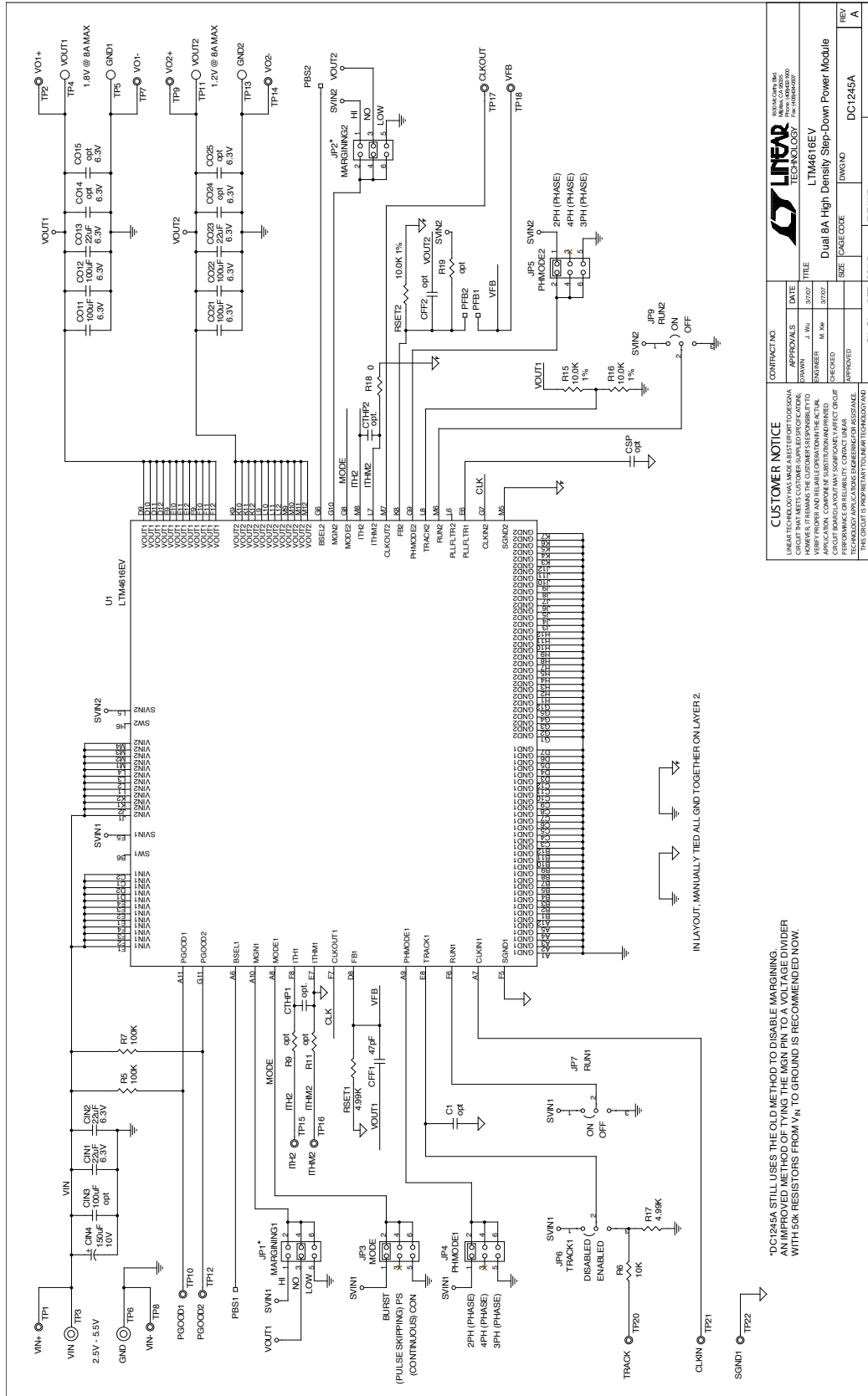
Figure 6. Measured Tracking Performance of V_{OUT1} and V_{OUT2} (with 2A Load Current)

DEMO MANUAL DC1245A

PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|--|-----|--|--|-----------------------------------|
| Required Circuit Components | | | | |
| 1 | 4 | CIN1, CIN2, C013, C023 | Capacitor, X5R, 22µF, 6.3V, 20%, 1206 | AVX, 12066D226MAT2A |
| 2 | 1 | CIN4 | Capacitor, OS-CON, 150µF, 10V, E7 Size | Sanyo, 10SVPA150MAA |
| 3 | 4 | C011, C012, C021, C022 | Capacitor, X5R, 100µF, 6.3V, 20%, 1210 | AVX, 12106D107MAT2A |
| 4 | 1 | RSET1 | Resistor, Chip, 4.99k, 1/16W, 1%, 0402 | Vishay, CRCW04024K99FKED |
| 5 | 1 | RSET2 | Resistor, Chip, 10k, 1/16W, 1%, 0402 | Vishay, CRCW040210K0FKED |
| 6 | 1 | U1 | IC LTM4616EV 144-Pin LGA | Linear Technology, LTM4616EV |
| Additional Demo Board Circuit Components | | | | |
| 1 | 0 | C014, C015, C024, C025 (OPT) | Capacitor, 1210-3743 | |
| 2 | 2 | R7, R5 | Resistor, Chip, 100k, 1/16W, 5%, 0402 | Vishay, CRCW0402100KJNED |
| 3 | 0 | R9, R11, R19 (OPT) | Resistor, Chip, 0402 | |
| 4 | 0 | CTHP1, CTHP2, C1, CFF2, CSP (OPT) | Capacitor, 0402 | |
| 5 | 1 | CFF1 | Capacitor, COG, 47pF, 50V, 10%, 0402 | AVX, 04025A470KAT2A |
| 6 | 1 | R17 | Resistor, Chip, 4.99k, 1/16W, 1%, 0402 | Vishay, CRCW04024K99FKED |
| 7 | 3 | R15, R16, R6 | Resistor, Chip, 10k, 1/16W, 1%, 0402 | Vishay, CRCW040210K0FKED |
| 8 | 1 | R18 | Resistor, Chip, 0, 1/16W, 0402 | Vishay, CRCW04020000Z0ED |
| Hardware/Components (For Demo Board Only) | | | | |
| 1 | 0 | CIN3(OPT) | Capacitor, 1210-3743 | |
| 2 | 5 | JP1, JP2, JP3-JP5 | 2 × 3, 0.079 Double Row Header | Samtec, TMM103-02-L-D |
| 3 | 3 | JP6, JP7, JP9 | Header 3-Pin 0.079 Single Row | Samtec, TMM103-02-L-S |
| 4 | 8 | JP1-JP7, JP9 | Shunt, 0.079" Center | Samtec, 2SN-BK-G |
| 5 | 15 | TP1, TP2, TP7-TP10, TP12, TP14-TP18, TP20-TP22 | Testpoint, Turret, 0.094" Pbf | Mill-Max, 2501-2-00-80-00-00-07-0 |
| 6 | 2 | TP6, TP3 | Stud, Test Pin | PEM KFH-032-10 |
| 7 | 4 | TP6, TP3 | Nut, Brass Nuts #10-32 | Any #10-32 |
| 8 | 2 | TP6, TP3 | Ring, Lug Ring #10 | Keystone #10 |
| 9 | 2 | TP6, TP3 | Washer, Tin Plated Brass | Any #10 |
| 10 | 4 | TP4, TP5, TP11, TP13 | Jack Banana | Keystone, 575-4 |
| 11 | 4 | (STAND-OFF) | Stand-Off, Nylon 0.50" | Keystone, 8833(SNAP ON) |

SCHEMATIC DIAGRAM



IN LAYOUT, MANUALLY TIE ALL GND TOGETHER ON LAYER2

*DC1245A STILL USES THE OLD METHOD TO DISABLE MARGINING. AN IMPROVED METHOD OF TYING THE MGN PIN TO A VOLTAGE DIVIDER WITH 50K RESISTORS FROM VIN- TO GROUND IS RECOMMENDED NOW.



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DEMO MANUAL DC1245A

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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