3V_{IN} to 40V_{IN} Isolated µModule DC/DC Converter with LDO Post Regulator

FEATURES

- **2kVAC Isolated µModule Converter**
- **UL60950 Recognized File E464570**
- **Wide Input Voltage Range: 3V to 40V**
- **V_{OUT1} Output:**
  - **Up to 450mA (V_{IN} = 24V, V_{OUT1} = 5V)**
  - **2.5V to 18V Output Range**
- **V_{OUT2} Low Noise Linear Post Regulator:**
  - **Up to 300mA**
  - **1.2V to 18V Output Range**
- Current Mode Control
- User Configurable Undervoltage Lockout
- Low Profile (9mm × 11.25mm × 4.92mm) BGA Package

APPLICATIONS

- Industrial Sensors
- Industrial Switches
- Ground Loop Mitigation

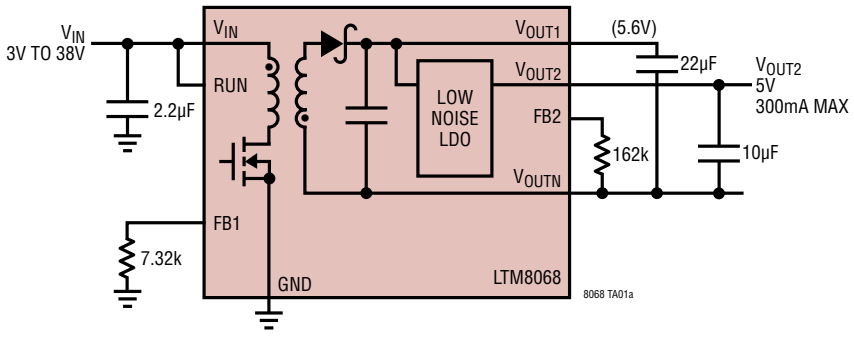
DESCRIPTION

The LTM®8068 is a 2kVAC isolated flyback µModule® (power module) DC/DC converter with LDO post regulator. Included in the package are the switching controller, power switches, transformer, LDO, and all support components. Operating over an input voltage range of 3V to 40V, the LTM8068 supports an output voltage range of 2.5V to 18V, set by a single resistor. There is also a linear post regulator whose output voltage is adjustable from 1.2V to 18V as set by a single resistor. Only output and input capacitors are needed to finish the design.

The LTM8068 is packaged in a thermally enhanced, compact (9mm × 11.25mm × 4.92mm) overmolded ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8068 is available with SnPb or RoHS compliant terminal finish.

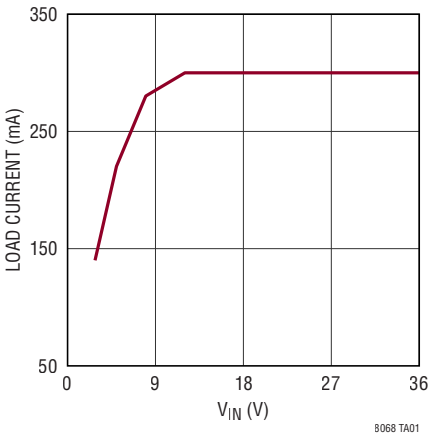
TYPICAL APPLICATION

2kVAC Isolated Low Noise µModule Regulator



PIN BYP IS NOT USED IN THIS SCHEMATIC

Total Output Current vs V_{IN}

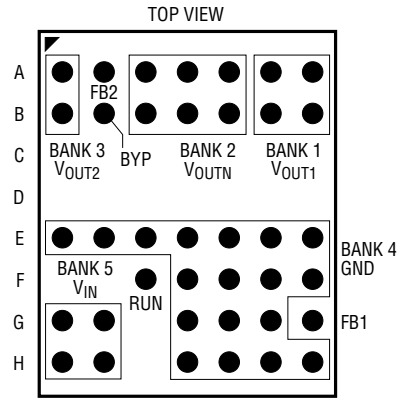


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN 42V
V_{OUT1} Relative to V_{OUTN}.....25V
V_{IN} + V_{OUT1} (Note 2) 45V
V_{OUT2} Relative to V_{OUTN}.....+20V
FB2 Relative to V_{OUTN} .....+7V
GND to V_{OUTN} Isolation (Note 3).....2kVAC
Maximum Internal Temperature (Note 4) ..... 125°C
Maximum Peak Body Reflow Temperature ..... 245°C
Storage Temperature..... –55°C to 125°C

PIN CONFIGURATION



BGA PACKAGE
38-LEAD (11.25mm × 9mm × 4.92mm)

T_{JMAX} = 125°C, θ_{JA} = 18.2°C/W, $\theta_{JCbottom}$ = 4.8°C/W, θ_{JCtop} = 18.1°C/W, θ_{JB} = 4.8°C/W
WEIGHT = 1.1g, θ VALUES DETERMINED PER JESD 51-9, 51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 4)
		DEVICE	FINISH CODE			
LTM8068EY#PBF	SAC305 (RoHS)	LTM8068Y	e1	BGA	3	–40°C to 125°C
LTM8068IY#PBF	SAC305 (RoHS)	LTM8068Y	e1	BGA	3	–40°C to 125°C
LTM8068IY	SnPb (63/37)	LTM8068Y	e0	BGA	3	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges.
- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C, RUN = 2V (Note 4).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input DC Voltage	RUN = 2V	●			3	V
V_{OUT1} DC Voltage	R_{FB1} = 15.4k R_{FB1} = 8.25k R_{FB1} = 2.37k	 ● 	 4.75 	2.5 5 18	 5.25 	V V V
V_{IN} Quiescent Current	V_{RUN} = 0V Not Switching			 7	3 	µA mA
V_{OUT1} Line Regulation	3V ≤ V_{IN} ≤ 40V, I_{OUT} = 0.1A, RUN = 2V			1		%
V_{OUT1} Load Regulation	0.05A ≤ I_{OUT} ≤ 0.3A, RUN = 2V			1		%
V_{OUT1} Ripple (RMS)	I_{OUT} = 0.1A, 1MHz BW			30		mV
Isolation Voltage	(Note 3)			2		kV
Input Short-Circuit Current	V_{OUT1} Shorted			80		mA
RUN Pin Input Threshold	RUN Pin Falling		1.18	1.214	1.25	V
RUN Pin Current	V_{RUN} = 1V V_{RUN} = 1.3V			2.5 	 0.1	µA µA
LDO (V_{OUT2}) Minimum Input DC Voltage	(Note 5)			1.5	2.3	V
V_{OUT2} Voltage Range	V_{OUT1} = 16V, R_{FB2} Open, No Load (Note 5) V_{OUT1} = 16V, R_{FB2} = 41.2k, No Load (Note 5)			1.22 17.7		V V
FB2 Pin Voltage	V_{OUT1} = 2V, I_{OUT2} = 1mA (Note 5) V_{OUT1} = 2V, I_{OUT2} = 1mA (Note 5)	 ●	 1.19	1.22 	 1.25	V V
V_{OUT2} Line Regulation	2V < V_{OUT1} < 16V, I_{OUT2} = 1mA (Note 5)			1	5	mV
V_{OUT2} Load Regulation	V_{OUT1} = 5V, 10mA ≤ I_{OUT2} ≤ 300mA (Note 5)			2	10	mV
LDO Dropout Voltage	I_{OUT2} = 10mA (Note 5) I_{OUT2} = 100mA (Note 5) I_{OUT2} = 300mA (Note 5)			 	0.25 0.34 0.43	V V V
V_{OUT2} Ripple (RMS)	C_{BYP} = 0.01µF, I_{OUT2} = 300mA, BW = 100Hz to 100kHz (Note 5)			20		μV_{RMS}

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: V_{IN} + V_{OUT1} is defined as the sum of:

(V_{IN} – GND) + (V_{OUT1} – V_{OUTN})

Note 3: The LTM8068 isolation test voltage of either 2kVAC or its equivalent of 2.83kVDC is applied for one second.

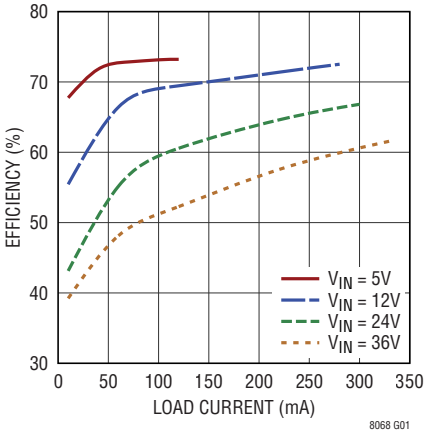
Note 4: The LTM8068E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C internal temperature range are assured by design, characterization and correlation with statistical process controls. LTM8068I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 5: V_{RUN} = 0V (Flyback not running), but the V_{OUT2} post regulator is powered by applying a voltage to V_{OUT1}.

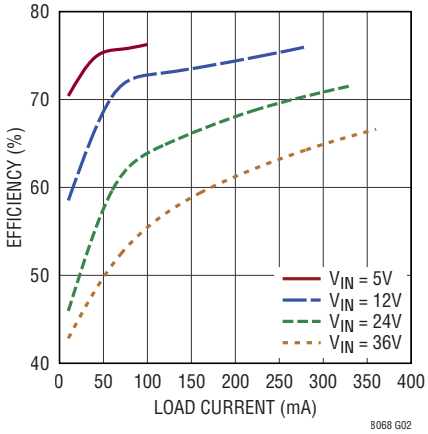
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, operating conditions are as in Table 1 and Table 2 (T_A = 25°C).

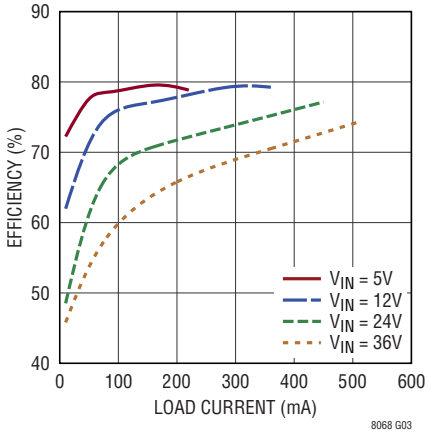
Efficiency vs Load Current, V_{OUT1} = 2.5V



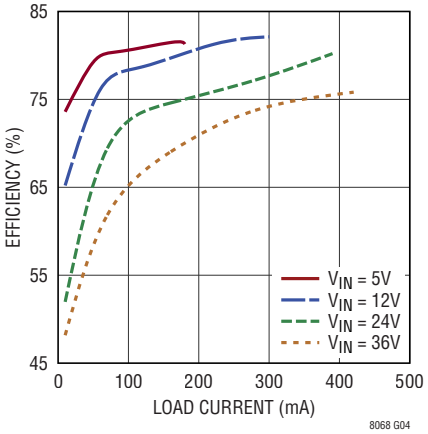
Efficiency vs Load Current, V_{OUT1} = 3.3V



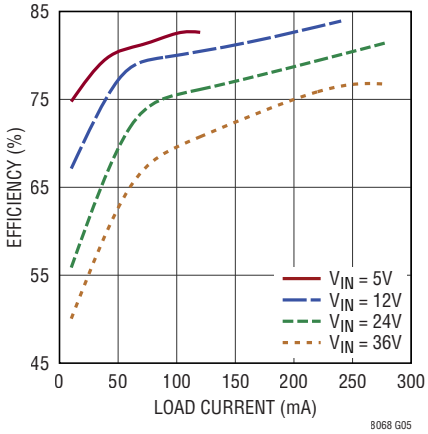
Efficiency vs Load Current, V_{OUT1} = 5V



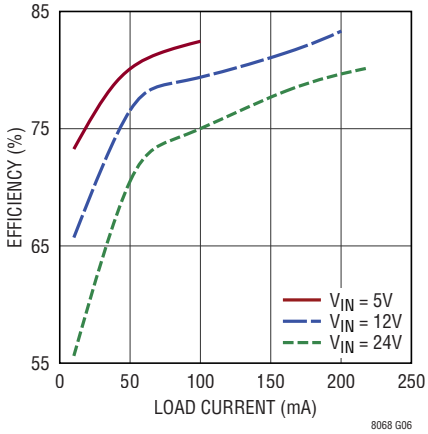
Efficiency vs Load Current, V_{OUT1} = 8V



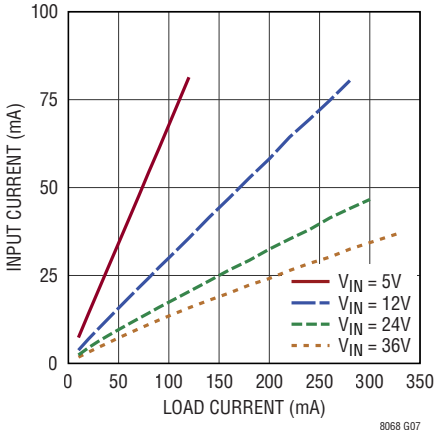
Efficiency vs Load Current, V_{OUT1} = 12V



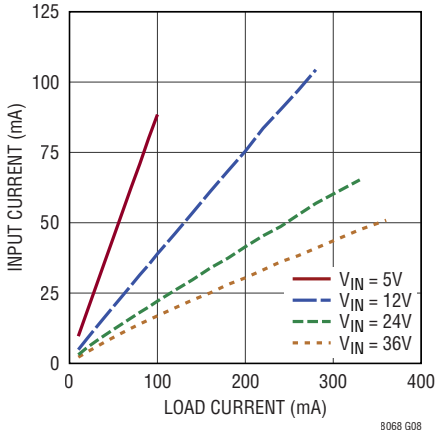
Input Current vs Load Current, V_{OUT1} = 15V



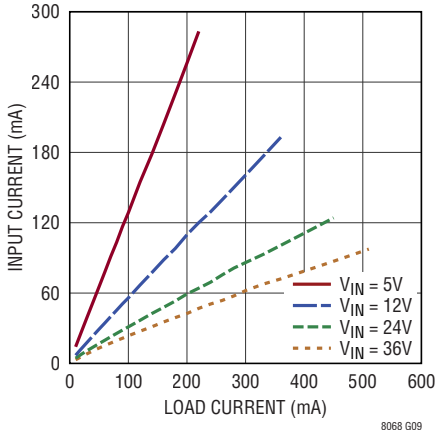
Input Current vs Load Current, V_{OUT1} = 2.5



Input Current vs Load Current, V_{OUT1} = 3.3V



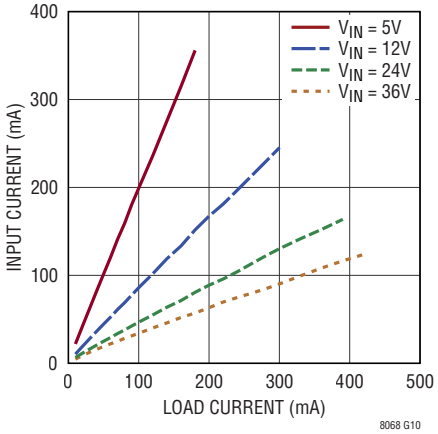
Input Current vs Load Current, V_{OUT1} = 5V



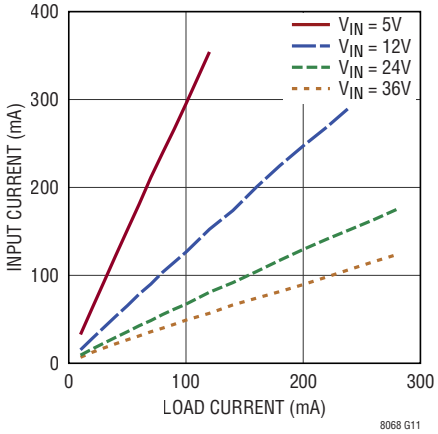
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, operating conditions are as in Table 1 and Table 2 (T_A = 25°C).

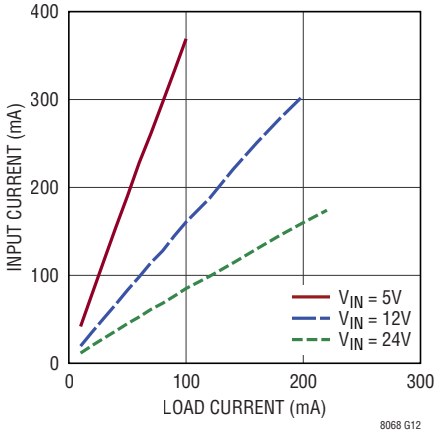
Input Current vs Load Current, V_{OUT1} = 8V



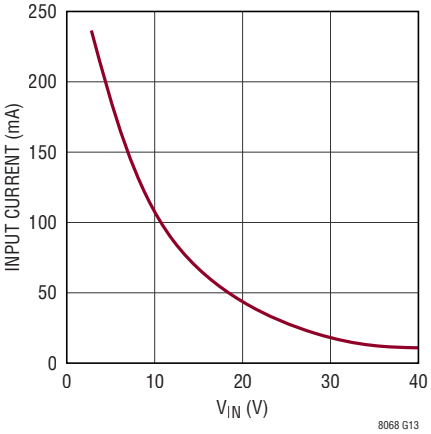
Input Current vs Load Current, V_{OUT1} = 12V



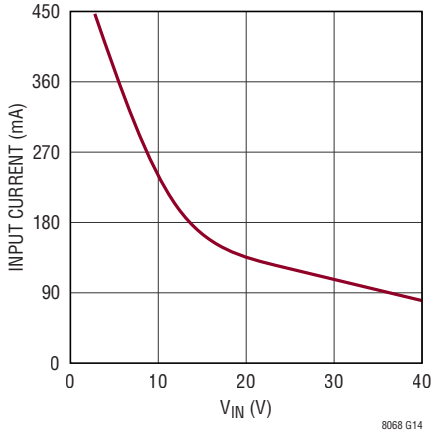
Input Current vs Load Current, V_{OUT1} = 15V



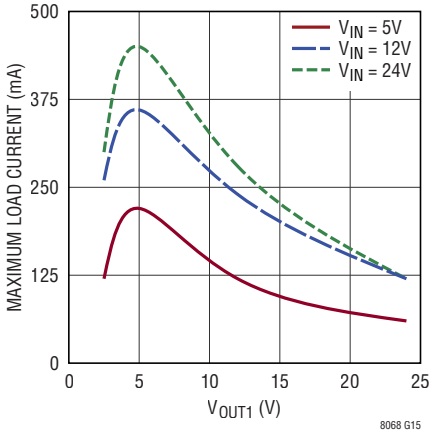
Input Current vs V_{IN}, V_{OUT1} Shorted, V_{OUT2} Open



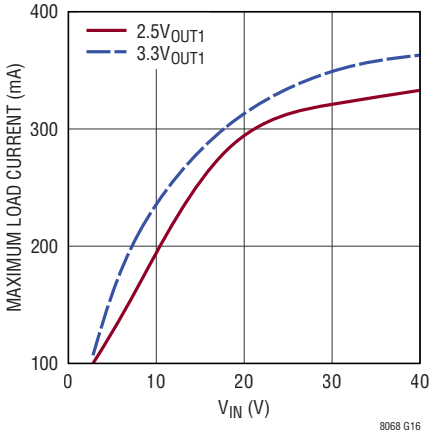
Input Current vs V_{IN}, V_{OUT2} Shorted



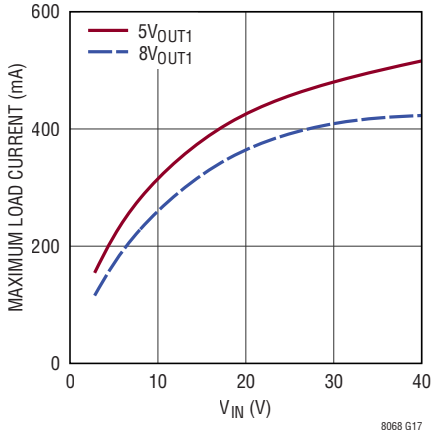
Maximum Load Current vs V_{OUT1}



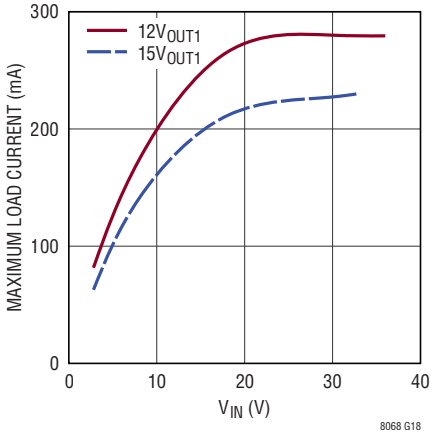
Maximum Load Current vs V_{IN}



Maximum Load Current vs V_{IN}



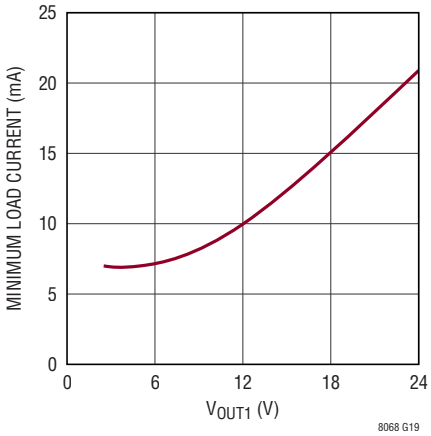
Maximum Load Current vs V_{IN}



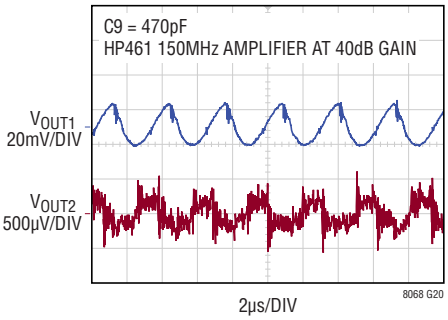
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, operating conditions are as in Table 1 and Table 2 (T_A = 25°C).

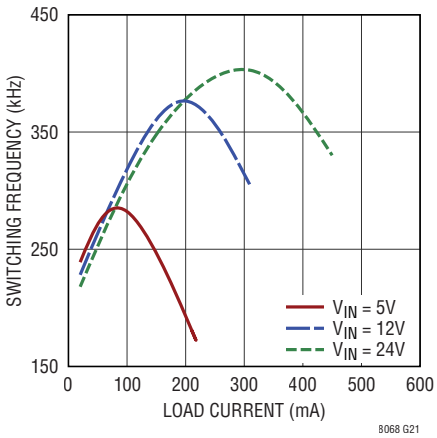
Minimum Load Current vs V_{OUT1} Over Full Input Voltage Range



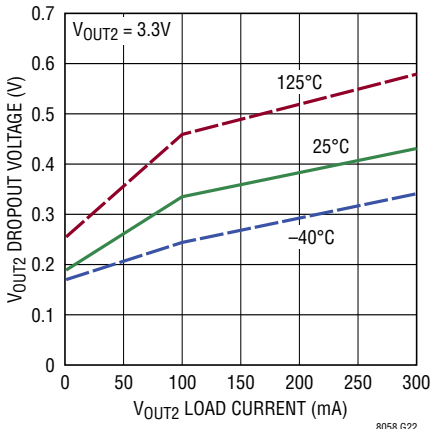
Output Noise and Ripple DC2358A, 200mA Load Current



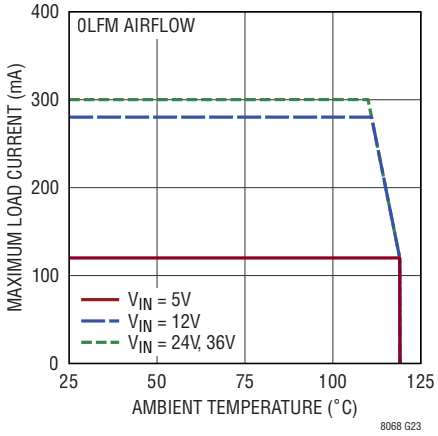
Frequency vs V_{OUT1} Load Current Stock DC2358A Demo Board



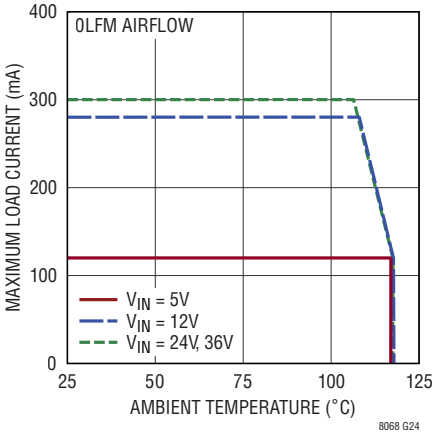
V_{OUT2} Dropout



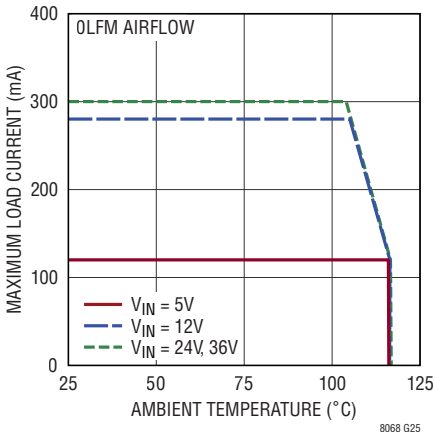
Derating, 1.2V_{OUT2}



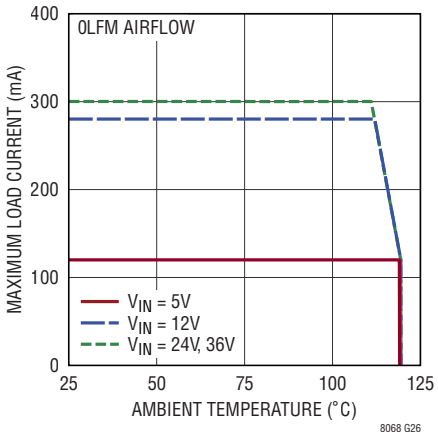
Derating, 1.5V_{OUT2}



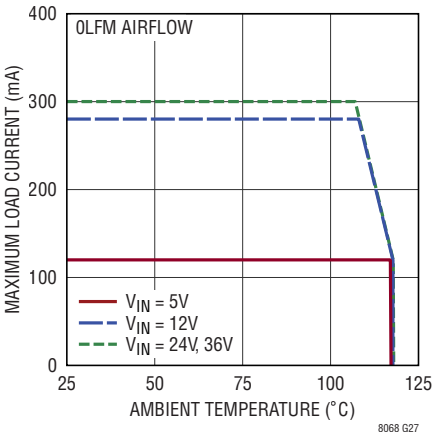
Derating, 1.8V_{OUT2}



Derating, 2.5V_{OUT2}



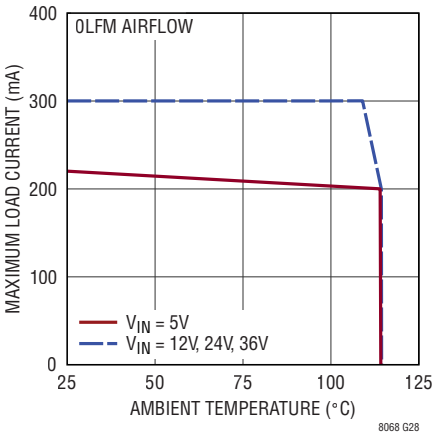
Derating,3.3V_{OUT2}



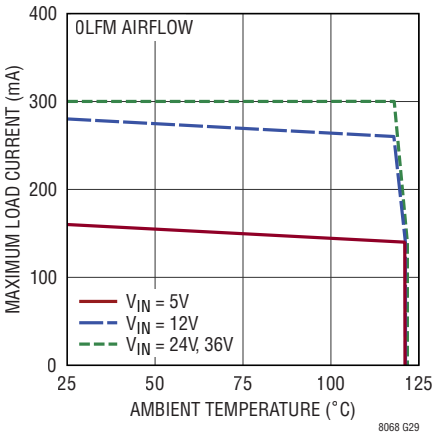
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, operating conditions are as in Table 1 and Table 2 (T_A = 25°C).

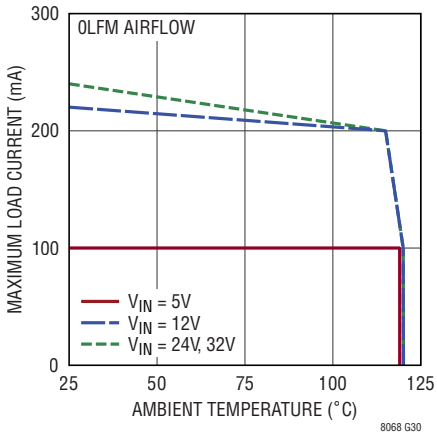
Derating, 5V$_{OUT2}$



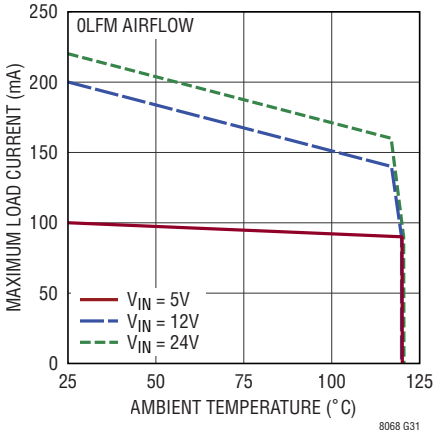
Derating, 8V$_{OUT2}$



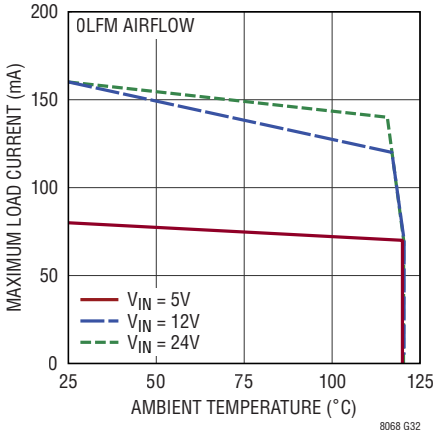
Derating, 12V$_{OUT2}$



Derating, 15V$_{OUT2}$



Derating, 18V$_{OUT2}$



PIN FUNCTIONS

V_{OUT1} (Bank 1): V_{OUT1} and V_{OUTN} comprise the isolated output of the LTM8068 flyback stage. Apply an external capacitor between V_{OUT1} and V_{OUTN}. Do not allow V_{OUTN} to exceed V_{OUT1}.

V_{OUTN} (Bank 2): V_{OUTN} is the return for both V_{OUT1} and V_{OUT2}. V_{OUT1} and V_{OUTN} comprise the isolated output of the LTM8068. In most applications, the bulk of the heat flow out of the LTM8068 is through the GND and V_{OUTN} pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Apply an external capacitor between V_{OUT1} and V_{OUTN}.

V_{OUT2} (Bank 3): The output of the secondary side linear post regulator. Apply the load and output capacitor between V_{OUT2} and V_{OUTN}. See the Applications Information section for more information on output capacitance and reverse output characteristics.

GND (Bank 4): This is the local ground of the LTM8068 primary. In most applications, the bulk of the heat flow out of the LTM8068 is through the GND and V_{OUTN} pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details.

V_{IN} (Bank 5): V_{IN} supplies current to the LTM8068's internal regulator and to the integrated power switch. These pins must be locally bypassed with an external, low ESR capacitor.

FB2 (Pin A2): This is the input to the error amplifier of the secondary side LDO post regulator. This pin is internally clamped to ±7V. The FB2 pin voltage is 1.22V referenced to V_{OUTN} and the output voltage range is 1.22V to 12V. Apply a resistor from this pin to V_{OUTN}, using the equation $R_{FB2} = 608.78/(V_{OUT2} – 1.22)k\Omega$. If the post regulator is not used, leave this pin floating.

BYP (Pin B2): The BYP pin is used to bypass the reference of the LDO to achieve low noise performance from the linear post regulator. The BYP pin is clamped internally to ±0.6V relative to V_{OUTN}. A small capacitor from V_{OUT2} to this pin will bypass the reference to lower the output voltage noise. A maximum value of 0.01µF can be used for reducing output voltage noise to a typical $20\mu V_{RMS}$ over a 100Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

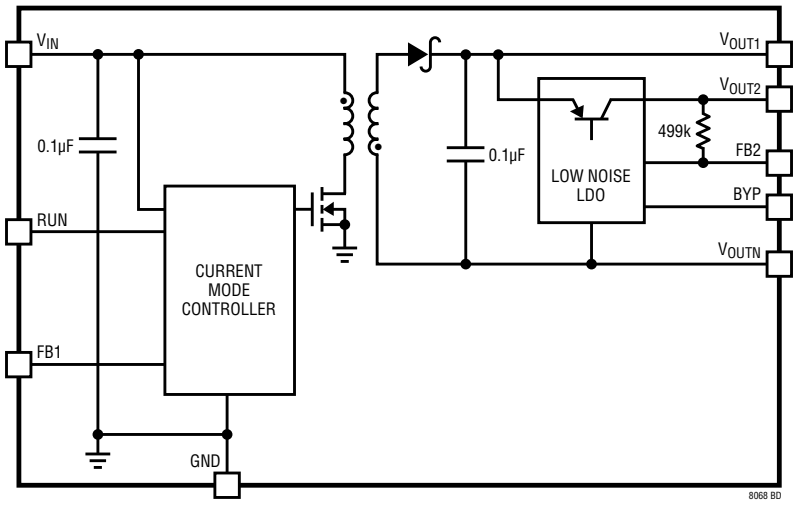
RUN (Pin F3): A resistive divider connected to V_{IN} and this pin programs the minimum voltage at which the LTM8068 will operate. Below 1.24V, the LTM8068 does not deliver power to the secondary. When RUN is less than 1.24V, the pin draws 2.5µA, allowing for a programmable hysteresis. Do not allow a negative voltage (relative to GND) on this pin.

FB1 (Pin G7): Apply a resistor from this pin to GND to set the output voltage V_{OUT1} relative to V_{OUTN}, using the recommended value given in Table 1 and Table 2. If Table 1 and Table 2 do not list the desired V_{OUT1} value, the equation:

$$R_{FB1} = 37.415\left(V_{OUT1}^{-0.955}\right)k\Omega$$

may be used to approximate the value. To the seasoned designer, this exponential equation may seem unusual. The equation is exponential due to nonlinear current sources that are used to temperature compensate the regulation. Do not drive this pin.

BLOCK DIAGRAM



OPERATION

The LTM8068 is a stand-alone isolated flyback switching DC/DC power supply that can deliver up to 450mA of output current at $5V_{OUT1}$, $24V_{IN}$. This module provides a regulated output voltage programmable via one external resistor from 2.5V to 18V. It is also equipped with a high performance linear post regulator. The input voltage range of the LTM8068 is 3V to 40V. Given that the LTM8068 is a flyback converter, the output current depends upon the input and output voltages, so make sure that the input voltage is high enough to support the desired output voltage and load current. The Typical Performance Characteristics section gives several graphs of the maximum load versus V_{IN} for several output voltages.

A simplified block diagram is given. The LTM8068 contains a current mode controller, power switching element, power transformer, power Schottky diode, a modest amount of input and output capacitance, and a high performance linear post regulator.

The LTM8068 has a galvanic primary to secondary isolation rating of 2kVAC. For details please refer to the Isolation, Working Voltage and Safely Compliance section. The LTM8068 is a UL 60950 recognized component.

The RUN pin is used to turn on or off the LTM8068, disconnecting the output and reducing the input current to 1µA or less.

The LTM8068 is a variable frequency device. For a given input and output voltage, the frequency increases from light load through moderate load, then begins to decrease until full load is reached. An example of this is shown in the Typical Performance Characteristics section. For light loads, the current through the internal transformer may be discontinuous.

The post regulator is a high performance 300mA low dropout regulator with micropower quiescent current and shutdown. The device is capable of supplying 300mA at a dropout voltage of 430mV. Output voltage noise can be lowered to $20\mu V_{RMS}$ over a 100Hz to 100kHz bandwidth with the addition of a 0.01µF reference bypass capacitor. Additionally, this reference bypass capacitor will improve transient response of the regulator, lowering the settling time for transient load conditions. The linear regulator is protected against both reverse input and reverse output voltages.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 (or Table 2, if the post linear regulator is used) and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT1}, C_{OUT2}, R_{FB1} and R_{FB2} as required.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current may be limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

Capacitor Selection Considerations

The C_{IN}, C_{OUT1} and C_{OUT2} capacitor values in Table 1 and Table 2 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 and Table 2 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8068. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8068 circuit is plugged into a live supply, the input voltage can ring to much higher than its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Table 1. LTM8068 Recommended Component Values and Configuration for Specific V_{OUT1} Voltages (T_A = 25°C)

V_{IN}	V_{OUT1}	C_{IN}	C_{OUT1}	R_{FB1}
3V to 40V	2.5V	2.2µF, 50V, 1206	100µF, 6.3V, 1210	15.4k
3V to 40V	3.3V	2.2µF, 50V, 1206	47µF, 6.3V, 1210	11.8k
3V to 40V	5V	2.2µF, 50V, 1206	22µF, 16V, 1210	8.25k
3V to 37V	8V	2.2µF, 50V, 1206	22µF, 16V, 1210	5.23k
3V to 33V	12V	4.7µF, 50V, 1206	10µF, 50V, 1210	3.48k
3V to 30V	15V	4.7µF, 50V, 1206	4.7µF, 25V, 1210	2.8k
3V to 27V	18V	4.7µF, 50V, 1206	4.7µF, 25V, 1210	2.37k

Note: An input bulk capacitor is required.

APPLICATIONS INFORMATION

Table 2. LTM8068 Recommended Component Values and Configuration for Specific V_{OUT2} Voltages (T_A = 25°C)

V_{IN}	V_{OUT1}	V_{OUT2}	C_{IN}	C_{OUT1}	C_{OUT2}	R_{FB1}	R_{FB2}
3V to 40V	1.7V	1.2V	2.2µF, 50V, 1206	100µF, 6.3V, 1210	10µF, 6.3V, 1206	20.5k	open
3V to 40V	2V	1.5V	2.2µF, 50V, 1206	100µF, 6.3V, 1210	10µF, 6.3V, 1206	18.2k	2.32M
3V to 40V	2.4V	1.8V	2.2µF, 50V, 1206	100µF, 6.3V, 1210	10µF, 6.3V, 1206	15.8k	1.07M
3V to 40V	3.1V	2.5V	2.2µF, 50V, 1206	100µF, 6.3V, 1210	10µF, 6.3V, 1206	12.7k	487k
3V to 40V	3.9V	3.3V	2.2µF, 50V, 1206	47µF, 6.3V, 1210	10µF, 6.3V, 1206	10.5k	294k
3V to 38V	5.6V	5V	2.2µF, 50V, 1206	22µF, 16V, 1210	10µF, 6.3V, 1206	7.32k	162k
3V to 36V	8.6V	8V	2.2µF, 50V, 1206	22µF, 16V, 1210	10µF, 10V, 1206	4.89k	88.7k
3V to 32V	12.7V	12V	4.7µF, 50V, 1206	10µF, 50V, 1210	22µF, 16V, 1206	3.32k	56.2k
3V to 29V	15.8V	15V	4.7µF, 50V, 1206	4.7µF, 25V, 1210	22µF, 16V, 1206	2.67k	44.2k
3V to 26V	18.8V	18V	4.7µF, 50V, 1206	4.7µF, 25V, 1210	22µF, 25V, 1206	2.26k	36.5k

Note: An input bulk capacitor is required.

Isolation, Working Voltage and Safety Compliance

The LTM8068 isolation is 100% hi-pot tested by tying all of the primary pins together, all of the secondary pins together and subjecting the two resultant circuits to a high voltage differential for one second. This establishes the isolation voltage rating of the LTM8068 component.

The isolation rating of the LTM8068 is not the same as the working or operational voltage that the application will experience. This is subject to the application's power source, operating conditions, the industry where the end product is used and other factors that dictate design requirements such as the gap between copper planes, traces and component pins on the printed circuit board, as well as the type of connector that may be used. To maximize the allowable working voltage, the LTM8068 has two columns of solder balls removed to facilitate the printed circuit board design. The ball to ball pitch is 1.27mm, and the typical ball diameter is 0.75mm. Accounting for the missing columns and the ball diameter, the printed circuit board may be designed for a metal-to-metal separation of up to 3.06mm. This may have to be reduced somewhat to allow for tolerances in solder mask or other printed circuit board design rules. For those situations where information about the spacing of LTM8068 internal circuitry is required, the minimum metal to metal separation of the primary and secondary is 1mm.

To reiterate, the manufacturer's isolation voltage rating and the required working or operational voltage are often different numbers. In the case of the LTM8068, the isolation voltage rating is established by 100% hi-pot testing. The working or operational voltage is a function of the end product and its system level specifications. The actual required operational voltage is often smaller than the manufacturer's isolation rating.

The LTM8068 is a UL recognized component under UL 60950, file number E464570. The UL 60950 insulation category of the LTM8068 transformer is Functional. Considering UL 60950 Table 2N and the gap distances stated above, 3.06mm external and 1mm internal, the LTM8068 may be operated with up to 250V working voltage in a pollution degree 2 environment. The actual working voltage, insulation category, pollution degree and other critical parameters for the specific end application depend upon the actual environmental, application and safety compliance requirements. It is therefore up to the user to perform a safety and compliance review to ensure that the LTM8068 is suitable for the intended application.

V_{OUT2} Post Regulator

V_{OUT2} is produced by a high performance low dropout 300mA regulator. At full load, its dropout is less than 430mV. Its output is set by applying a resistor from the R_{FB2} pin to GND; the value of R_{FB2} can be calculated by the equation:

$$R_{FB2} = \frac{608.78}{V_{OUT2} - 1.22}\ k\Omega$$

APPLICATIONS INFORMATION

V_{OUT2} Post Regulator Bypass Capacitance and Low Noise Performance

The V_{OUT2} linear regulator may be used with the addition of a 0.01µF bypass capacitor from V_{OUT} to the BYP pin to lower output voltage noise. A good quality low leakage capacitor, such as a X5R or X7R ceramic, is recommended. This capacitor will bypass the reference of the regulator, lowering the output voltage noise to as low as $20\mu V_{RMS}$. Using a bypass capacitor has the added benefit of improving transient response.

Safety Rated Capacitors

Some applications require safety rated capacitors, which are high voltage capacitors that are specifically designed and rated for AC operation and high voltage surges. These capacitors are often certified to safety standards such as UL 60950, IEC 60950 and others. In the case of the LTM8068, a common application of a safety rated capacitor would be to connect it from GND to V_{OUTN}. To provide maximum flexibility, the LTM8068 does not include any components between GND and V_{OUTN}. Any safety capacitors must be added externally.

The specific capacitor and circuit configuration for any application depends upon the safety requirements of the system into which the LTM8068 is being designed. Table 3 provides a list of possible capacitors and their manufacturers. The application of a capacitor from GND to V_{OUTN} may also reduce the high frequency output noise on the output.

Table 3. Safety Rated Capacitors

MANUFACTURER	PART NUMBER	DESCRIPTION
Murata Electronics	GA343DR7GD472KW01L	4700pF, 250V AC, X7R, 4.5mm × 3.2mm Capacitor
Johanson Dielectrics	302R29W471KV3E-****-SC	470pF, 250V AC, X7R, 4.5mm × 2mm Capacitor
Syfer Technology	1808JA250102JCTSP	100pF, 250V AC, C0G, 1808 Capacitor

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8068. The LTM8068 is nevertheless a switching power supply, and care must be taken to minimize electrical noise to ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 1 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{FB1} and R_{FB2} resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connections of the LTM8068.
3. Place the C_{OUT1} capacitor as close as possible to V_{OUT1} and V_{OUTN}. Likewise, place the C_{OUT2} capacitor as close as possible to V_{OUT2} and V_{OUTN}.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent or underneath the LTM8068.

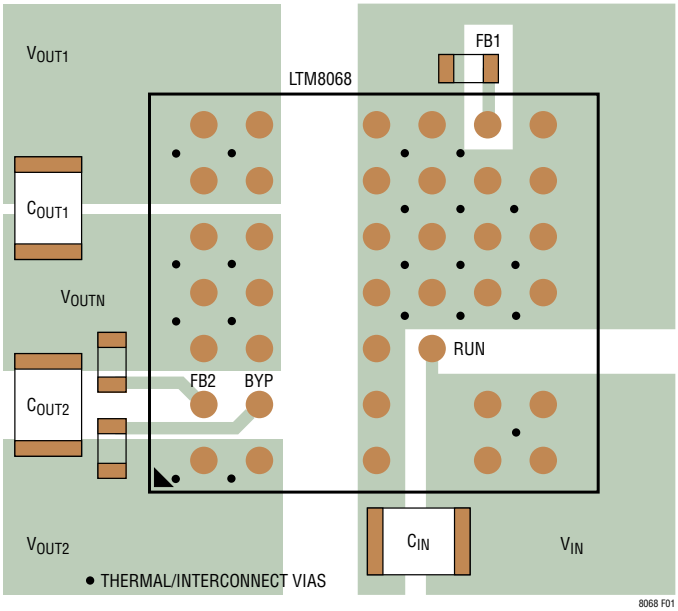


Figure 1. Layout Showing Suggested External Components, Planes and Thermal Vias

APPLICATIONS INFORMATION

5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8068.

6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 1. The LTM8068 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

Minimum Load

Due to the nature of the flyback regulator in general, and the LTM8068 control scheme specifically, the LTM8068 requires a minimum load for proper operation. Otherwise, the output may go out of regulation if the load is too light. The most common way to address this is to place a resistor across the output. The Minimum Load Current vs V_{OUT} Over Full Output Voltage Range graph in the Typical Performance Characteristics section of may be used as a guide in selecting the resistor. Note that this graph describes room temperature operation. If the end application operates at a colder temperature, the minimum load requirement may be higher and the minimum load condition must be characterized for the lowest operating temperature.

If it is impractical to place a resistive load permanently across the output, a resistor and Zener diode may be used instead, as shown in Figure 2. While the minimum load resistor mentioned in the prior paragraph will always draw current while the LTM8068 output is powered, the series resistor-Zener diode combination will only draw current if the output is too high. When using this circuit, take care to ensure that the characteristics of the Zener diode are appropriate for the intended application's temperature range.

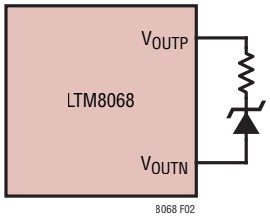


Figure 2. Use a Resistor and Zener Diode to Meet the Minimum Load Requirement

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of the LTM8068. However, these capacitors can cause problems if the LTM8068 is plugged into a live supply (see Analog Devices Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8068 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8068's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8068 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it can be a large component in the circuit.

Thermal Considerations

The LTM8068 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8068 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal

APPLICATIONS INFORMATION

behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration section of the data sheet typically gives four thermal coefficients:

θ_{JA}: Thermal resistance from junction to ambient

$\theta_{JCbottom}$: Thermal resistance from junction to the bottom of the product case

θ_{JCtop}: Thermal resistance from junction to top of the product case

$\theta_{JCboard}$: Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased as follows:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as still air although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule converter, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule converter are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

$\theta_{JCboard}$ is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule converter and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two-sided, two-layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule converter. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 3.

The blue resistances are contained within the µModule converter, and the green are outside.

The die temperature of the LTM8068 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8068. The bulk of the heat flow out of the LTM8068 is through the bottom of the module and the BGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

APPLICATIONS INFORMATION

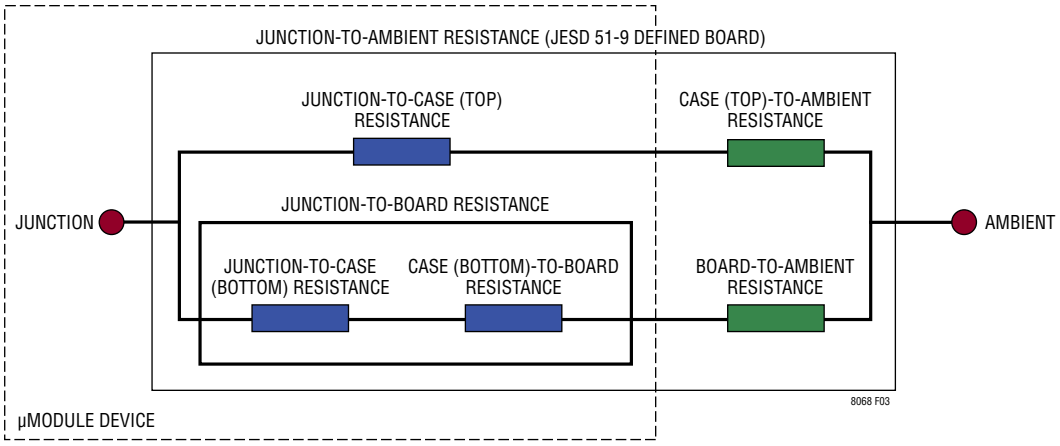
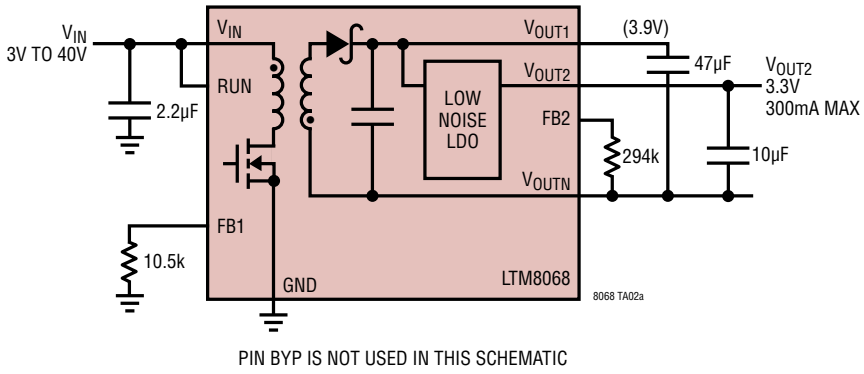


Figure 3. Approximate Thermal Model of LTM8068

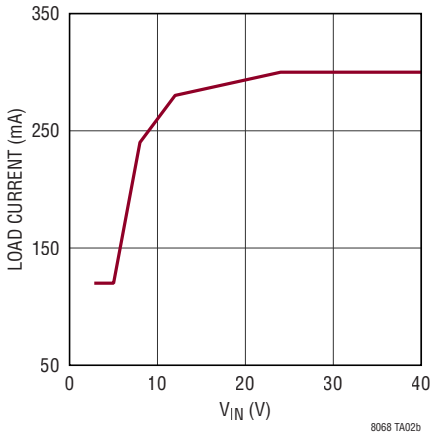
TYPICAL APPLICATIONS

3.3V Flyback Converter

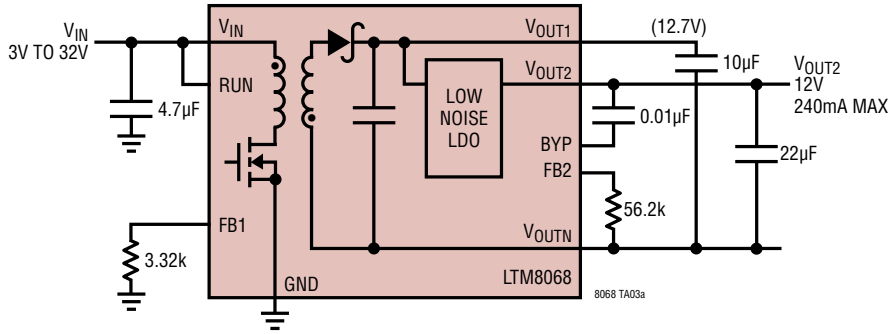


PIN BYP IS NOT USED IN THIS SCHEMATIC

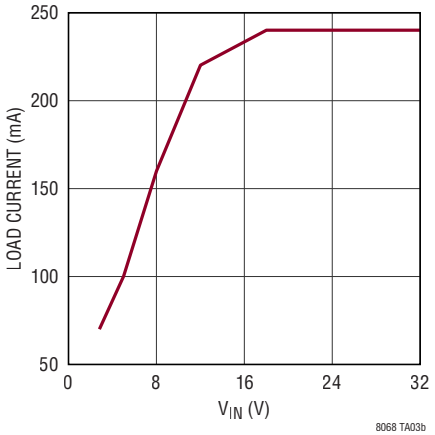
V_{OUT2} Maximum Load Current vs V_{IN}



12V Flyback Converter with Low Noise Bypass



V_{OUT2} Maximum Load Current vs V_{IN}



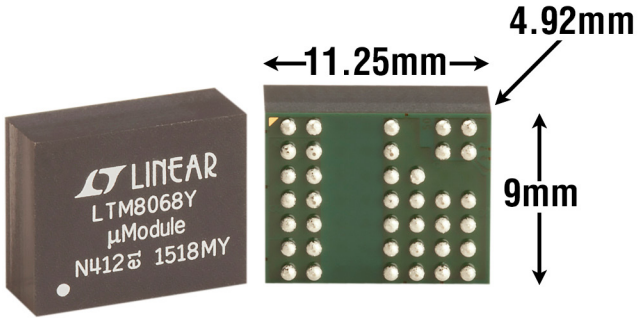
Rev. C

PACKAGE DESCRIPTION

Pin Assignment Table
(Arranged by Pin Number)

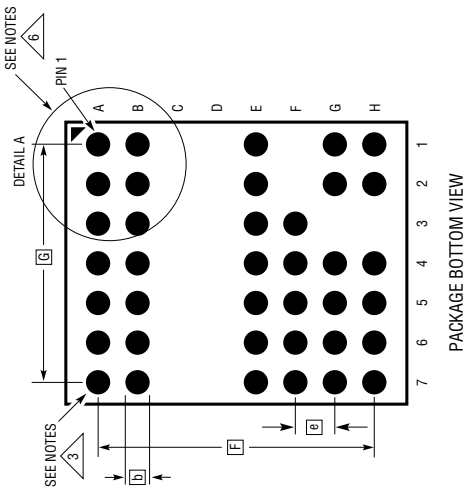
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A1	V_{OUT2}	B1	V_{OUT2}	C1	–	D1	–	E1	GND	F1	–	G1	V_{IN}	H1	V_{IN}
A2	FB2	B2	BYP	C2	–	D2	–	E2	GND	F2	–	G2	V_{IN}	H2	V_{IN}
A3	V_{OUTN}	B3	V_{OUTN}	C3	–	D3	–	E3	GND	F3	RUN	G3	–	H3	–
A4	V_{OUTN}	B4	V_{OUTN}	C4	–	D4	–	E4	GND	F4	GND	G4	GND	H4	GND
A5	V_{OUTN}	B5	V_{OUTN}	C5	–	D5	–	E5	GND	F5	GND	G5	GND	H5	GND
A6	V_{OUT1}	B6	V_{OUT1}	C6	–	D6	–	E6	GND	F6	GND	G6	GND	H6	GND
A7	V_{OUT1}	B7	V_{OUT1}	C7	–	D7	–	E7	GND	F7	GND	G7	FB1	H7	GND

PACKAGE PHOTO



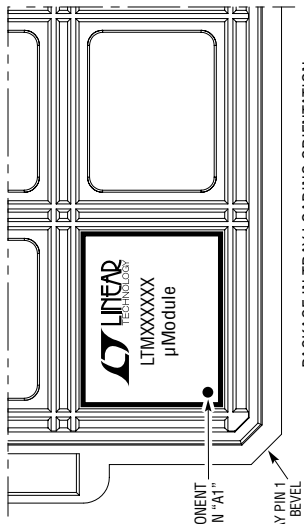
PACKAGE DESCRIPTION

BGA Package
38-Lead (11.25mm × 9.00mm × 4.92mm)
(Reference LTC DWG # 05-08-1925 Rev B)



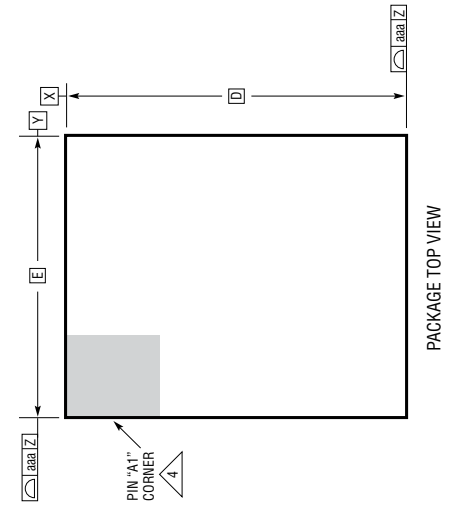
PACKAGE BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

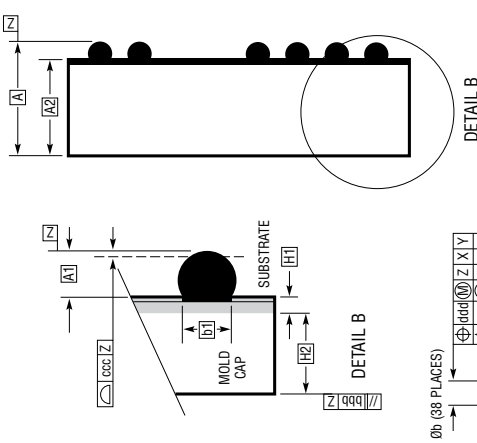


PACKAGE IN TRAY LOADING ORIENTATION

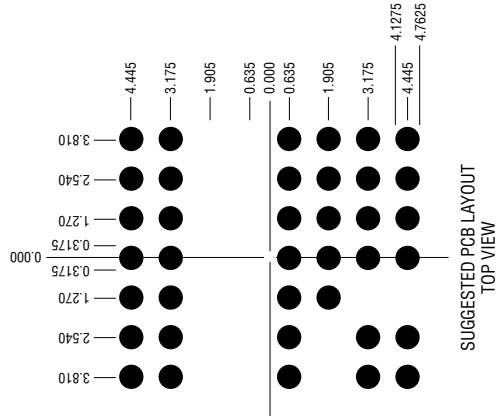
BGA 38 0517 REV B



PACKAGE TOP VIEW



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	BALL HT
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		11.25		
E		9.0		
e		1.27		
F		8.89		
G		7.62		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 38				



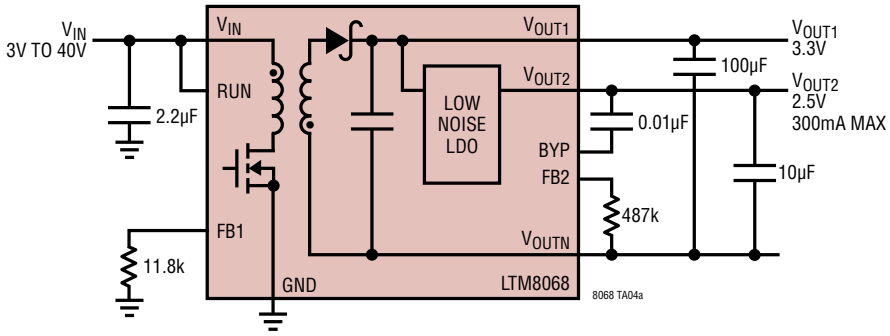
SUGGESTED PCB LAYOUT
TOP VIEW

REVISION HISTORY

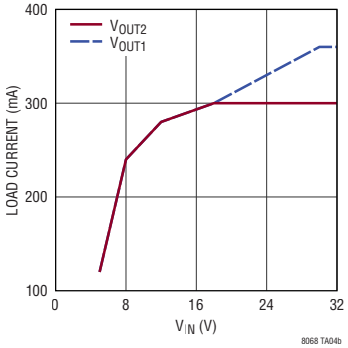
REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/16	Corrected symbol of internal switch on Block Diagram from NPN transistor to N-channel MOSFET	9
B	07/17	Added Minimum Load section	14
C	11/20	Minimum V_{IN} changed from 2.8V to 3V Updated Derating graph Updated text about operating frequency Corrected BGA ball diameter and separation distance in Isolation, Working Voltage and Safety Compliance section	1, 3, 10, 11, 12, 16, 20 6, 7 10 12

TYPICAL APPLICATION

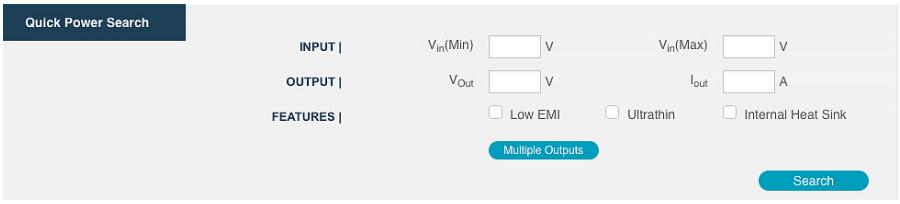
3.3V, 2.5V Dual Output Converter with Low Noise Bypass



Maximum Load Current vs V_{IN}



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

Part Number	Description	Comments
LTM8067	2kVAC Isolated µModule Converter	$3V \le V_{IN} \le 40V$, $2.5V \le V_{OUT} \le 24V$, UL60950 Recognized
LTM8047	725VDC, 1.5W Isolated µModule Converter	$3.1V \le V_{IN} \le 32V$, $2.5V \le V_{OUT} \le 12V$
LTM8048	725VDC, 1.5W Isolated µModule Converter with LDO Post Regulator	$3.1V \le V_{IN} \le 32V$, $1.2V \le V_{OUT} \le 12V$; $20\mu V_{RMS}$ Output Ripple
LTM8045	Inverting or SEPIC µModule DC/DC Converter	$2.8V \le V_{IN} \le 18V$, $2.5V \le V_{OUT} \le 15V$ or $-2.5V \le V_{OUT} \le -15V$, Up to 700mA
LT®8300	Isolated Flyback Converter with $100V_{IN}$, 150V/260mA Power Switch	$6V \le V_{IN} \le 100V$, No Opt-Isolator Required
LT8301	Isolated Flyback Converter with 65V/1.2A Power Switch	$2.7V \le V_{IN} \le 42V$, No Opt-Isolator Required
LT8302	Isolated Flyback Converter with 65V/3.6A Power Switch	$3V \le V_{IN} \le 42V$, No Opt-Isolator Required