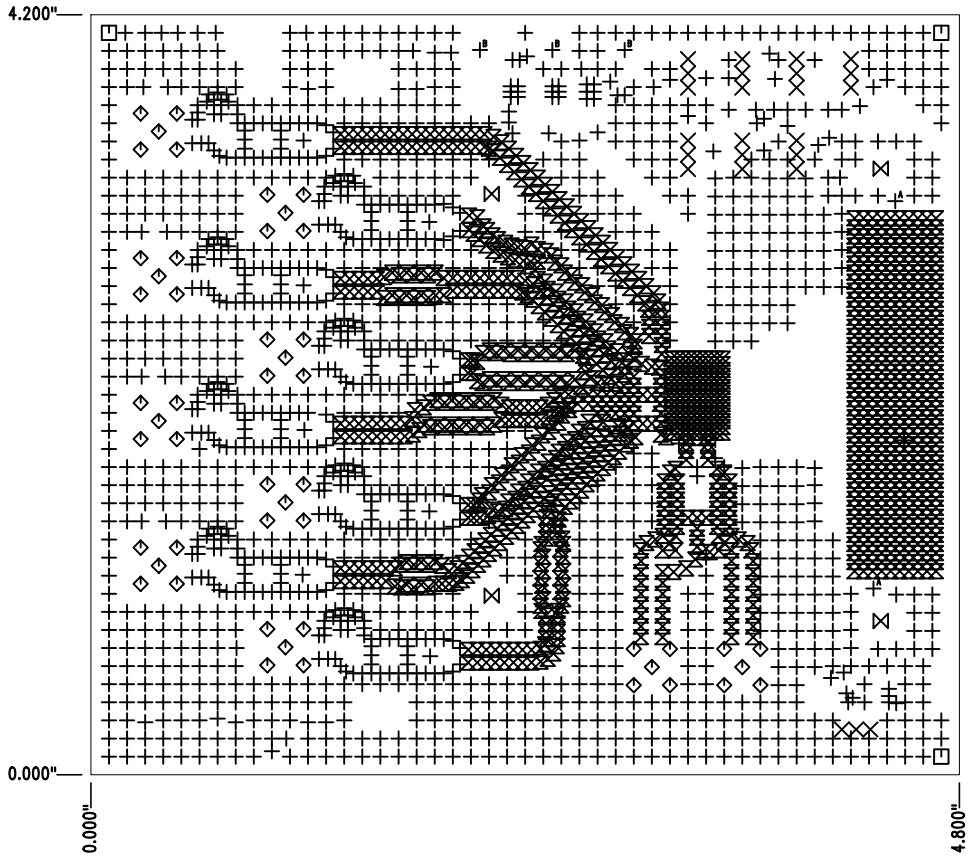
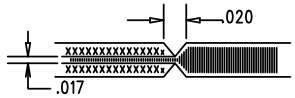
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
–	2	PRODUCTION	CLARENCE M.	03-20-12



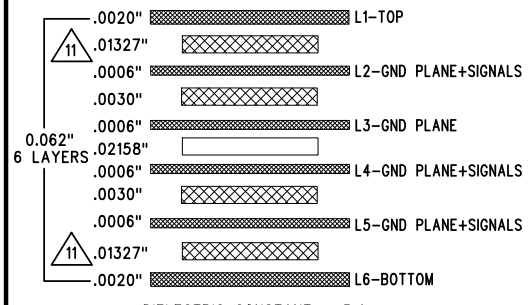
NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC-A-600.
2. MATERIAL: -EPOXY FIBERGLASS, NEMA GRADE FR408, UL 94V-0,
   -FINISHED THICKNESS TO BE 0.062" +/- .005"
   -TOTAL OF 6 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
   -FLAMMABILITY RATING: 94 V-O MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN. 0.00" ARE PRIMARY DATUMS.
4. DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
   -ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
   -HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
5. FINISH: -SMOBC USING LPI BOTH SIDES, COLOR BLACK.
   -GOLD IMMERSION BOTH SIDES.
   -FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
7. PCBS ARE TO BE RoHS COMPLIANT.
8. SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



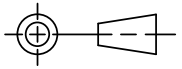
9. DESIGN HAS SOLDER MASK DEFINED PADS ON U1 WITH 0.020" PAD, 0.016" SOLDER MASK, AND 0.015" SOLDER PASTE. DO NOT CHANGE ANY SIZE ON THIS COMPONENT.
10. CONTROLLED 50 OHM +/-10% IMPEDANCE FOR LAYERS 1-3 USING 0.029" TRACES.
    CONTROLLED 50 OHM +/-10% IMPEDANCE FOR LAYERS 6-4 USING 0.030" TRACES.
    CONTROLLED 100 OHM +/-10% IMPEDANCE DIFFERENTIAL PAIRS FOR LAYER 2, 4, AND 5 USING 0.003" TRACES.
11. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.
12. BOARD CONTAINS VIA-IN-PAD TECHNOLOGY. FILL ALL VIAS WITH NON-CONDUCTIVE EPOXY FOLLOWED BY A PLATING CAP TO CREATE A SMOOTH CO-PLANAR SURFACE. NO VISIBLE DIMPLING ALLOWED. VIA PLUGS SHOULD BE COVERED DURING LPI MASK PROCESS.

LAYER STRUCTURE



SIZE	QTY	SYM	PLATED	TOL
10	1469	+	YES	+/-0.003"
35	24	X	YES	+/-0.003"
70	3	□	NO	+/-0.003"
70	50	◇	YES	+/-0.003"
8	1231	⧖	YES	+/-0.003"
120	4	⋈	YES	+/-0.003"
50	2	+A	NO	+/-0.003"
94	3	+B	YES	+/-0.003"

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
0.XX" = ±0.01"
0.XXX" = ±0.005"
INTERPRET DIM AND TOL PER ASME Y14.5M-1994
THIRD ANGLE PROJECTION



APPROVALS	
PCB DES.	KIM T.
APP ENG.	CLARENCE M.

SCALE = NONE

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TITLE: FABRICATION DRAWING

LOW POWER OCTAL-ADC

SIZE	IC NO.	REV
N/A	LTM90XXIY DEMO CIRCUIT 1884A	2

FILENAME: DC1884A-2.PCB | SHT 1 OF 1