

REVISION HISTORY				APPR	DATE
ECO	REV	DESCRIPTION			
-	2	PRODUCTION		CLARENCE M.	02/11/11
<b>LAYER STRUCTURE</b>					
<b>NOTES : UNLESS OTHERWISE SPECIFIED:</b>					
<p>1. FAB PER IPC-A-800. PCB'S ARE TO BE ROHS COMPLIANT.</p> <p>2. MATERIAL: EPOXY FIBERGLASS, NEMA GRADE FR-4.</p> <p>3. SIZE: DIMENSIONS AND TOLERANCES SHOWN.</p> <p>4. DRILLING: DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER. .001 INCH THICK MIN. ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.</p> <p>5. FINISH: SMOBC USING LPI BOTH SIDES COLOR GREEN.</p> <p>6. SILKSCREEN: USING WHITE NON-CONDUCTIVE EPOXY INK.</p> <p>7. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE BUT YOU MAY MODIFY PAD SIZE TO MEET END FINISH.</p> <p>9. CONTROLLED 50 OHM +/-5% IMPEDANCE FOR LAYERS 1 USING 0.03" TRACE.</p> <p>10. OHM FOR DIFFERENTIAL PAIR LAYER 1.3-4.5%@TRACE 3 MILS</p>					
<p> SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.</p> <p>11. BOARD CONTAINS VIA-IN-PAD TECHNOLOGY. FILL ALL 8 MILS VIAS WITH NON-CONDUCTIVE EPOXY FOLLOWED BY A PLATING CAP TO CREATE A SMOOTH CO-PLANAR SURFACE. NO VISIBLE DIMPLING ALLOWED. VIA PLUGS SHOULD BE COVERED DURING LPI MASK PROCESS.</p> <p>12. SCORING FOR PANELIZED PCB:</p>					
<p>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: 0.0XX = +/- 0.01" 0.00XX = +/- 0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION</p> <p><b>LINEAR</b> TECHNOLOGY TITLE: FABRICATION DRAWING SIZE: IC NO. LTM90XXX-Y14 FAMILY N/A DEMO CIRCUIT 1751A REV SCALE = NONE FILENAME: DC1751A-2-PCB</p> <p>1650 MOUNTAIN BLVD MILPITAS, CA 95035 PH: (408) 52-1500 WWW.linear.com INC FOR CUSTOMER USE ONLY</p> <p>LOW POWER OCTAL-ADC</p> <p>1751A 2 SHT 1 OF 1</p>					