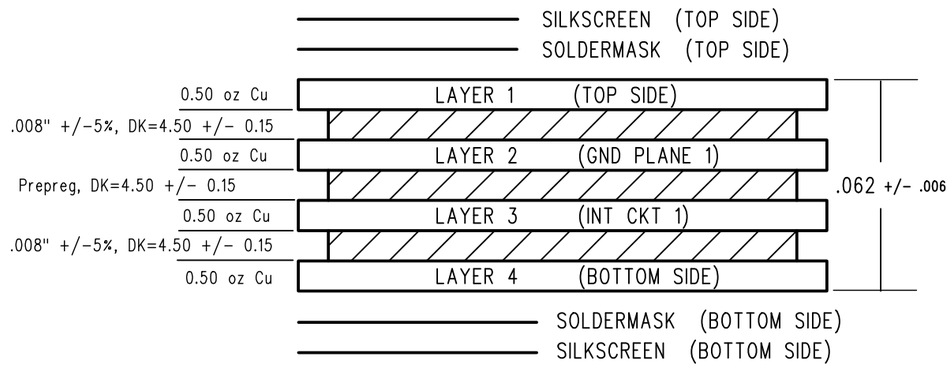
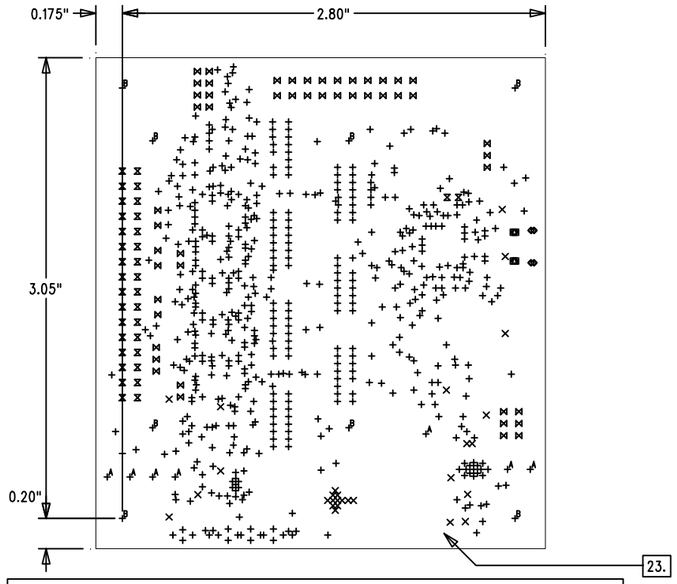
23. MANUFACTURER TO ADD COUNTRY OF ORIGIN IN SILKSCREEN (FARSIDE).
22. INTERPRET DIMENSIONS PER ANSI-Y14.5.
21. CERTIFICATE OF COMPLIANCE TO BE PROVIDED ON ALL SHIPMENTS.
20. EACH LOT MUST INCLUDE ONE SOLDER SAMPLE AND ONE CORE SAMPLE.
19. TEAR DROPPING OF TRACE TO PAD JUNCTION ON ANY LAYER IS PERMITTED PROVIDING MINIMUM METAL-TO-METAL SPACING IS NOT COMPROMISED.
18. THIEVING NOT PERMITTED ON THIS DESIGN.
17. REMOVAL OF INNER SIGNAL LAYER NON-FUNCTIONAL PADS IS PERMITTED.
16. HOLE SIZE: HOLE SIZES GIVEN ARE "FINISHED" HOLE SIZE.
15. ELECTRICAL TEST: FINISHED PCB SHALL BE SUBJECT TO 100% CONTINUITY AND ELECTRICAL ISOLATION (SHORTS AND OPENS) TESTING. TEST FIXTURES TO BE GENERATED FROM PROVIDED IPC-D-356A FORMATTED NET LIST, CROSS-REFERENCED TO GERBER-EXTRACTED NET LIST DATA. THE BOARD MUST BE MARKED WITH A PERMANENT INK STAMP TO INDICATE PASSING THE ELECTRICAL TEST.
14. TRACE IMPEDANCE:
OUTER LAYERS: DIFFERENTAL PAIR: 0.012" TRACES TO BE 90 OHMS +/- 15%.
VENDOR MAY MODIFY TRACES/SPACINGS AS NECESSARY TO ACHIEVE THIS SPECIFICATION
13. PCB STACKUP: THE LAYERS SPECIFIED ON THE CROSS-SECTION FIGURE ARE FOR REFERENCE ONLY. IMPEDANCE IS THE CONTROLLING PARAMETER FOR THE STACKUP. USE DUST NETWORKS STACKUP DRAWING IF PROVIDED.
12. PCB TRACES: NOMINAL CONDUCTOR WIDTHS ON FINISHED PCB TO BE WITHIN +/-15% OR 0.001 WHICHEVER IS LESS OF ARTWORK AS DEFINED ON GERBER DATA AND SUPPLIED APERTURE WIDTH.
11. SILKSCREEN: SILKSCREEN LEGEND OVER SOLDER MASK, TOP SIDE. MATERIAL TO BE WHITE ELECTRICALLY NONCONDUCTIVE INK, NO INK TO APPEAR ON COMPONENT PADS, FIDUCIALS, ELECTRICALLY EXPOSED VIAS OR MOUNTING HOLES. MINIMUM TEXT HEIGHT TO BE 0.040 WITH 0.004 STROKE WIDTH. OVERLAP ONTO TENTED HOLES IS ALLOWED. USE ROHS-COMPLIANT MATERIAL.
10. MARKINGS: DATE CODE AND UL RECOGNIZED VENDOR MARK TO BE ETCHED ON SECONDARY (SOLDER) SIDE OF PCB. TOPSIDE SILKSCREEN LEGEND "DOM: WW-YY" SHOULD HAVE THE "WW-YY" CHANGED TO THE ACTUAL WEEK # (WW) AND YEAR (YY) THAT THE FAB WAS MANUFACTURED (SAME DATE CODE ETCHED ON SECONDARY SIDE).
9. WARP AND TWIST: NOT TO EXCEED 0.010" / INCH.
8. TOLERANCES: ALL TOLERANCES ARE NONCUMULATIVE. HOLE TO EDGE TOLERANCE SHALL NOT VARY MORE THAN +/-0.010 INCHES. TRACE LINE WIDTH TO BE +/-0.001".
7. SOLDER MASK: ROHS COMPLIANT, LPI SOLDER MASK PER IPC-SM-840C, OVER BARE COPPER (SMOBC) BOTH SIDES. REGISTRATION TO BE WITHIN +/-0.002 OF THE ASSOCIATED CIRCUIT LAYER, WITH NO MASK APPEARING ON PADS. PRESENCE OF SOLDER MASK RESIDUE SCRATCHES, AND/OR CONTAMINATION WHICH IMPAIR CONTACT PERFORMANCE ARE CONSIDERED MAJOR DEFECTS, AND CAUSE FOR LOT REJECTION. COLOR: GREEN.
6. ANNULAR RING: 0.002 DIA MIN FOR EXTERNAL LAYERS, 0.001 DIA MIN FOR INTERNAL LAYERS.
5. FINISH: GOLD IMMERSION, 2-5 MICRO INCHES (ROHS COMPLIANT).
4. PLATING: 0.50 OZ COPPER ON 2 OUTER LAYERS, 0.50 OZ COPPER ON 2 INNER LAYERS. SEE STACKUP DRAWING.
3. THICKNESS: 0.062 +/- .006 (FINISHED).
2. MATERIAL: NATURAL EPOXY/GLASS LAMINATES IS410 OR EQUIVALENT ROHS-COMPLIANT MATERIAL. GLASS TRANSITION TEMPERATURE MUST MEET OR EXCEED THAT REQUIRED FOR LEAD-FREE PROCESSING. MATERIAL SHALL BE UL94V-0 FLAMMABILITY RATED. DIELECTRIC CONSTANT TO BE 4.5 +/-5%.
1. FABRICATION: FABRICATION AND ACCEPTANCE TO MEET THE REQUIREMENTS OF IPC-A-600 AND IPC/ANSI-MLL950-C CLASS 2, AOL .25 GENERAL INSPECTION LEVEL II. ACCEPTANCE STAMP NO LARGER THAN 0.25 INCH IS TO BE LOCATED ON THE SOLDER SIDE USING CONTRASTING (WHITE PREFERRED) NONCONDUCTIVE PERMANENT INK.

THE FAB SHALL BE ROHS-COMPLIANT.
NOTE: THE FAB SHALL BE BUILT TO THE SPECIFICATIONS LISTED HERE

LAYUP DETAIL - 4 LAYER





SIZE	QTY	SYM	PLATED	TOL
0.01	613	+	YES	+/-0.003
0.015	28	X	YES	+/-0.003
0.02559 x 0.04134	2	◱	YES	+/-0.003
0.02756 x 0.04724	2	◇	YES	+/-0.003
0.035	34	⧖	YES	+/-0.003
0.04	50	⋈	YES	+/-0.003
0.064	7	+A	YES	+/-0.003
0.125	8	+B	NO	+/-0.003

REVISIONS				
ECO	REV	DESCRIPTION	DATE	APPROVED
1106	1	INITIAL RELEASE	3/13/12	
1121	2	MINOR UPDATES	4/10/12	

RPD ENGINEERING, GRASS VALLEY, CA 95945 530-271-0804	
COMPANY: DUST NETWORKS	DATE: 4/10/12 / P/N: 600-0184
TITLE: GERBERS, INTERFACE BOARD, PITT	
LAYER: DRILL DRAWING	A/W: 610-0184 / REV: 2

SEE ARENA | NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES:
TOLERANCES ARE:
FRACTIONS: DECIMALS: .XX ± .01
ANGLES: 0° 30" .XXX ± .005
MATERIAL - SEE NOTES
FINISH - SEE NOTES
DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN BY: R.P.D.	3-05-12
CHECKED	
ENGRG	
ISSUED	
CONTRACT NO.	

DUST NETWORKS

TITLE: PCB FAB, INTERFACE BOARD, PITT

B	FSCM NO.	DWG NO. 615-0184	REV. 2

SCALE: NONE | SHEET 1 OF 1