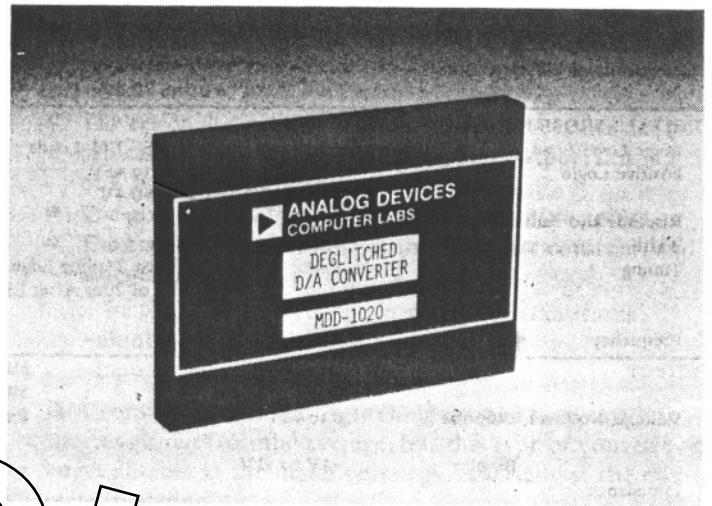


FEATURES

- Ultra-High Speed: 20MHz Word Rate
- 8- and 10-Bit Versions Available
- TTL Compatible
- Smallest Size Available: 3" X 4" X 0.5"
- Completely Self-Contained with Input Register, D/A, Deglitcher, Timing, Internal References, and Output Buffering

APPLICATIONS

- Color-Television Video Reconstruction, Time-Base Correction and Frame Synchronization
- Graphic Displays
- Deflection Systems
- Character Generators
- High Speed D/A Systems



GENERAL DESCRIPTION

The MDD Series is a subsystem module which contains an input digital register, ultra-high speed current output D/A converter, deglitcher, output buffer amplifier, precision references, and timing circuitry within a 3"X4"X0.5" case. The output of the device is an ultra-linear analog representation of the digital input. Requiring only external gain and offset potentiometers for final calibration, the MDD D/A solves the glitch problem associated with high-speed D/A converters. The incorporation of an internal register virtually eliminates the need for input bit time deskewing. While not totally eliminating the glitch per se, the remnant glitch is very small, and more importantly, constant (and therefore filterable) over the output range.

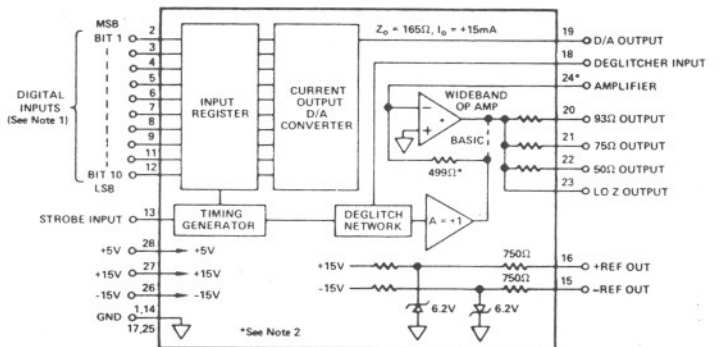
The MDD Series is available with 8- or 10-bit resolution and in two versions. The basic versions contain a unity gain output buffer and can deliver 2V p-p open circuit (or 1V p-p into a load) when the MDD output is both source and load terminated. The "A" versions contain a very high speed output gain amplifier to allow the MDD to deliver 4V p-p open circuit (or 2V p-p into a load) when the device is source and load terminated. Higher output voltages may be obtained—up to ±10V by external feedback resistor selection. However, settling time degradation must be expected.

TV APPLICATION

The "A" version of the MDD Series deglitched D/A is ideally suited for color television video reconstruction. Its output can directly drive the low impedances normally associated with video baseband transmission. Since the output impedance of

the internal operational amplifier is less than 1Ω, the transmission-line match obtained with the internal source terminating resistor is almost perfect. Other applications include waveform generation, automatic test equipment, and fast process control systems.

Designed primarily for PC board mounting, these D/A's may also be plugged into pin sockets. The pins are 0.04" diameter, gold plated, and are on 0.2" centers. For increased reliability, each module is burned in for 96 hours at +25°C before final test and shipment.



NOTES:
 1. INPUTS SHOWN FOR 10-BIT VERSIONS. FOR 8-BIT VERSIONS PINS 11 AND 12 ARE UNUSED.
 2. THESE PARTS (*) ARE OMITTED IN BASIC VERSIONS, BUT PRESENT IN "A" VERSIONS.

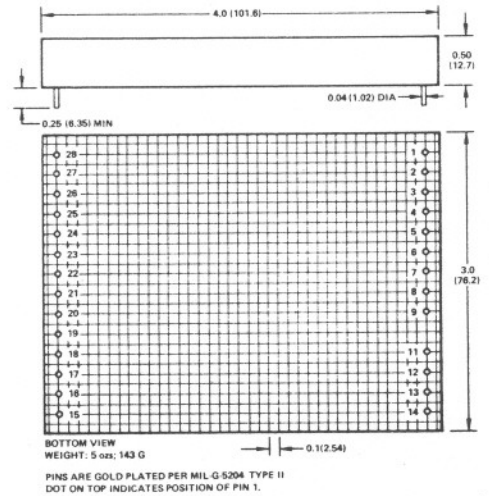
MDD Series Block Diagram

SPECIFICATIONS (typical at +25°C and nominal supply voltages unless otherwise noted)

| MODEL | MDD-0820 MDD-0820A | MDD-1020 MDD-1020A |
|---|--|--|
| RESOLUTION | 8 Bits | 10 Bits |
| Accuracy (including linearity) at Maximum Word Rate of 20MHz | ±0.2% | ±0.05% |
| Monotonicity | Guaranteed 0 to +70°C | |
| DIGITAL DATA BIT INPUTS | 1 Standard "S" TTL Load | |
| Logic Level/Load | "1" = +2.4V to +5V | |
| Positive Logic-Binary (BIN) | "0" = 0V to +0.4V | |
| DIGITAL STROBE INPUT | 2 Standard "S" TTL Loads | |
| Logic Level/Load | "1" = +2.4V to +5V | |
| Positive Logic | "0" = 0V to +0.4V | |
| Risetime and Falltime | 10ns max | |
| Width | 15ns min | |
| Timing | Negative-Going Trailing Edge to Occur a Minimum of 20ns After Last Data Bit Change | |
| Frequency | 20MHz max | |
| OUTPUT | MDD-0820 MDD-1020 | MDD-0820A MDD-1020A |
| Voltage, No Load, Unipolar | 0 to +2V | Externally Programmable with Gain and Offset Resistors to ±10V max |
| Bipolar | +1V to -1V | |
| Impedance | | |
| Pin 22, Low Z | 10Ω max | 15Ω max |
| Pin 22, 50Ω | 30Ω ±5% | 50Ω ±1% |
| Pin 21, 75Ω | 75Ω ±5% | 75Ω ±1% |
| Pin 20, 93Ω | 93Ω ±5% | 93Ω ±1% |
| Amplifier Current | ±50mA for dc load = 100Ω min, dc load = Z _{OUT} + R _{LOAD} | |
| DAC Current | +15mA | |
| SETTLING TIME | | |
| DAC Current Output (to 0.1%) | 15ns | |
| Voltage Output | 50ns to 0.1% 2V p-p | 120ns to 0.1% 4V p-p |
| RESIDUAL GLITCH¹ | 30mV for 2V p-p F.S. Output or 1.5% of F.S. | |
| PEDESTAL | 10mV for 2V p-p F.S. Output or 0.5% of F.S. | |
| OUTPUT ZERO OFFSET | Adjustable to Zero | |
| OUTPUT ZERO OFFSET vs. TEMP | 100ppm/°C | |
| GAIN | Adjustable | |
| REFERENCES AVAILABLE | ±6.2V | |
| POWER REQUIREMENTS | | |
| +15V ±3% | 120mA | |
| -15V ±3% | 150mA | |
| +5V ±5% | 250mA | |
| Power Supply Rejection Ratio | 0.1%/V | |
| CASE | Diallyl Phthalate (per MIL-M-14 type SDG-F) | |
| TEMPERATURE RANGE | | |
| Operating | 0 to +70°C | |
| Storage | -55°C to +85°C | |

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

| PIN | FUNCTION | PIN | FUNCTION |
|-----|--------------------|-----|------------------|
| 1 | GROUND* | 15 | -REF OUT |
| 2 | BIT 1 INPUT (MSB) | 16 | +REF OUT |
| 3 | BIT 2 INPUT | 17 | GROUND* |
| 4 | BIT 3 INPUT | 18 | DEGLITCHER INPUT |
| 5 | BIT 4 INPUT | 19 | D/A OUTPUT |
| 6 | BIT 5 INPUT | 20 | 93Ω OUTPUT |
| 7 | BIT 6 INPUT | 21 | 75Ω OUTPUT |
| 8 | BIT 7 INPUT | 22 | 50Ω OUTPUT |
| 9 | BIT 8 INPUT | 23 | LO Z OUTPUT |
| 10 | NC | 24 | AMP FEEDBACK |
| 11 | BIT 9 INPUT | 25 | GROUND* |
| 12 | BIT 10 INPUT (LSB) | 26 | -15V POWER INPUT |
| 13 | STROBE INPUT | 27 | +15V POWER INPUT |
| 14 | GROUND* | 28 | +5V POWER INPUT |

*ALL GROUNDS INTERNALLY CORRECTED

NOTES

¹ Occurs at the update rate.

Specifications subject to change without notice.

NOTES ON "DEGLITCHING"

An MDD Series D/A converter operating with a full-scale p-p analog output of 1V will typically have a glitch, or transient, in its output which is 15mV in amplitude and is 25ns wide, at the 50% points. These typical values are independent of whether the D/A converter is an 8-bit unit or a 10-bit unit.

This glitch remains constant, regardless of the transition points. In other words, it is the same for the transition from 000000001 to 100000000 as it is for the transition from 100000000 to 100000001 or any other two input words.

A constant glitch is the purpose of the deglitcher circuits. They are intended to hold the area under the curve at a constant value; they are not intended to get rid of all glitches per se.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line; i.e., a single-line spectrum at the sample rate frequency, and harmonics of the sample frequency.

If the glitch is a function of signal dynamics, as it is in the case of a D/A converter output which is not deglitched, a multitude of intermodulation products are formed. Some of

these IM products appear in the video pass-band as spurious signals and increased noise level. The deglitcher circuits effectively eliminate these products. When they do, the S/N ratio approaches that of an ideally-quantized signal, where the rms noise is $Q/\sqrt{12}$, when frequencies above Nyquist are filtered out.

In summary then:

- The residual glitch for an MDD Series D/A converter is typically 15mV for a full-scale 1V p-p output; this is 1.5% of F.S.
- The glitch width is typically 25ns at the 50% points.
- The amplitude and width of the glitch are constant, and independent of:
 - the magnitude of change in successive transitions
 - number of bits of digital output
 - input (update) data rates

D/A converters without deglitching circuits have smaller, shorter glitches, on the average; but this type of converter has larger glitches at the major crossings, especially at the mid-scale transition.

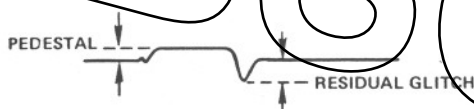


Figure 1. Pedestal/Glitch Relationship

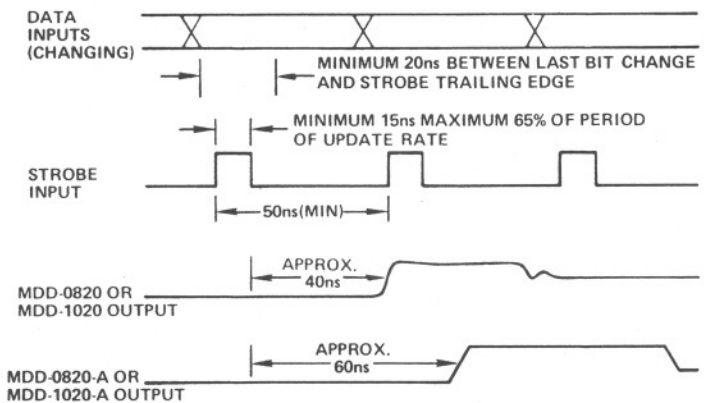


Figure 2. MDD Series Timing Diagram

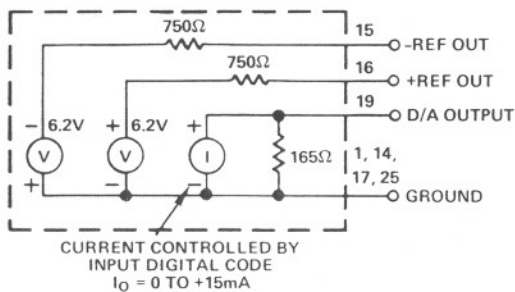


Figure 3. D/A Current Equivalent Circuit

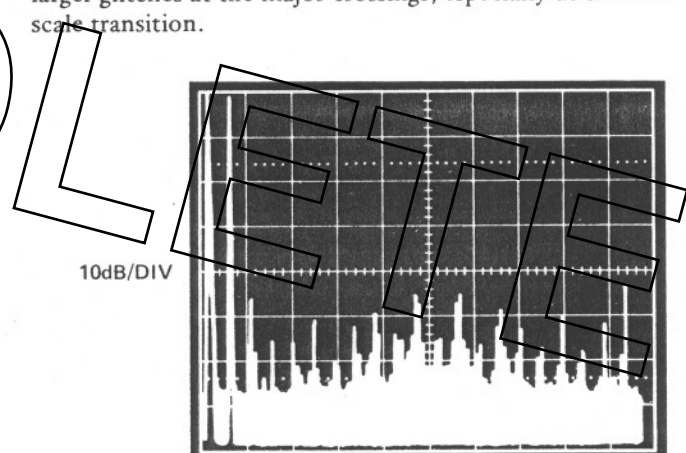


Figure 4. Spectrum of 10-bit D/A Operating at 11MHz Update Rate Without Deglitching - Unfiltered

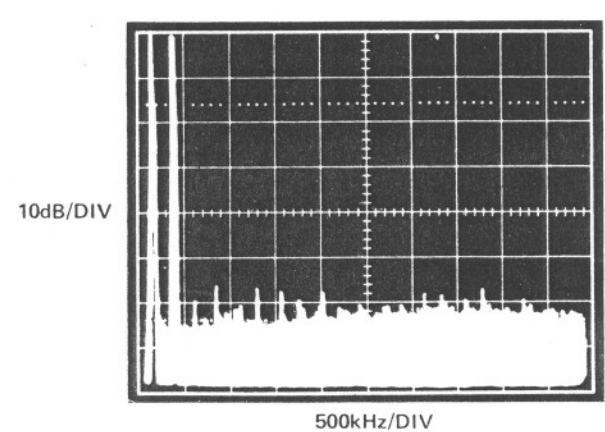


Figure 5. Spectrum of 10-bit D/A Operating at 11MHz Update Rate With Deglitching - Unfiltered

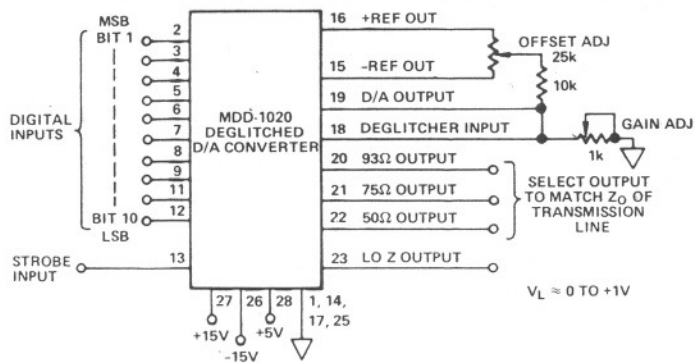
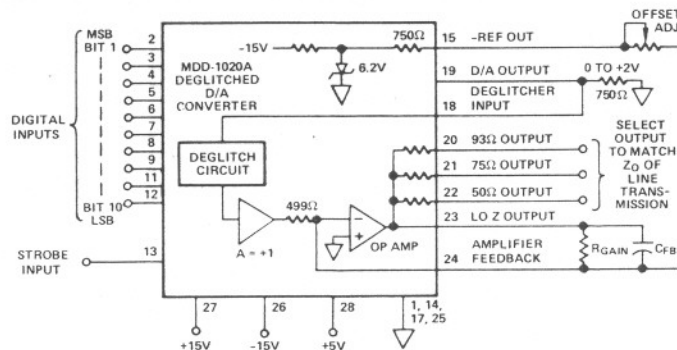


Figure 6. Unipolar Output Configuration Basic Versions



- NOTES:
1. SELECT R_{GAIN} TO GIVE DESIRED OPEN CIRCUIT OUTPUT VOLTAGE. THE INPUT VOLTAGE TO THE OP AMP IS APPROXIMATELY 0 TO +2V. THE OUTPUT OF THE OP AMP IS THEREFORE $(2 \times R_{GAIN})/5000\Omega$ VOLTS P-P.
 2. THE LOGIC IS INVERTED INTERNALLY FOR THE "A" VERSIONS SUCH THAT ALL "1S" AT THE DIGITAL INPUTS YIELDS A FULL-SCALE POSITIVE VOLTAGE AT THE OP AMP OUTPUT.
 3. FOR POSITIVE UNIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY 800Ω, MAKING A 2000Ω POTENTIOMETER IDEAL.
 4. FOR BIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY 2300Ω, MAKING A 5000Ω POTENTIOMETER IDEAL. THE OUTPUT VOLTAGE SHOULD BE ADJUSTED FOR ZERO WITH AN INPUT CODE OF 10 00.
 5. MAKE C_{FB} NOMINALLY 10pF. SELECT FOR OPTIMUM SETTLING TIME IF DESIRED.
 6. IF ADJUSTABLE GAIN IS DESIRED, ADD A LOW-VALUE, LOW-INDUCTANCE CERMET TRIMMING POTENTIOMETER IN SERIES WITH R_{GAIN} . BY PUTTING THE GAIN ADJUSTMENT HERE, THE GAIN AND OFFSET ADJUSTMENTS ARE INDEPENDENT OF EACH OTHER.

Figure 8. Output Configuration - "A" Versions

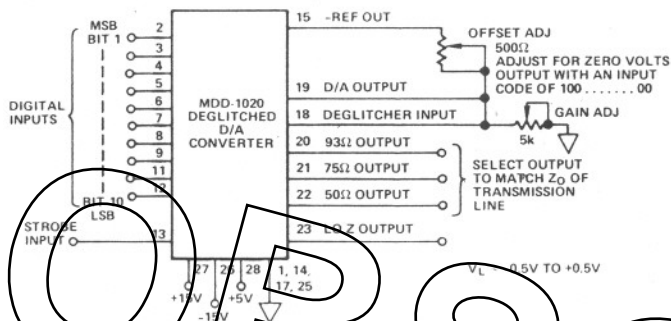


Figure 7. Bipolar Output Configuration Basic Versions

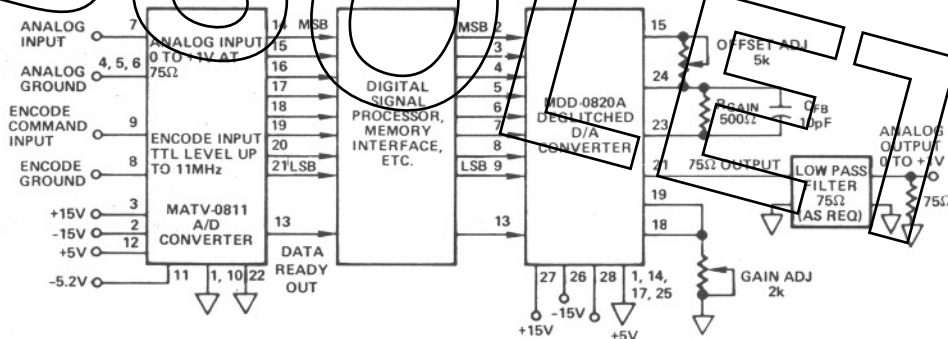


Figure 9. Typical A/D-D/A Back-to-Back Connections for Video Applications or Testing

The typical video differential phase and gain errors (disregarding quantization effects) for the configuration shown are 3° and 3%, respectively, using an encode command frequency of three times the NTSC color subcarrier (10.74MHz). For applications requiring digitization at frequencies of four times NTSC (14.32MHz) or three times PAL (13.29MHz) the MATV-0816 A/D Converter should be substituted. For applications requiring digitization at four times PAL (17.74MHz), the MATV-0820 A/D Converter should be substituted. Results are applicable for either NTSC or PAL test signals using the 20 IRE modulated ramp.

Due to the inherently stable characteristics of the output operational amplifier, the "A" versions are recommended for driving properly terminated video terminated lines.

ORDERING INFORMATION

- | | | |
|--------------------|-----------|--------------------------|
| For 8-Bit Models, | MDD-0820 | without output amplifier |
| Order: | MDD-0820A | with output amplifier |
| For 10-Bit Models, | MDD-1020 | without output amplifier |
| Order: | MDD-1020A | with output amplifier |

Mating pin socket connectors for the MDD Series is model MSB-2. Prototyping socket is MSD-1.

The MDD Series D/A's are normally burned-in at +25°C for a minimum of 96 hours. For extended burn-in, consult the factory. All of Analog Devices' data acquisition products are covered by a one-year warranty.