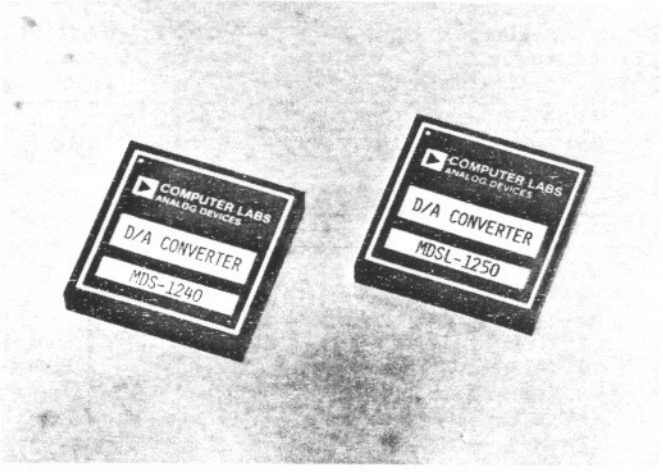
AD9708 ?

ANALOG DEVICES 8-, 10-, 12-Bit Video Speed Current and Voltage Out, D/A Converters

MDS/MDSE/MDSL/MDH SERIES

FEATURES
- Current Settling Times to 15ns
- ±1.5V Compliance
- Voltage Settling Times to 100ns (MDH)
- Monotonicity Guaranteed Over Temperature
- High Output Currents — 15mA
- -30°C to +85°C Operating Range
- Industry Standard Pin Outs
- 20V, p-p Out (MDH)
- TTL or ECL Logic

APPLICATIONS
- CRT Vector Displays
- Digital Waveform Generation
- Automatic Test Equipment
- TV Picture Reconstruction



GENERAL DESCRIPTION

This broad family of digital-to-analog converters represents the "state of the art" in modular, high speed, voltage and current output devices. The family consists of a total of 11 devices in 4 series (MDS, MDSE, MDSL and MDH) that allow the user to make engineering trade-offs between resolution, speed, output and logic type. The first 3 are high compliance current output units which make possible linear output swings greater than ±1.5V. The voltage output MDH series contain a fast settling hybrid operational amplifier which provides ±10V output at ±50mA. To simplify selection these major specifications are summarized in Table 1.

MODEL	BITS	FULL SCALE OUTPUT	FULL SCALE SETTLING TIME	INPUT LOGIC
		(Fastest Settling High Current Out)		
MDS-0815	8	15mA	15ns to 0.4% FS	TTL
MDS-1020	10	15mA	20ns to 0.1% FS	TTL
MDS-1240	12	15mA	40ns to 0.025% FS	TTL
		(MDS with ECL Logic)		
MDS-0815E	8	15mA	15ns to 0.4% FS	ECL
MDS-1020E	10	15mA	20ns to 0.1% FS	ECL
		(Low Current MDS)		
MDSL-0825	8	5mA	25ns to 0.1%	TTL
MDSL-1035	10	5mA	25ns to 0.1%	TTL
MDSL-1250	12	5mA	50ns to 0.025%	TTL
		(Voltage Out MDSL)		
MDH-0870	8	10V/50mA	150ns to 0.4%	TTL
MDH-1001	10	10V/50mA	200ns to 0.1%	TTL
MDH-1202	12	10V/50mA	500ns to 0.025%	TTL

Table 1.

SPEED WITH PRECISION

Analog Devices' model MDS-1240 is the first D/A converter available with highly reliable, internal hybrid construction to achieve ultra-high speed operation. In fact, it is the fastest 12-bit D/A available, settling to 0.025% in 40ns. Hybrid construction eliminates the thermal lag problem inherent in 12-bit D/A's constructed with discrete components. This in turn means that the accuracy is maintained over the total frequency range of operation, yielding superior results for frequency domain applications.

The MDS-1240 is particularly well suited for CRT display applications because of its unsurpassed speed and drive capabilities. The high output current (15mA) allows the use of low impedance loads so that settling times remain short — even with higher output voltage levels. The ability to drive load capacitance is at least 3 times that of other 12-bit D/A's thus providing capability to drive a terminated transmission line directly. The MDS-815 and MDS-1020 provide similar performance at 8 and 10 bits, while the MDS-E units provide it with ECL logic. MDSL-0825, MDSL-1035 and MDSL-1250 also utilize this reliable hybrid construction. The use of laser trimmed resistor networks within the D/A's not only eliminates thermal time lag errors but provide the linearity tempco of 2ppm/°C; guaranteeing monotonic operation over the extended temperature range of -30°C to +85°C. The power dissipation of the MDSL series is one-half that of competitive D/A's, but a full 5mA output current is maintained. This allows driving transmission lines or other low impedance loads directly.

(continued on page 195S)

SPECIFICATIONS (typical @ +25°C unless otherwise specified)

MODEL	UNITS	CURRENT OUTPUT MDS 0815	CURRENT OUTPUT MDS 1020	CURRENT OUTPUT MDS 1240	CURRENT OUTPUT MDS-E (ECL) 0815	CURRENT OUTPUT MDS-E (ECL) 1020
RESOLUTION	Bits	8	10	12	8	10
LSB (Weight)	μA	58.6	14.6	3.66	58.6	14.6
ACCURACY						
Initial (Adjust to 0)	±%FS	0.2	0.05	0.012	0.2	0.05
Linearity (Integral)	LSB max	±1/2	*	*	*	*
Monotonicity		Guaranteed Over Operating Temp Range			*	*
Zero Offset (Adjust to 0)		15nA max	*	*	*	*
TEMPERATURE COEFFICIENTS						
Linearity	ppm/°C	5	*	2	*	2
Gain	ppm/°C	30	*	20	*	*
Offset (Bipolar)	ppm/°C	15	*	*	*	*
STABILITY WITH TIME	±%/yr max	0.5	*	*	*	*
DATA INPUTS						
Logic Compatability		TTL	*	*	ECL	ECL
Logic Voltage Levels						
Bit On Logic "1"	V	+2 to +5.0	*	*	-0.9	-0.9
Bit Off Logic "0"	V	0 to +0.4	*	*	-1.7	-1.7
Logic Current (Each Bit)						
Bit On Logic "1"	μA	≤50	*	*	*	*
Bit Off Logic "0"	mA	-8	*	-5 max	*	*
MSB	mA	N/A	*	-10 max	*	*
Coding		All Units Binary (BIN) for Unipolar, Offset Binary (OBN) for Bipolar			*	*
OUTPUT						
Current Range						
Unipolar	mA	0 to +15	*	*	0 to -15	0 to -15
Bipolar	mA	±7.5	*	*	*	*
Impedance (See Figure 3)	Ω	165	*	200 ±1%	*	*
Compliance (MDH V_{OUT})	V	+1.5, -2	*	*	-1.5, +2	-1.5, +2
Load Resistance for V_{OUT} (See Figure 5)						
0 to +1V	Ω	112	*	100	*	*
±1V	Ω	4.32k	*	750	*	*
INTERNAL REFERENCE VOLTAGE OUT	V	N/A	*	-6.2 ±5%	*	*
SETTLING TIME[2]						
Current	ns to %.	15 to 0.4	20 to 0.10	20 to 0.1 40 to 0.025	*	20 to 0.10
Unipolar Voltage (R_L = 300Ω ‖ 10pF)	ns to %					
Bipolar Voltage (R_L = 2325Ω ‖ 10pF)	ns to %					
POWER REQUIREMENTS						
Range	V	±11 to ±16	*	±14.5 to ±16.5	*	*
Current at Nominal +V	mA max	105	120	55	*	120
Current at Nominal -V	mA max	15	*	20	*	*
POWER SUPPLY REJECTION RATIO	%/V	0.04	*		*	*
+15V	%/V			-0.0001		
-15V (Bipolar)	%/V			-0.002		
-15V (Unipolar)	%/V			-0.2		
TEMPERATURE RANGE						
Operating	°C	-20 to +75	*	-30 to +85	*	*
Storage	°C	-55 to +85	*	-55 to +125	*	*
CASE		Diallyl Phthalate per MIL-M-14 Type SDG-F			*	*
PRICE						
(1–4)	$	115	137	149	129	149

*Specifications same as MDS-0815.

NOTES:

[1] 1ppm/°C for current output. Op amp is 50μV/°C. (See tables in Figures 15, 16 and 17, for overall TC in various configurations.)

[2] For Full Scale Step.

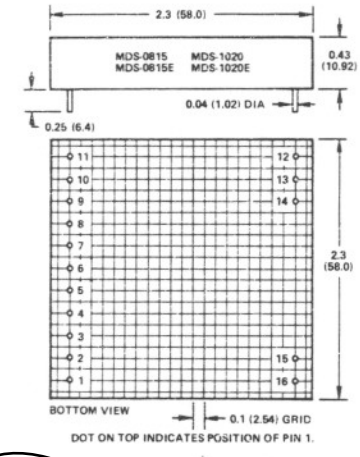
[3] 0 to +5V Out
[4] 0 to +10V Out
[5] ±5V Out
} See Figures 15 and 16 for test circuits.

Specifications subject to change without notice.

CURRENT OUTPUT MDSL			VOLTAGE OUT MDH		
0825	1035	1250	0870	1001	1202
8	10	12	8	10	12
19.6	4.88	1.22	Depends on V_{OUT}		
0.2	0.05	0.012	0.2	0.05	0.012
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	10mV	10mV	10mV
2	2	2	2	2	2
20	20	20	20	20	20
*	*	*	See Note 1		
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
-1.6	-1.6	-1.6	-1.6	-1.6	-1.6
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
0 to +5	0 to +5	0 to +5	±50 max	±50 max	±50 max
±2.5	±2.5	±2.5	±50 max	±50 max	±50 max
600 ±1%	600 ±1%	600 ±1%	0.1 max	0.1 max	0.1 max
*	*	*	±10	±10	±10
300	300	300	N/A	N/A	N/A
2.325k	2.325k	2.325k	N/A	N/A	N/A
-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%
25 to 0.1	25 to 0.1	50 to 0.25	15 to 0.2	25 to 0.10	50 to 0.25
45 to 0.4	70 to 0.1	70 to 0.1	70 to 0.4[3]	100 to 0.1[3]	200 to 0.025[3]
70 to 0.1	80 to 0.05	90 to 0.025	150 to 0.4[4]	200 to 0.1[4]	400 to 0.025[4]
75 to 0.4	100 to 0.1	100 to 0.1	100 to 0.4[5]	130 to 0.1[5]	250 to 0.025[5]
100 to 0.1	110 to 0.05	125 to 0.025			
±12 to ±15	±12 to ±15	±12 to ±15	±14.5 to ±16.5	±14 5 to ±16.5	±14.5 to ±16.5
26	26	26	50	50	50
16	16	16	35	35	35
0.0001	0.0001	0.0001	0.003	0.003	0.003
0.001	0.001	0.001	0.01	0.01	0.01
0.2	0.15	0.15	0.15	0.15	0.15
-30 to +85	-30 to +85	-30 to +85	-30 to +85	-30 to +85	-30 to +85
-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125
*	*	*	*	*	*
112	119	129	204	214	224

MDS-0815, 0815E, 1020, 1020E OUTLINE DIMENSIONS

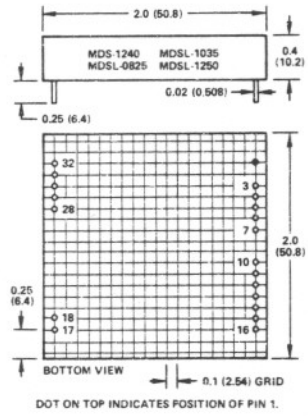
Dimensions shown in inches and (mm).



MATING SOCKET MSB-1 1713

MDS-1240, MDSL-0825, 1035, 1250 OUTLINE DIMENSIONS

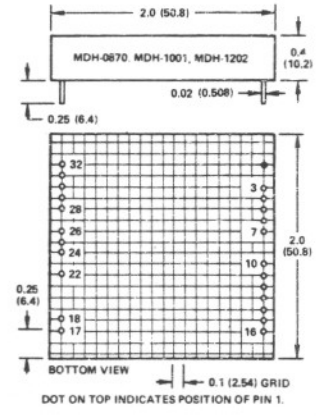
Dimensions shown in inches and (mm).



MATING SOCKET MSA-1

MDH-0870, 1001, 1202 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET MSA-1

PIN DESIGNATIONS MDS-0815E, 1020E

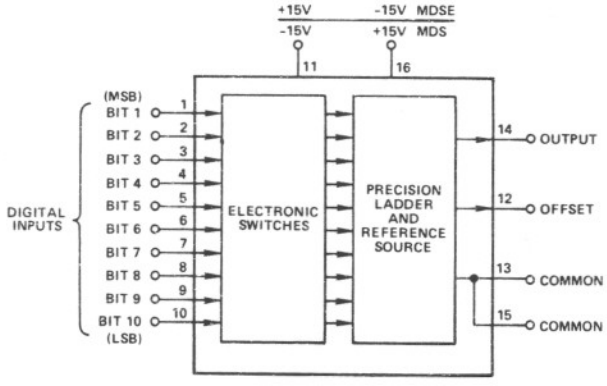
PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	9	BIT 9
2	BIT 2	10	BIT 10
3	BIT 3	11	+15V
4	BIT 4	12	OFFSET
5	BIT 5	13	COMMON
6	BIT 6	14	OUTPUT
7	BIT 7	15	COMMON
8	BIT 8	16	-15V

PIN DESIGNATIONS MDS-0815, MDS-1020

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	9	BIT 9
2	BIT 2	10	BIT 10
3	BIT 3	11	-15V
4	BIT 4	12	OFFSET
5	BIT 5	13	COMMON
6	BIT 6	14	OUTPUT
7	BIT 7	15	COMMON
8	BIT 8	16	+15V

PIN DESIGNATIONS MDS-1240, MDSL-0825, 1035, 1250

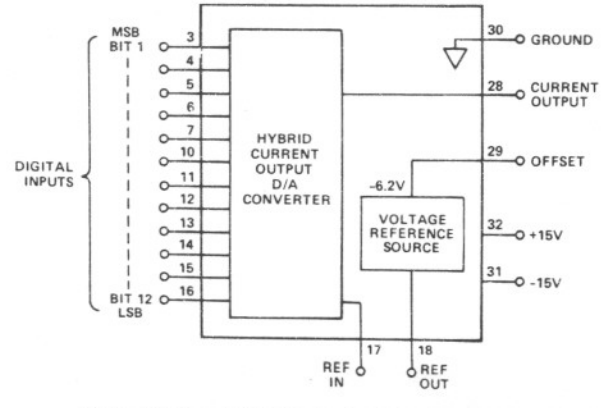
PIN	FUNCTION	PIN	FUNCTION
3	BIT 1 INPUT (MSB)	15	BIT 11 INPUT
4	BIT 2 INPUT	16	BIT 12 INPUT
5	BIT 3 INPUT	17	REFERENCE INPUT
6	BIT 4 INPUT	18	REFERENCE OUTPUT
7	BIT 5 INPUT	28	ANALOG OUTPUT
10	BIT 6 INPUT	29	OFFSET
11	BIT 7 INPUT	30	GROUND
12	BIT 8 INPUT	31	-15V POWER INPUT
13	BIT 9 INPUT	32	+15V POWER INPUT
14	BIT 10 INPUT		



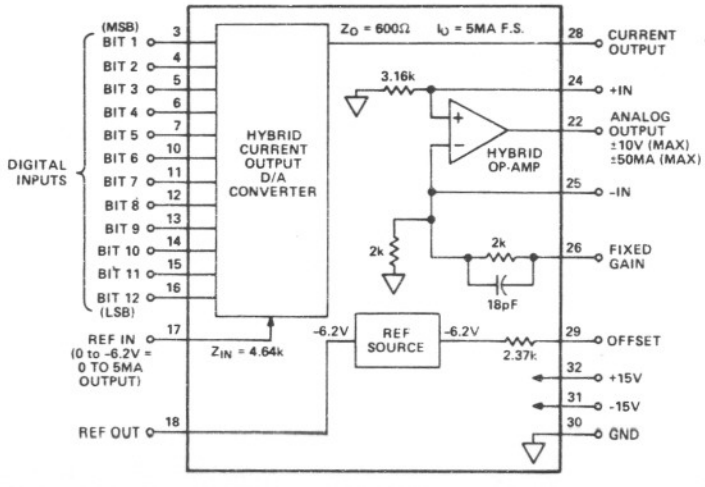
MDS and MDSE Block Diagram

PIN DESIGNATIONS MDH-0870, 1001, 1202

PIN	FUNCTION	PIN	FUNCTION
3	BIT 1 INPUT (MSB)	17	REFERENCE INPUT
4	BIT 2 INPUT	18	REFERENCE OUTPUT
5	BIT 3 INPUT	22	ANALOG OUTPUT
6	BIT 4 INPUT	24	+INPUT
7	BIT 5 INPUT	25	-INPUT
10	BIT 6 INPUT	26	FIXED GAIN
11	BIT 7 INPUT	28	CURRENT OUTPUT
12	BIT 8 INPUT	29	OFFSET
13	BIT 9 INPUT	30	GROUND
14	BIT 10 INPUT	31	-15V POWER INPUT
15	BIT 11 INPUT	32	+15V POWER INPUT
16	BIT 12 INPUT		



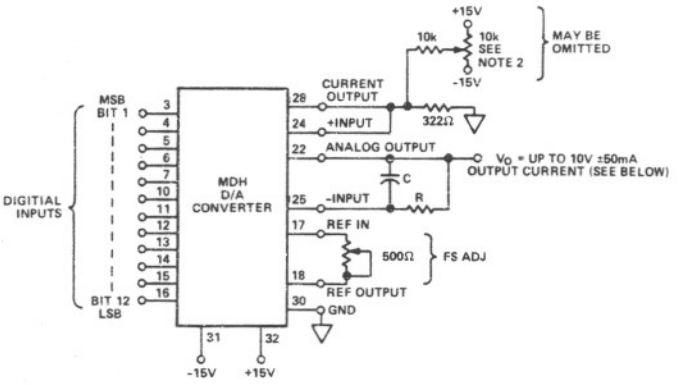
MDS-1240 and MDSL Series Block Diagram



MDH Series Block Diagram

MDH SERIES APPLICATIONS

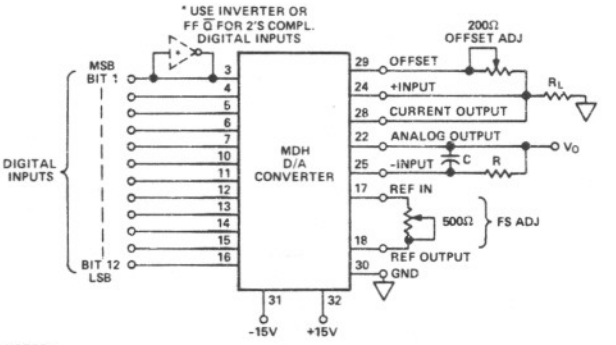
By using external feedback resistor and capacitor as shown in Figures 15 and 16, other full scale output ranges from 2V to 10V may be obtained.



NOTES:
1. VALUE OF C IS APPROXIMATE. A FIXED CAPACITOR WITH TOLERANCE OF ±1pF MAY BE USED IF 50% DEGRADATION OF SETTLING TIME IS PERMITTED. IF SETTLING TIME IS TO BE OPTIMIZED, AN ADJUSTABLE CAPACITOR SHOULD BE USED FOR C AND ADJUSTED FOR MINIMUM SETTLING TIME.
2. OFFSET NULLING MAY BE ACCOMPLISHED BY CONNECTING A 10k POTENTIOMETER BETWEEN +15V AND -15V, AND CONNECTING ITS ADJUSTABLE TAP TO A 10k RESISTOR. THE OTHER END OF THE RESISTOR IS CONNECTED TO PIN 28. TYPICAL UNCOMPENSATED OFFSET IS 1% OF FULL SCALE.

VOLTAGE OUTPUT	SETTLING TIME	OFFSET TEMPCO	R	C
0 to +2V	70ns	100μV/°C	2k	10pF
0 to +5V	100ns	250μV/°C	8k	2pF
0 to +10V	200ns	500μV/°C	18k	0.5pF

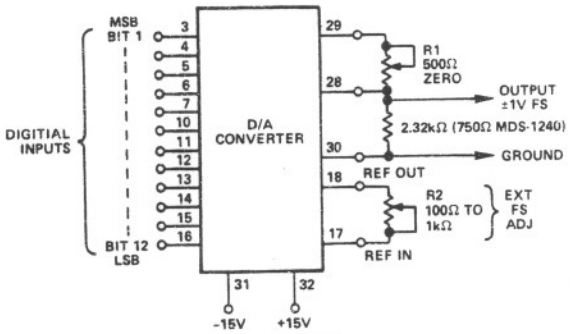
Figure 15. Binary Coding Unipolar Output Configuration



NOTES:
1. The 200Ω POTENTIOMETER IS ADJUSTED FOR AN OUTPUT OF -FS WITH ALL ZEROES IN THE DIGITAL INPUT.
2. THE 500Ω POTENTIOMETER IS ADJUSTED FOR AN OUTPUT OF +FS-1LSB WITH ALL ONE'S IN THE DIGITAL INPUT.
3. FOR TWO'S COMPLEMENT (2SC) OPERATION, AN EXTERNAL INVERTER MUST BE USED TO COMPLEMENT BIT 1 (MSB).
4. AN ADJUSTABLE CAPACITOR MAY BE USED FOR C AND ADJUSTED TO OPTIMIZE SETTLING TIME.

VOLTAGE OUTPUT	SETTLING TIME	OFFSET TEMPCO	R_L	C	R
±1V	70ns	100μV/°C	383	10pF	2k
±2V	100ns	200μV/°C	383	2pF	6k
±5V	100ns	250μV/°C	9.1k	2pF	8k
±10V	200ns	500μV/°C	9.1k	0.5pF	18k

Figure 16. Offset Binary Coding or 2's Comp Coding Bipolar Output Configuration



CALIBRATION PROCEDURE

WITH INPUT CODE 000000000000 ADJUST THE 500Ω (R1) POTENTIOMETER FOR -1.0000 VOLTS OUTPUT. WITH INPUT CODE 111111111111 ADJUST THE 100Ω (R2) POTENTIOMETER FOR +0.99976 VOLTS OUTPUT.

Figure 10. Bipolar Current Output

VOLTAGE OUTPUT
MDS/MDSE-811, 1040

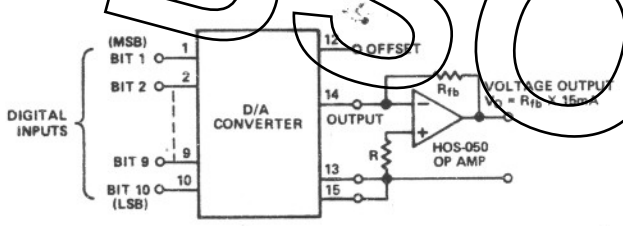
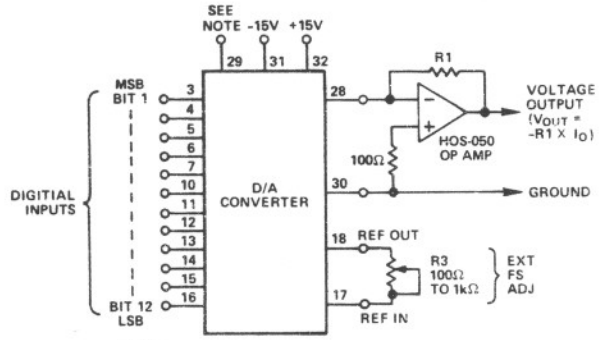


Figure 11. Voltage Output

MDS-1240, MDSL (all)

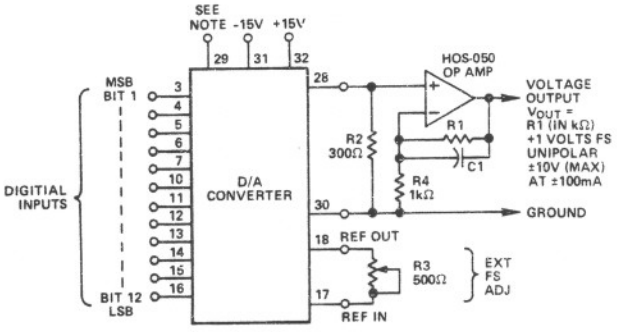


NOTE:

FOR UNIPOLAR VOLTAGE OUTPUT CONNECT JUMPER BETWEEN PINS 29 AND 30. FOR BIPOLAR VOLTAGE OUTPUT CONNECT A 500Ω POTENTIOMETER BETWEEN PINS 28 AND 29 AND ADJUST FOR ZERO OUTPUT WITH 100000000000 INPUT.

Figure 12. Inverting Unipolar or Bipolar Voltage Output

MDSL

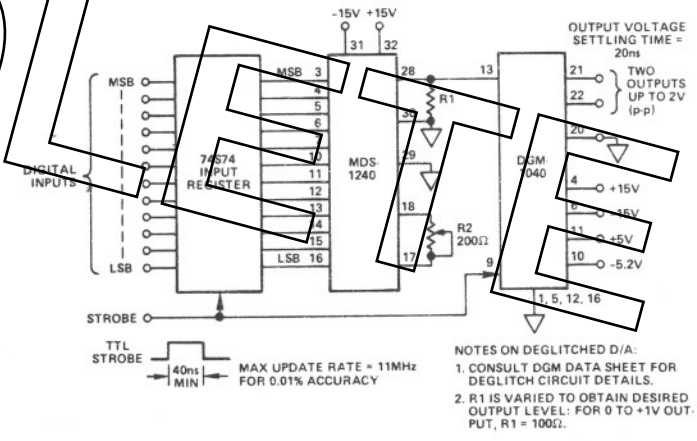


NOTES:

1. CIRCUIT SHOWN FOR UNIPOLAR POSITIVE OUTPUT. OUTPUT SETTLING TIME IS APPROXIMATELY 150ns.
2. FOR 0 TO +10V OUTPUT R2 = 300Ω, R1 = 9kΩ.
3. R3 IS ADJUSTED FOR DESIRED OUTPUT, RANGE IS APPROXIMATELY +5%.
4. FOR BIPOLAR OUTPUT CONNECT 500Ω POTENTIOMETER BETWEEN PINS 29 AND 28 AND UNGROUND PIN 29. R2 IS SET TO 2.32kΩ, AND V_{OUT} (p-p) = 2 (R1 (IN kΩ) +1).
5. C1 IS APPROXIMATELY 10pF AND MAY BE ADJUSTED FOR BEST TRANSIENT RESPONSE.

Figure 13. Noninverting Unipolar or Bipolar Voltage Output

APPLICATIONS



NOTES ON DEGLITCHED D/A:

1. CONSULT DGM DATA SHEET FOR DEGLITCH CIRCUIT DETAILS.
2. R1 IS VARIED TO OBTAIN DESIRED OUTPUT LEVEL: FOR 0 TO +1V OUTPUT, R1 = 100Ω.

Figure 14. Ultra High-Speed Deglitched D/A

ANALOG OUTPUT BIPOLAR, NONINVERTING	OFFSET BINARY	ANALOG OUTPUT UNIPOLAR, NONINVERTING	STRAIGHT BINARY
+FS, -1LSB	111.....1	+FS, -1LSB	111.....1
+1/2 FS	110.....0	+3/4 FS	110.....0
0	100.....0	+1/2 FS	100.....0
-1/2 FS	010.....0	+1/4 FS	010.....0
-FS	000.....0	0	000.....0

Table 2. Input Coding

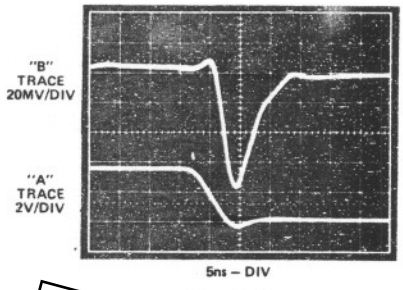


Figure 2.

INTERNAL CURRENT DAC CHARACTERISTICS

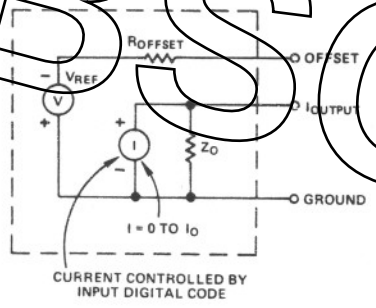


Figure 3. Current Equivalent Circuit

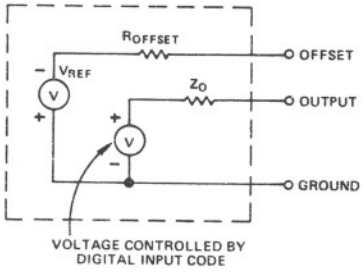


Figure 4. Voltage Equivalent Circuit

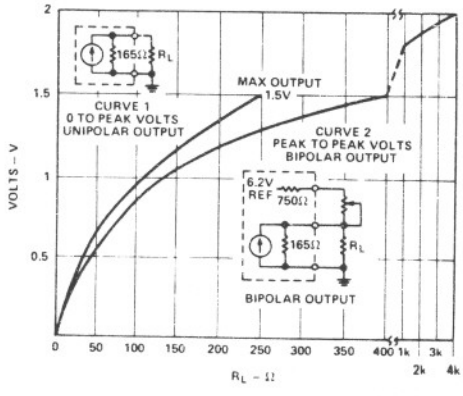


Figure 5. VOUT vs. Load Resistance MDS-0815, -1020

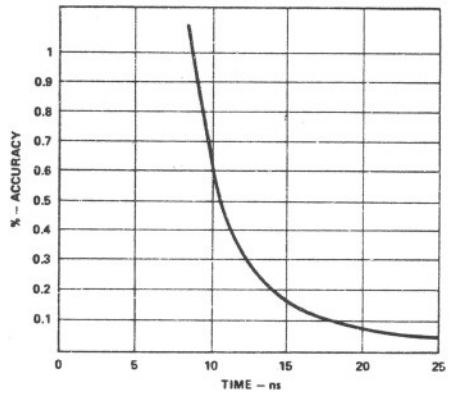


Figure 6. Accuracy vs. Time – MDS and MDSE

BASIC CONNECTIONS AND CALIBRATIONS

MDS/MDSE-0815, 1020

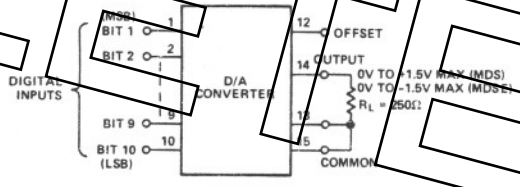


Figure 7. Unipolar Output Current

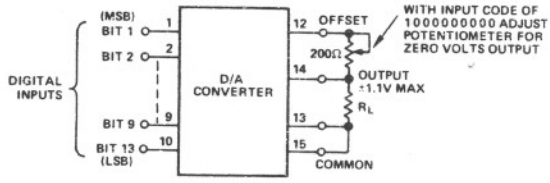


Figure 8. Bipolar Output Current

MDS-1240, MDSL-0825, 1035, 1250

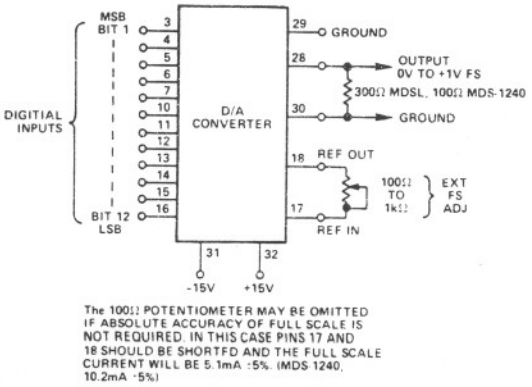


Figure 9. Unipolar Current Output

(continued from page 191S)

Each D/A is housed in industry standard size cases, and each has an internal precision reference. Bipolar operation is achieved by external pin interconnection. In normal circumstances, no external components are required for operation into low impedance loads. Designed primarily for PCB mounting, these D/A's may also be plugged into standard DIL sockets mounted on 1.8″ centers (MDS series 2″ centers).

For ultra-high reliability, this D/A series is optionally available with burn-in extended beyond the Analog Devices standard of 96 hours at +25°C.

NOTES ON FAST-SETTLING D/A CONVERTERS

Invariably, fast-settling D/A converters use current rather than voltage switching.

There are inherent advantages to current-switching converters, since it eliminates an output amplifier. If there is no output amplifier, there is no slew rate limitation which slows settling. The absence of an output amplifier also means there are no overshoot and ringing problems often associated with feedback amplifiers.

The settling time of a current-switching D/A converter, then, is based on:

1. The RC time constant of the converter output.
2. The settling time of the output current change.

If the settling time of the D/A converter under consideration is determined by the RC time constant, the output capacitance and output impedance become very important.

As a typical example in the Analog Devices' D/A converters, output capacitance is 5pF, and nominal output impedance is 165Ω.

For test purposes, the output of these D/A converters are loaded with approximately 150Ω . (There is no "trick" or "gimmick" in loading the output of the converter; it is done to provide an output voltage of approximately 1.0V to 1.2V.) This loading means RC = $80 \times 5 \times 10^{-12}$ = 0.4ns. Since settling time is approximately 7 RC, the overall settling time, if determined by the RC time constant, would be 2.8ns.

Based on this, it becomes obvious the RC time constant of such converters outputs is not the limiting factor in establishing settling time. Instead, the settling time of the converters is based primarily on the settling time of the overall (output) current change, since the effect of the RC time constant is "swamped." Expressed in another way, this means settling time for the MDS series converters is relatively independent of load resistance, unless substantial load capacitance is present. The settling time of the output current, in turn, is based on:

1. The settling time of each switch within the converter.
2. The time skew among the digital inputs which cause the switching action.

Some manufacturers of fast-settling D/A converters spec settling time under the conditions of all digital inputs changing from "0" to "1", or vice versa. At first glance, it would appear this is the "worst case" condition for measuring settling time, since maximum current is being switched.

Unfortunately, this method of specifying neglects an important characteristic of saturated logic . . . the propagation delay for negative-going inputs is different from the delay for positive-going inputs on all forms of saturated logic. The TTL or DTL driving logic, and the D/A input circuits for current-switching D/A's are subject to this same characteristic.

Thus, the time skew of the individual current switches within the converter is worse when one or more input bits are out of phase with the others. This is true even for ideal inputs in which the digital inputs arrive simultaneously; if there is time skew among the bit inputs, of course, the problem becomes more pronounced.

Note, settling times even better than those specified for the MDS series become possible if digital input bit arrivals are deskewed.

These differences among the switches cause a discontinuity or "glitch" in the output. The true "worst case" glitch always occurs at the switching point of the Most Significant Bit or the center point of the output range, because nearly equal and opposite currents are being switched within the converter.

In addition, all "0" to all "1" switching overlooks the practical aspects involved. There are relatively few times when all of the input bits will be changing from one state to the other on successive input changes; however, the MSB will switch out of phase with all other bits each time the analog output of the converter crosses the midpoint.

In considering the choice of a "fast-settling" D/A converter, then, the user should look for the following points in the data sheet:

1. If the settling time spec has all bits changing state identically, it neglects the phenomenon associated with saturated logic discussed earlier.
2. Is the settling time specified with an impractically-low-impedance load?

If the RC time constant of the converter output is the major factor in establishing settling time (because of high output capacitance and/or resistance), a low impedance load helps make settling time look better.

A low impedance load means the voltage being developed at the output is oftentimes too small to be useful.

A higher-impedance load which can develop a useable output of 1.0V or more sometimes negates the fast settling time of the spec sheet.

A test setup for this worst-case measurement is shown in Figure 1. Two pulse generators are used to generate the required out-of-phase pulses, and the delays are adjusted for minimum skew. Figure 2 is an unretouched photo of the oscilloscope trace of an MDS-815 under test.

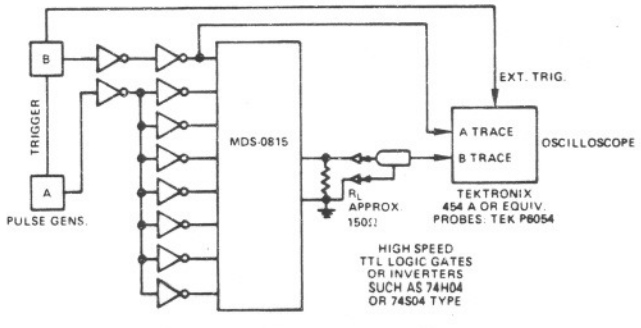


Figure 1.