ANALOG DEVICES

Circuit Note
CN-0174

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Devices Connected/Referenced	
ADF4156	6 GHz Fractional-N PLL
ADF5001	18 GHz Divide-by-4 Prescaler
OP184	Single-Supply, Rail-to-Rail Input/Output Operational Amplifier

Low Noise, 12 GHz, Microwave Fractional-N Phase-Locked Loop (PLL) Using an Active Loop Filter and RF Prescaler

CIRCUIT FUNCTION AND BENEFITS

This circuit is a complete implementation of a low noise microwave fractional-N PLL using the ADF4156 as the core fractional-N PLL device. The ADF5001 external prescaler is used to extend the frequency range of the PLL up to 18 GHz. An ultralow noise OP184 op amp with appropriate biasing and filtering is used to drive a microwave VCO to implement a complete low noise PLL at 12 GHz with a measured integrated phase noise of 0.35 ps rms. This function is typically used to generate the local oscillator frequency (LO) for applications such as microwave point-to-point systems, test and measurement equipment, automotive radar, and military applications.

CIRCUIT DESCRIPTION

A block diagram of the circuit is shown in Figure 1. A 12 GHz VCO from Synergy Microwave Corporation, the DXO11751220-5, was chosen for this circuit, although any VCO operating from 4 GHz to 18 GHz would also work, provided the loop filter is redesigned appropriately. As with the majority of microwave VCOs, the Synergy VCO has a wide input tuning range of 0.5 V to 15 V, which requires an active PLL loop filter to interface between the lower voltage ADF4156 charge pump (maximum output of 5.5 V) and the VCO input.

The OP184 was chosen as the op amp for the active loop filter because of its excellent noise performance, as well as its input

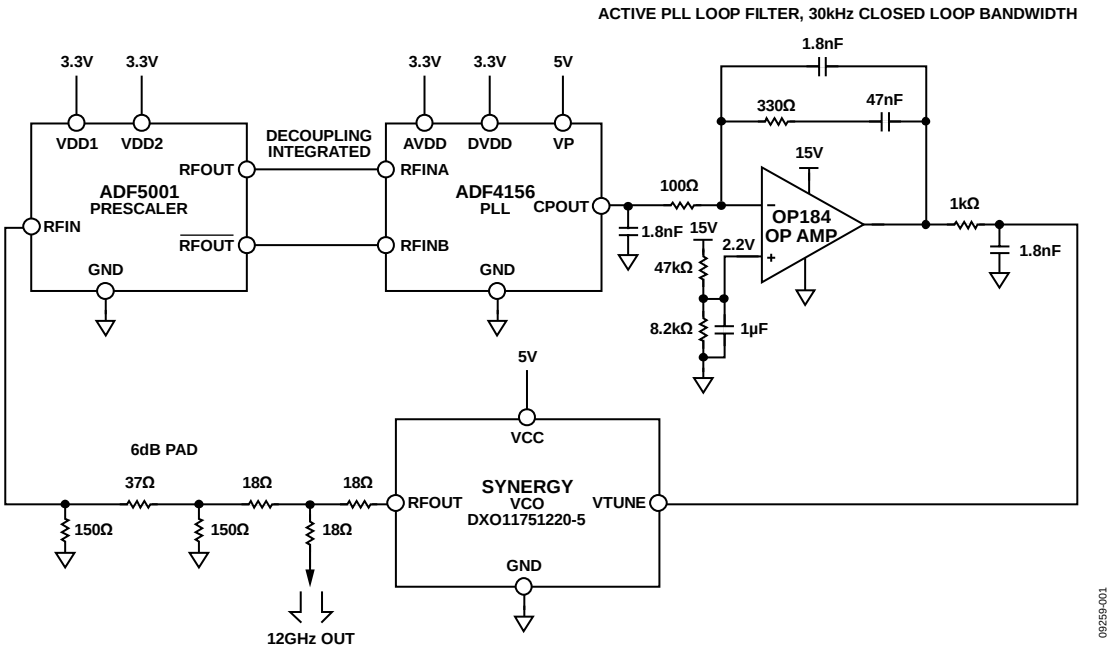

Figure 1. Low Noise Microwave Fractional-N PLL (Simplified Schematic: All Connections and Decoupling Not Shown)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

and output rail-to-rail operation. A low noise op amp is required because the op amp output noise will feed through to the RF output, shaped by the active filter response. Input rail-to-rail operation is also a very important consideration for PLL active filters as it allows the use of a single op amp supply. This is because the charge pump output (CPOUT) will start at 0 V on power-up, which can cause problems for op amps that do not have rail-to-rail input voltage ranges. This also allows the noninverting input of the op amp to be biased at a voltage above ground with built-in margin to any changes in the bias voltage due to resistor mismatch or temperature change.

It is recommended to set the bias voltage level to approximately half the charge pump supply (VP), as this meets both the input voltage range requirements with plenty of margin and gives best charge pump spur performance. Measurements for this circuit note were taken with VP = 5 V and op amp common-mode bias = 2.2 V. To help minimize any reference noise feed-through, a large decoupling capacitor of 1µF was placed close to the noninverting op amp input pin as shown in Figure 1. This capacitor with the 47 kΩ resistor forms an RC filter with a cut-off below 10 Hz.

Loop Filter Design

The PLL loop filter design was done using Analog Devices free simulation tool, ADIsimPLL. This tool allows the design and simulation of several passive and active PLL loop filter topologies and has a library of Analog Devices op amps built in, which include the important op amp specifications such as voltage and current noise, input offset and bias currents, and voltage supply range. The simulation tool accurately predicts PLL closed loop phase noise and is able to model the effect of op amp noise along with the noise of the other PLL loop components. The ADIsimPLL simulation design file for this circuit note can be found at www.analog.com/CN0174_ADIsimPLL.

An inverting topology with pre-filtering was chosen. Pre-filtering is advisable so as not to overdrive the amplifier with the very short current pulses from the charge pump—which could slew rate-limit the input voltage. When using the inverting topology, it is important to make sure that the PLL IC allows the PFD polarity to be inverted, canceling out the op amp's inversion, and driving the VCO with the correct polarity. The ADF4156 PLL has this PD polarity option.

Setup and Measurement

The settings used for the circuit are given in Table 1. Measured results are shown in Figure 2 versus the simulated performance as predicted by ADIsimPLL. As can be seen the results agree quite well. The measured integrated phase noise is 0.35 ps rms. The measurement setup is shown in Figure 3.

Table 1. Test Measurement Settings

Parameter	Value	Unit
RF Frequency	12	GHz
ADF4156 RF input frequency	3	GHz
PLL Loop Filter Bandwidth	30	kHz
Reference Input Frequency	100	MHz
PFD Frequency	25	MHz
Charge Pump Setting	5	mA
PD Polarity Bit	Negative	
Noise Mode	Low Noise	

The performance of this or any high speed circuit is highly dependent on proper PCB layout. This includes, but is not limited to, power supply bypassing, controlled impedance lines (where required), component placement, signal routing, power and ground planes. (See MT-031 Tutorial, MT-101Tutorial, and article, *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, for more detailed information regarding PCB layout.)

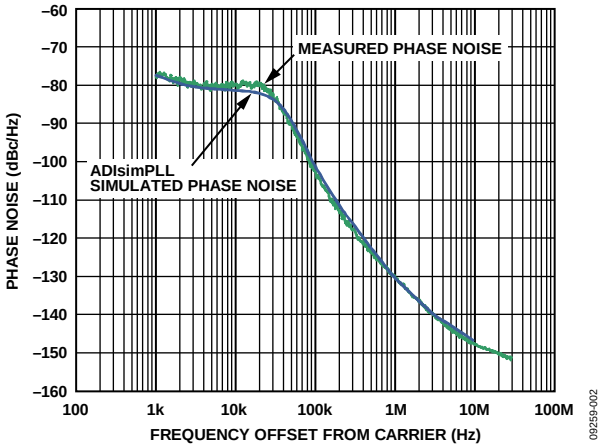

Figure 2. Measured vs. Simulated Phase Noise Performance of the 12 GHz PLL

COMMON VARIATIONS

There are several active loop filter topologies available in ADIsimPLL, using both inverting or non-inverting op amp configurations. The phase noise trade-offs can be investigated in ADIsimPLL. The inverting topology allows you to obtain output voltages as low as the minimum output voltage of the op amp, which can be as low as 125 mV for the OP184. In contrast to the non-inverting topology where the output voltage is limited to the minimum charge pump voltage (0.5 V) multiplied by the non-inverting gain.

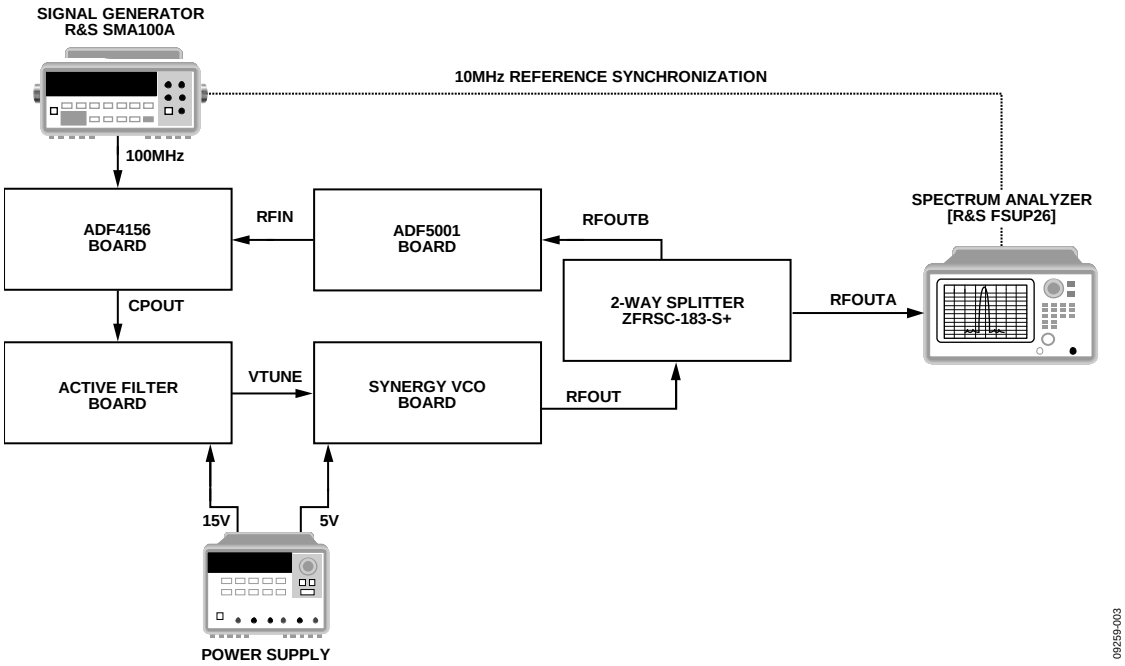

Figure 3. Measurement Circuit

LEARN MORE

ADIsimPLL Design File for CN-0174

ADIsimPLL Design Tool

ADIsimPower Design Tool

Ardizzoni, John. "A Practical Guide to High-Speed Printed-Circuit-Board Layout" *Analog Dialogue*, 39-09, September 2005.

Harney, Austin. "Designing High-Performance Phase-Locked Loops with High voltage VCOs" *Analog Dialogue*, Dec.2009.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-086 Tutorial, *Fundamentals of Phase Locked Loops*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

ADF4156 Data Sheet

ADF4156 Evaluation Board

ADF5001 Data Sheet

ADF5001 Evaluation Board

OP184 Data Sheet

REVISION HISTORY

3/11—Rev. 0 to Rev. A

Changes to Figure 2 2

10/10—Revision 0: Initial Version

CN09259-0-3/11(A)