DESCRIPTION

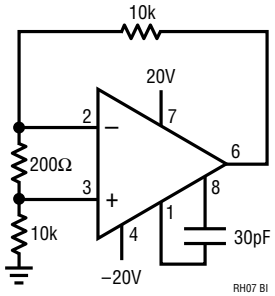
The RH07 is a precision op amp which provides very low offset voltage, low drift and low noise. In the design, processing and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. The wafer lots are processed to LTC's in-house Class S flow to yield circuits usable in stringent military applications.

For complete electrical specifications, performance curves, application notes and applications circuits, see the OP-07 data sheet.

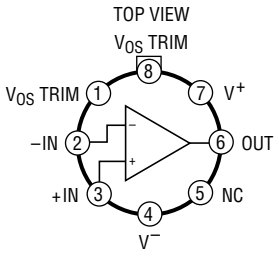
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... ±22V
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

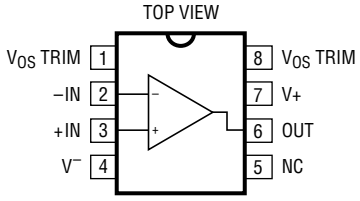
BURN-IN CIRCUIT



PACKAGE INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN



J8 PACKAGE
8-LEAD CERAMIC DIP

TABLE 1: ELECTRICAL CHARACTERISTICS (Pre-Irradiation) (Note 5)

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_A \le 125°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage		1			75	4			200	2,3	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Avg Input Offset Voltage Drift:											
	Without External Trim		3							1.3		µV/°C
	With External Trim	Null Pot = 20kΩ	3							1.3		µV/°C
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability		2,3			1						µV/Mo
I_{OS}	Input Offset Current					2.8	1			5.6	2,3	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Avg Input Bias Current Drift		3							50		pA/°C
I_B	Input Bias Current					±3	1			±6	2,3	nA
$\frac{\Delta I_B}{\Delta Temp}$	Avg Input Bias Current Drift		3							50		pA/°C
e_n	Input Noise Voltage	0.1Hz to 10Hz	3			0.6						μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz	4			18						nV/√Hz
		f_O = 100Hz	3			13						nV/√Hz
		f_O = 1000Hz	3			11						nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz	3			30						pA_{P-P}
	Input Noise Current Density	f_O = 10Hz	3			0.80						pA/√Hz
		f_O = 100Hz	3			0.23						pA/√Hz
		f_O = 1000Hz	3			0.17						pA/√Hz
R_{IN}	Input Resistance:											
	Differential Mode		3	20								MΩ
	Common Mode				200							GΩ
	Input Voltage Range		3	±13.5				±13.5				V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V		110			1	106			2,3	dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V		100			1	94			2,3	dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \ge 2k$, V_O = ±10V		200			4	150			5,6	V/mV
		$R_L \ge 500Ω$, V_O = ±0.5V	3	150								V/mV
		V_S = ±3V										
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 10k$				±12.5	4					
		$R_L \ge 2k$				±12.0	4			±12.0	5,6	
		$R_L \ge 1k$				±10.5	4					
SR	Slew Rate	$R_L \ge 2k$	3	0.1								V/µs
GBW	Closed-Loop Bandwidth	A_{VCL} = 1	3	0.4								MHz
P_D	Power Dissipation	V_S = ±15V				120	1					mW
		V_S = ±3V				6	1					mW

TABLE 1A: ELECTRICAL CHARACTERISTICS (Post-Irradiation) (Note 6)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage		1		90		150		200		250		300	µV
I_{OS}	Input Offset Current				2.8		4		8		12		20	nA
I_B	Input Bias Current				±3		±10		±25		±50		±100	nA
	Input Voltage Range		3	±13.5		±13.5		±13.5		±13.5		±13.5		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V		110		110		105		100		95		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V		100		100		100		95		90		dB
A_{VOL}	Large-Signal Voltage Gain	R_L ≥ 2k, V_O = ±10V		200		200		180		150		120		V/mV
V_{OUT}	Maximum Output Voltage Swing	R_L ≥ 10k		±12.5		±12.5		±12.5		±12.5		±12.5		V
SR	Slew Rate	R_L ≥ 2k		0.1		0.1		0.1		0.075		0.05		V/µs
P_D	Power Dissipation			120		120		120		120		120		mW

Note 1: Offset voltage is measured with high speed test equipment approximately 0.5 seconds after power is applied.

Note 2: Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV.

Note 3: Parameter is guaranteed by design, characterization, or correlation to other tested parameters.

Note 4: 10Hz noise voltage density is sample tested on every lot to an LTPD of 15. Devices 100% tested at 10Hz are available on request.

Note 5: V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

Note 6: T_A = 25°C, V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6
Group A Test Requirements (Method 5005)	1,2,3,4,5,6
Group B and D for Class S, and Group C and D for Class B End Point Electrical Parameters (Method 5005)	1

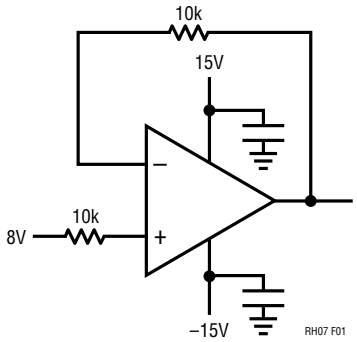
* PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

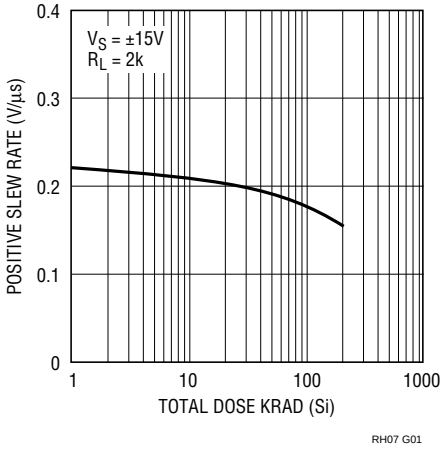
Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CURRENT

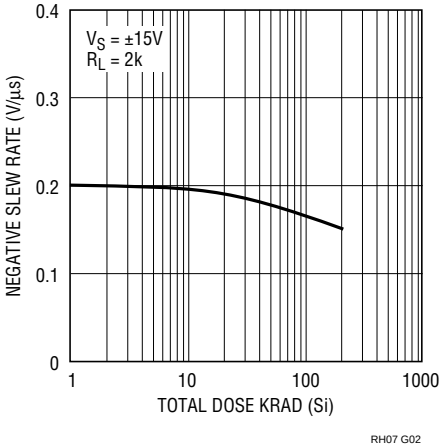


TYPICAL PERFORMANCE CHARACTERISTICS

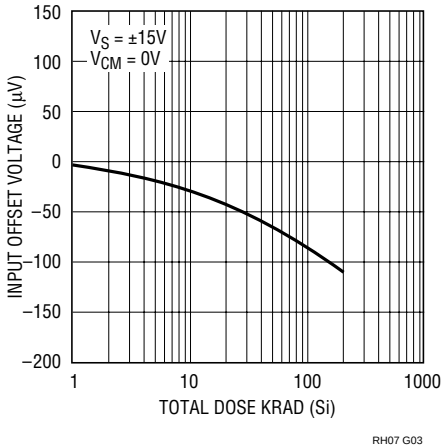
Positive Slew Rate



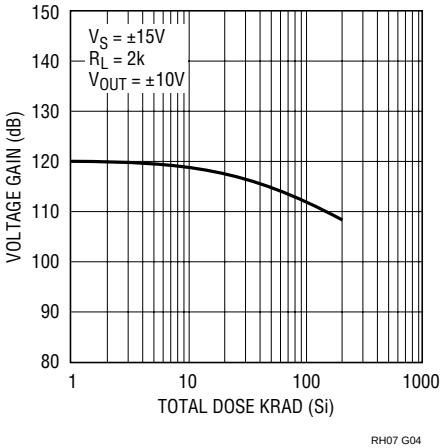
Negative Slew Rate



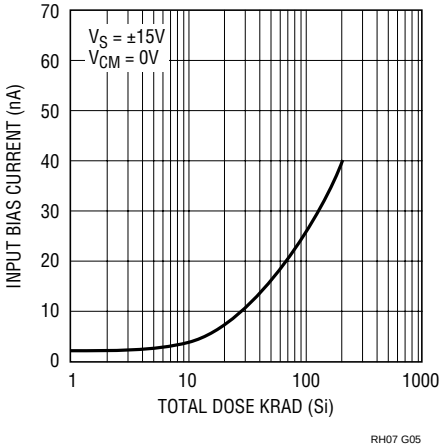
Input Offset Voltage



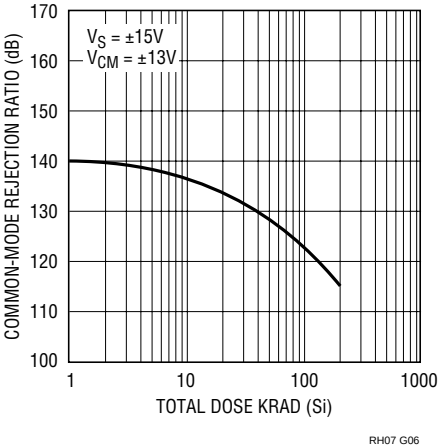
Open-Loop Gain



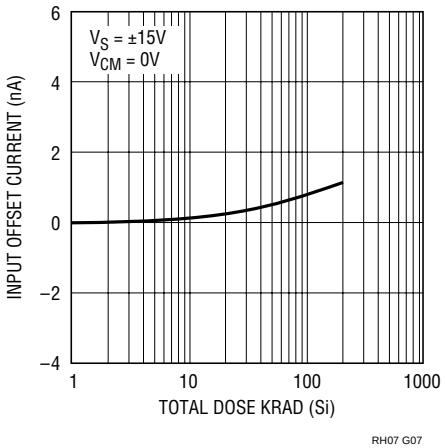
Input Bias Current



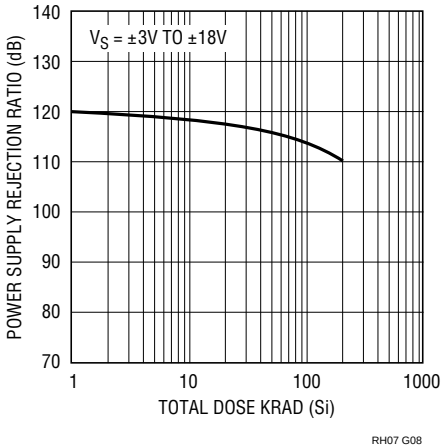
Common-Mode Rejection Ratio



Input Offset Current



Power Supply Rejection Ratio



I.D. No. 66-10-0170

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/LT 0803 REV B • PRINTED IN USA