REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/12/96
A	• PAGE 2, ADDED PARAGRAPHS 3.2.1, 3.2.2, AND 3.2.3. • PAGE 2, PARAGRAPH 3.3.b: ADDED "(SEE PARAGRAPH 3.2)". • PAGE 3, ADDED PARAGRAPHS 3.8.1, 3.8.2, AND 3.8.3. • PAGE 4, PARAGRAPH 3.12: WAFER LOT ACCEPTANCE EXPLANATION WAS REWRITTEN. • PAGE 4, PARAGRAPH 4.4.2, GROUP B INSPECTION WAS REDEFINED. PARAGRAPH 4.4.3, GROUP D INSPECTION WAS REDEFINED. • PAGE 5, PARAGRAPH 4.5.1, SOURCE INSPECTION WAS REDEFINED. • PAGES 6, 7, 8, FIGURES 1, 2, 3 CASE OUTLINES: ADDED θja AND θjc . • UPDATED ENTIRE SPEC TO REVISION A.	10/21/97
B	• PAGE 2, PARAGRAPH 3.2.3, DEVICE OPTION 3, CORRECTED THE PACKAGE TYPE FROM "FLATPACK" TO "FLATPACK, GLASS SEAL". • PAGE 3, PARAGRAPH 3.8.3, DEVICE OPTION 3, CORRECTED THE PACKAGE TYPE FROM "BOTTOM BRAZED FLATPACK" TO FLATPACK, GLASS SEAL" • PAGE 8, CORRECTED PACKAGE TYPE FROM "CERPACK" TO "FLATPACK, GLASS SEAL / 10 LEADS", FIGURE 3, CASE OUTLINE.	11/27/97
C	• PAGE 4, AMENDED PARAGRAPH 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES. • ADDED A SECOND PAGE FOR REVISION RECORD. UPDATE ENTIRE SPEC TO NEXT REVISION DUE TO THE ADDITIONAL PAGE.	03/13/98
D	• PAGE 20, CORRECTED TYPO ON THE MINIMUM ENDPOINT LIMITS FOR +IB, AND -IB, PARAMETERS FROM +1.0 TO –50.	10/01/98
E	• PAGE 7,8,9, FIGURE 1,2,3 CHANGED ΘJA AND ΘJC.	09/28/99

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
INDEX	REVISION	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**
REVISION	PAGE NO.	18	19	20														
INDEX	REVISION	**M**	**M**	**M**														

				ANALOG DEVICES INC.		
	ORIG					
	DSGN			TITLE:		
	ENGR			**MICROCIRCUIT,**		
	MFG			**RH1011, VOLTAGE COMPARATOR**		
	CM					
	QA			SIZE	CAGE CODE	DRAWING NUMBER	REV
	PROG				**64155**	**05-08-5012**	**N**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:		

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
F	• PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, 3.2.3 HAD FIGURES 1, 2, AND 3 REMOVED. • PAGE 4, PARAGRAPH 3.7, CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III" TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER "TABLE II", LINE 2. • PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IIA OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-883". • PAGE 6, PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883'. • PAGE 20, CORRECTED TABLE NUMBER FROM "TABLE II" TO "TABLE III ELECTRICAL TEST REQUIRMENTS".	11/19/99
G	• PAGE 9, CHANGED THETA JA TO θJA=170°C/W AND THETA JC TO θJC=40°C/W FROM θJA=225°C/W AND θJC=18°C/W PER PACKAGE ENGINEER.	9/5/00
H	• PAGE 3: PARAGRAPH 3.2.1 ADDED "OPTION 1", PARAGRAPH 3.2.2, ADDED "OPTION 2", PARAGRAPH 3.2.3, ADDED "OPTION 3". • PAGE 4: PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. TABLE IV REMOVED SUBGROUP 5,6. PARAGRAPH 3.8, CHANGE OPTIONS 1,2,3 STATIC BURN-IN FIGURE 7,9,11. PARAGRAPH 3.9, TABLE II CHANGED TO TABLE III. PARAGRAPH 3.10.3, ADDED "DEVICE OPTIONS 1, 2, AND 3" TO LINE 1. PARAGRAPH 3.11.1 WAS CHANGED FROM "…dosage rate of approximately 20 Rads per second" TO "…dosage rate of less than or equal to 10 Rads per second". • PAGE 5: PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 7 THROUGH 17, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 8: CASE OUTLINE REVISED. LEAD DIMENSION CHANGED FROM .068 TO 0.065. • PAGE 9: CASE OUTLINE UPDATED TO MEET MIL-STD-1835 GUIDELINES. • PAGE 10, MOVED FIGURES TO BETTER FIT THE PAGE. • PAGE 18, CHANGED TABLE 1,2 ELECTRICAL CHARACTERISTICS (PRE & POST IRRADIATION) PER NEW DATA SHEET. • PAGE 20, CHANGED ENDPOINT LIMIT FOR VOS FROM ± 2.0 TO ± 1.5.	9/5/04
J	• PAGE 5, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	3/16/05
K	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 • PAGE 4, PARAGRAPH 3.10.3 ADDED OPTION 3 IS ALLOY 42 FOR FLATPACK	03/05/08
L	• PAGE 4, PARAGRAPH 3.10.3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT. • PAGE 5, PARAGRAPH 3.11.1 CHANGED VERBIAGE.	04/29/08
M	• PAGE 5, PARAGRAPH 4.4.2 CHANGED VERBIAGE. • PAGE 9 FIGURE 3 NOTE 2 ADDED TO LEAD THICKNESS.	06/25/08
N	• **TO CHANGE LINEAR TO ANALOG AND REMOVE SOURCE**	**4/20/21**

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1011 LOW VOLTAGE COMPARATOR, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH1011H (TO5 Metal Can, 8 Leads)

3.2.2 Option 2 – RH1011J8 (Ceramic Dip, 8 Leads)

3.2.3 Option 3 – RH1011W (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage (Pin 8 to Pin 4)	36V
Output to Negative Supply (Pin 7 to Pin 4)	35V
Ground to Negative Supply (Pin 1 to Pin 4)	30V
Differential Input Voltage	±35V
Voltage at Strobe Pin (Pin 6 to Pin 8)	5V
Input Voltage **1/**	EQUAL TO SUPPLIES
Output Short Circuit Duration	10 sec
Operating Temperature Range	-55°C to +125°C
T_{jmax}	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

1/ Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection discussion in the LT1011 data sheet.

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and **Table II.**

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8

3.8.2 Option 2 (Ceramic Dip): Static Burn-In, Figure 9; Dynamic Burn-In, Figure 10

3.8.3 Option 3 (Glass Sealed Flatpack) : Static Burn-In, Figure 11; Dynamic Burn-In, Figure 12

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table II**I herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar and options 2, 3 is alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 13.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1 Group B, Subgroup 2c = 10%

Group B, Subgroup 3 = 10%

Group B, Subgroup 4 = 5%

Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)

Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.5.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.5.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.5.3 Burn-In Variables Data and Deltas (if applicable)

4.5.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.5.5 Generic Group D data (4.4.3 herein)

4.5.6 SEM photographs (3.13 herein)

4.5.7 Wafer Lot Acceptance Report (3.13 herein)

4.5.8 X-Ray Negatives and Radiographic Report

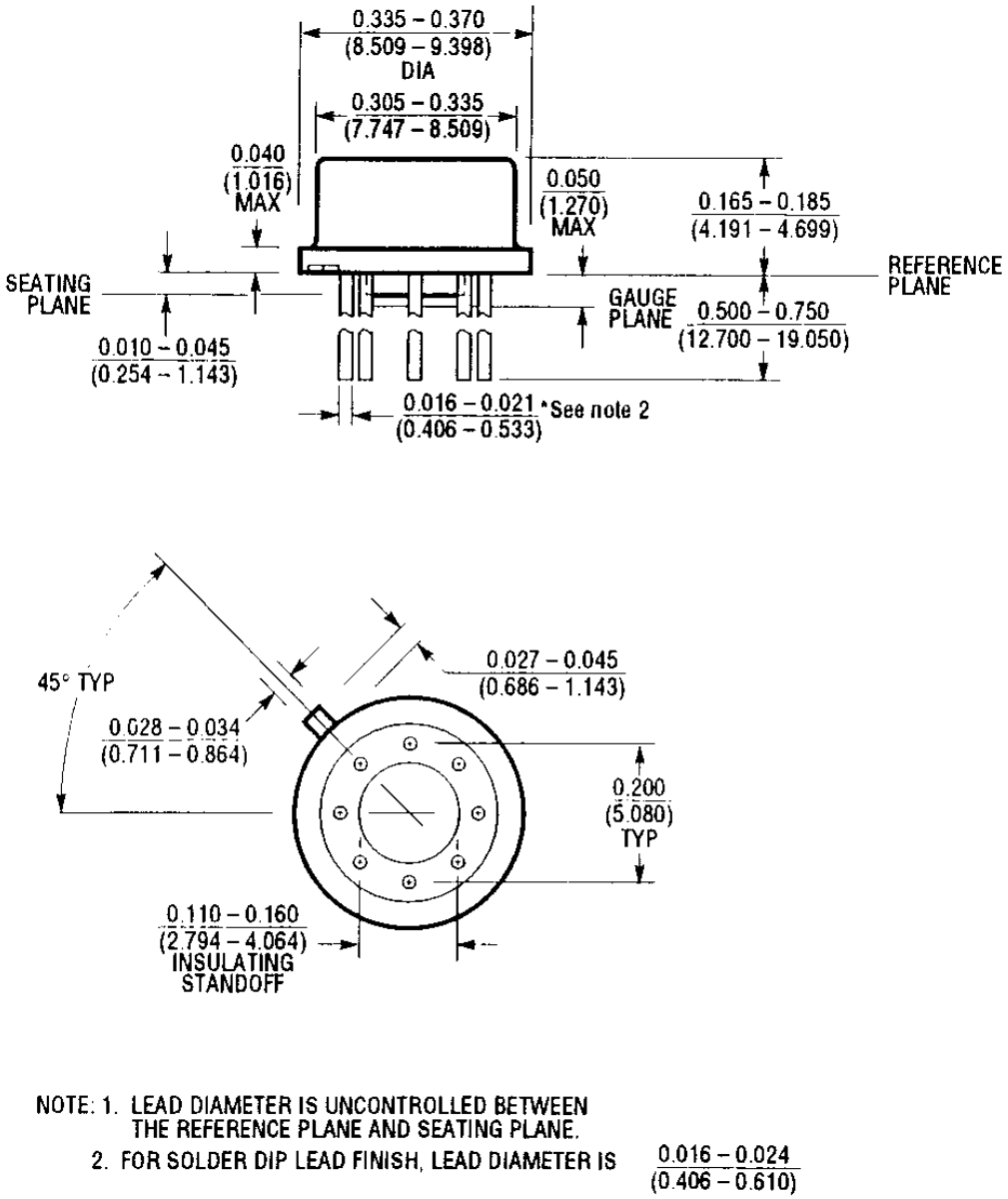
4.5.9 A copy of outside test laboratory radiation report if ordered

4.5.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.5.1 and 4.5.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as “No Charge Data”.

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1
(H) TO5 / 8 LEADS CASE OUTLINE

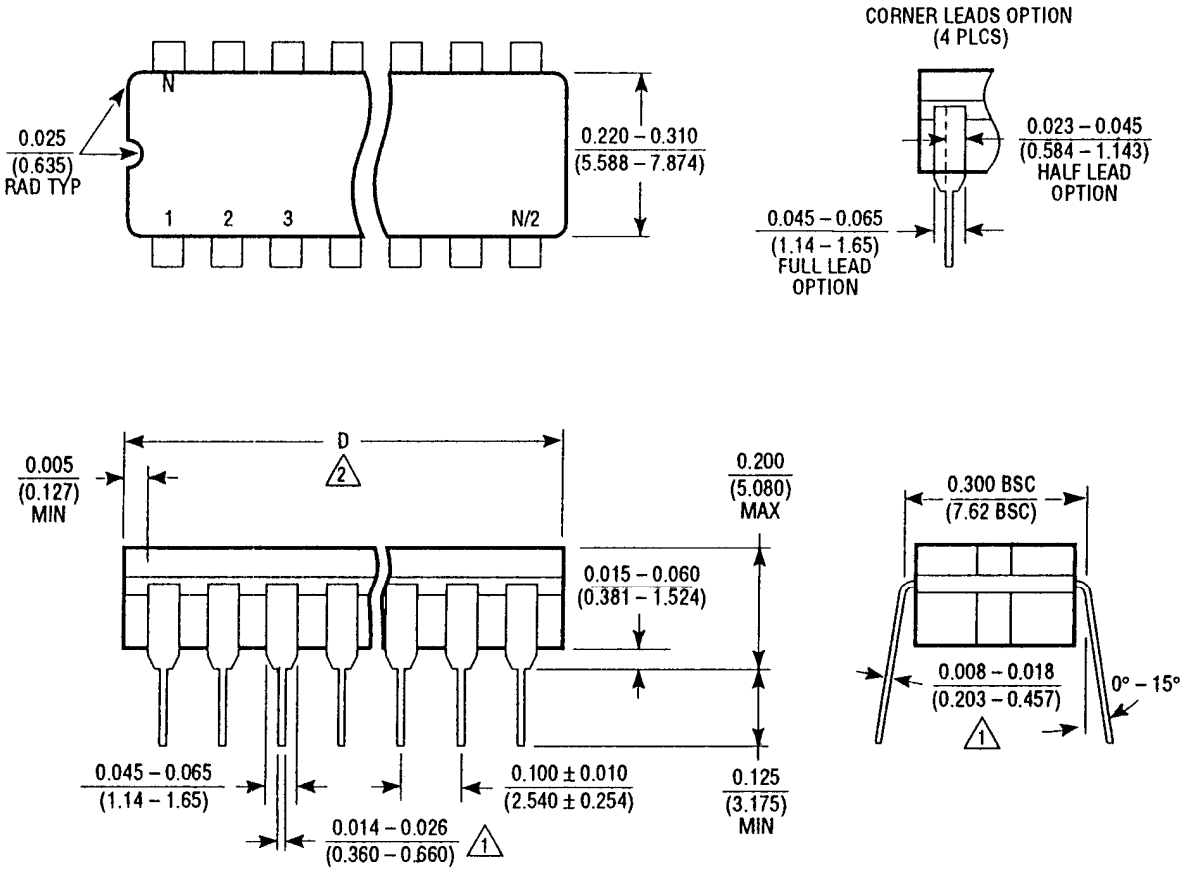


NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

θja = +150°C/W
θjc = +40°C/W

FIGURE 1

DEVICE OPTION # 2
(J8) CERAMIC DIP / 8 LEADS CASE OUTLINE

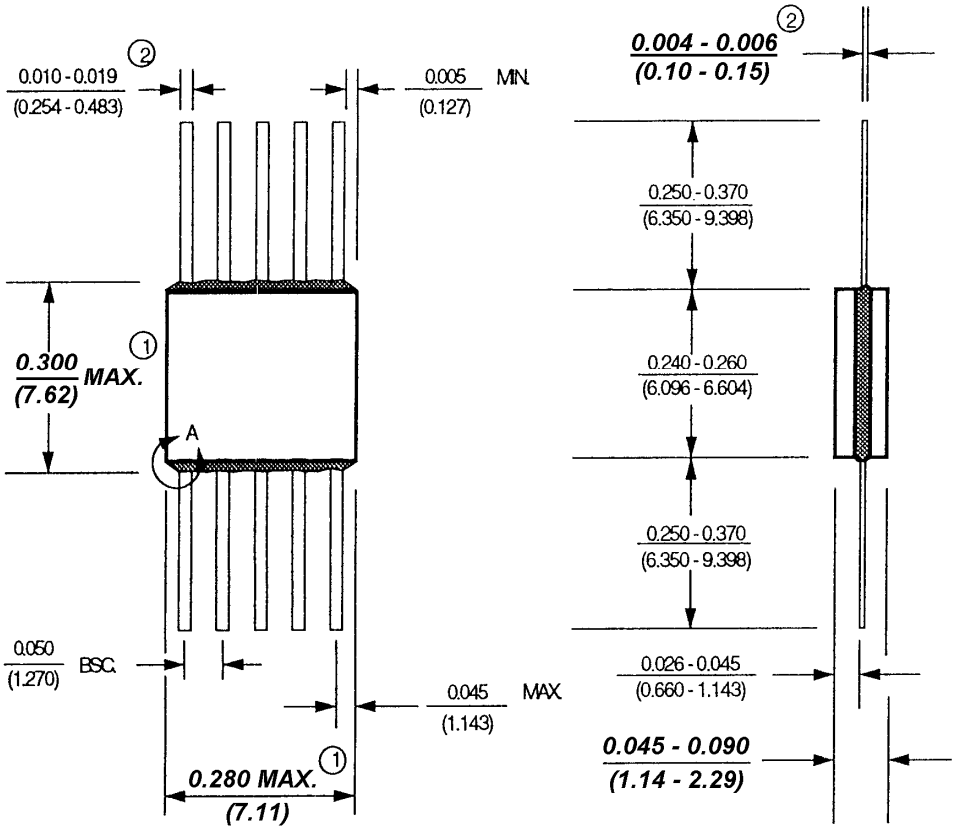


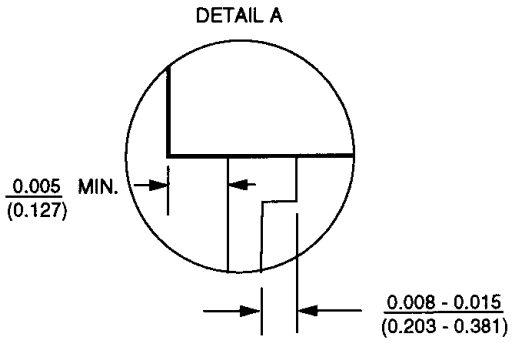
NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
2. 8 LEAD D MAX = .405 (10.287)

θja = +110°C/W
θjc = +30°C/W

FIGURE 2

DEVICE OPTION # 3
(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE





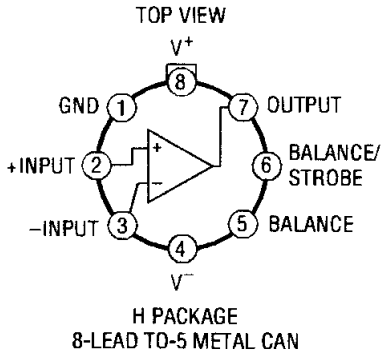
NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

θja = +170°C/W
θjc = +40°C/W

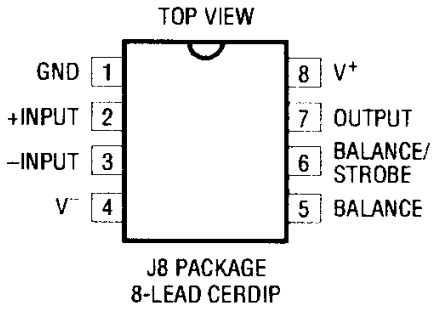
FIGURE 3

TERMINAL CONNECTIONS



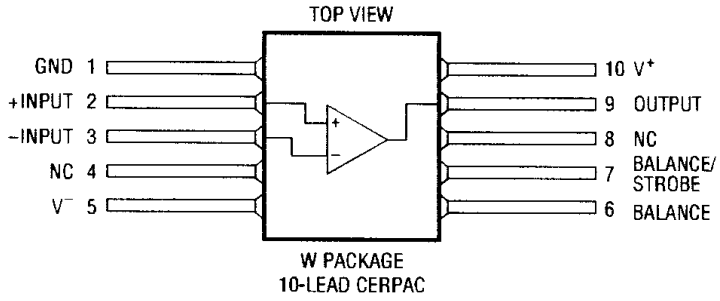
H PACKAGE
8-LEAD TO-5 METAL CAN

FIGURE 4



J8 PACKAGE
8-LEAD CERDIP

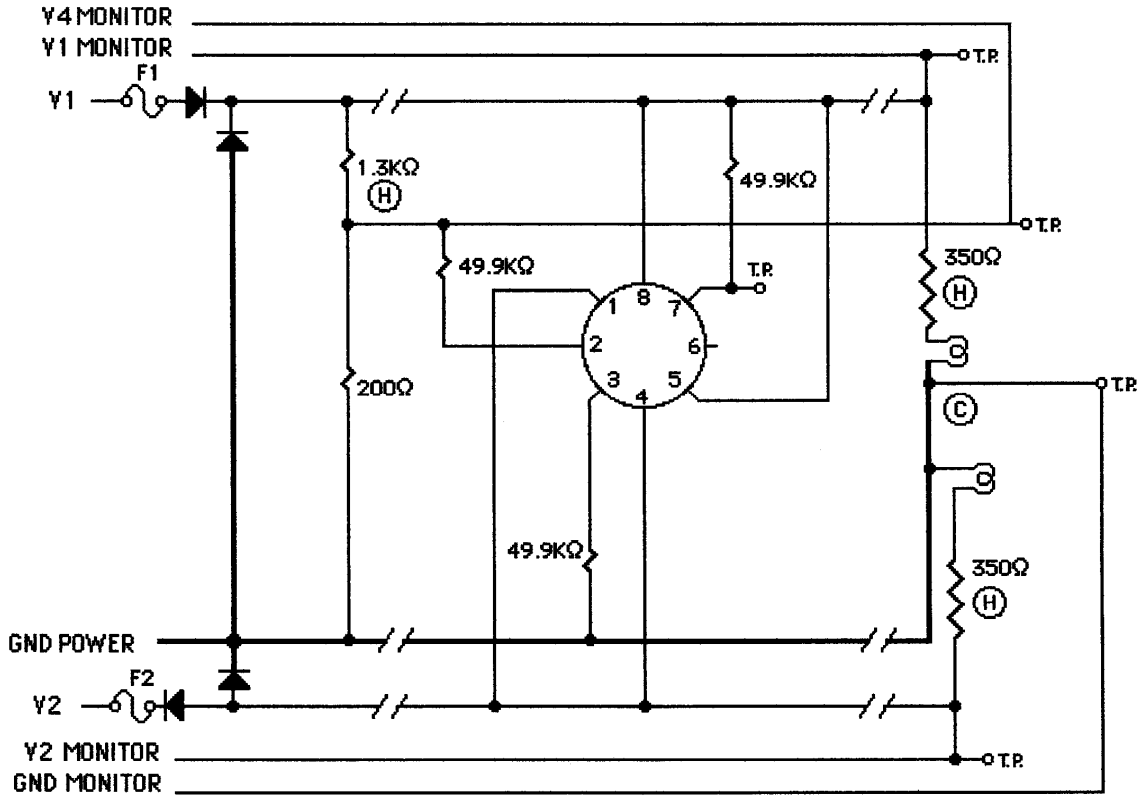
FIGURE 5



W PACKAGE
10-LEAD CERPAC

FIGURE 6

STATIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS



NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = +171 ° C maximum.
3. Ta = +150 ° C .
4. Burn-in Voltages: V1 = +15V to +16.5V
   V2 = -15V to -16.5V
   V4M = +1.9V to 2.3V
5. USE ALL OTHER INFORMATION ON # 04-06-0004

1. Ground
2. + Input
3. - Input
4. V-
5. Balance
6. Balance/Strobe
7. Output
8. V+

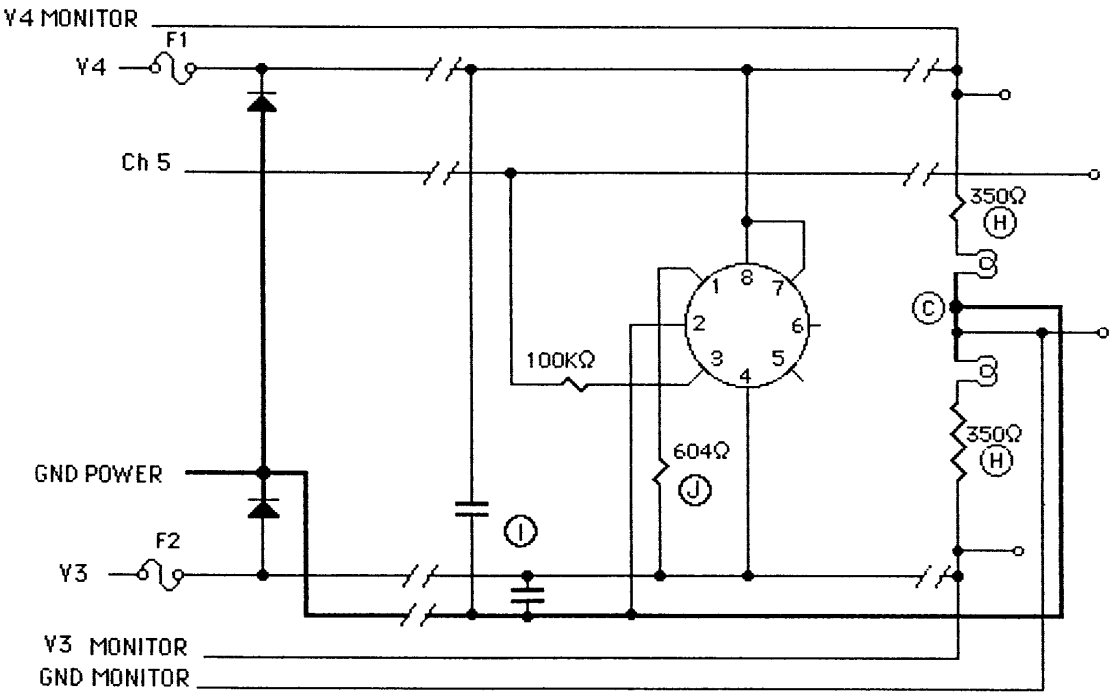
8 PIN TO-5

TOP VIEW

PACKAGE

FIGURE 7

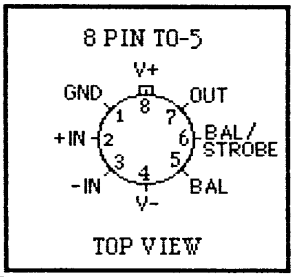
DYNAMIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 158 °C maximum.
3. Ta = 125 °C.
4. Burn-in Voltages: V4= + 15V to + 16.5V
   V3= - 15V to - 16.5V
5. CH. 5 = Square wave, + 2.0V to + 2.2V
   Gnd.
   - 2.0V to - 2.2V

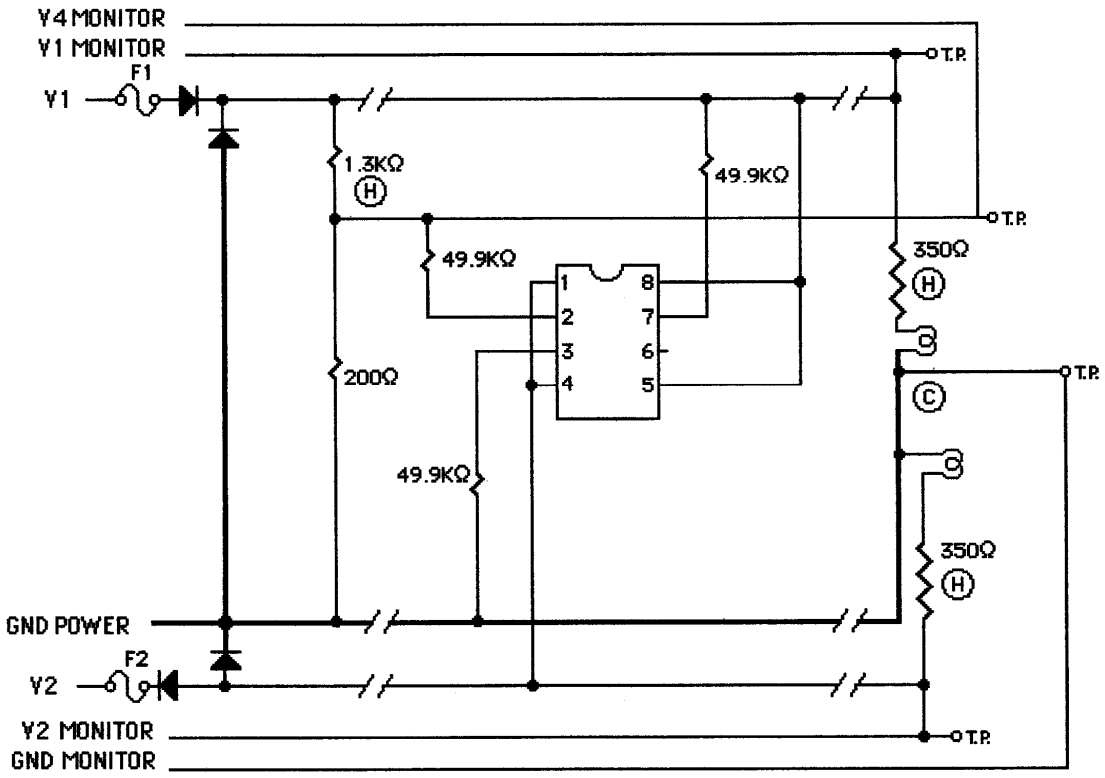
Frequency, 900hz (1.11ms) to 1100hz (909µs)



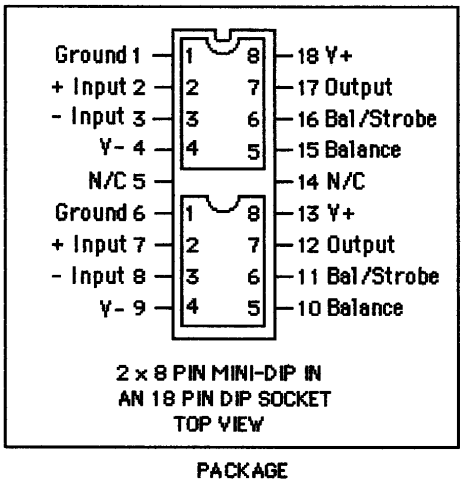
PACKAGE

FIGURE 8

STATIC BURN-IN CIRCUIT
OPTION #2, CERDIP / 8 LEADS



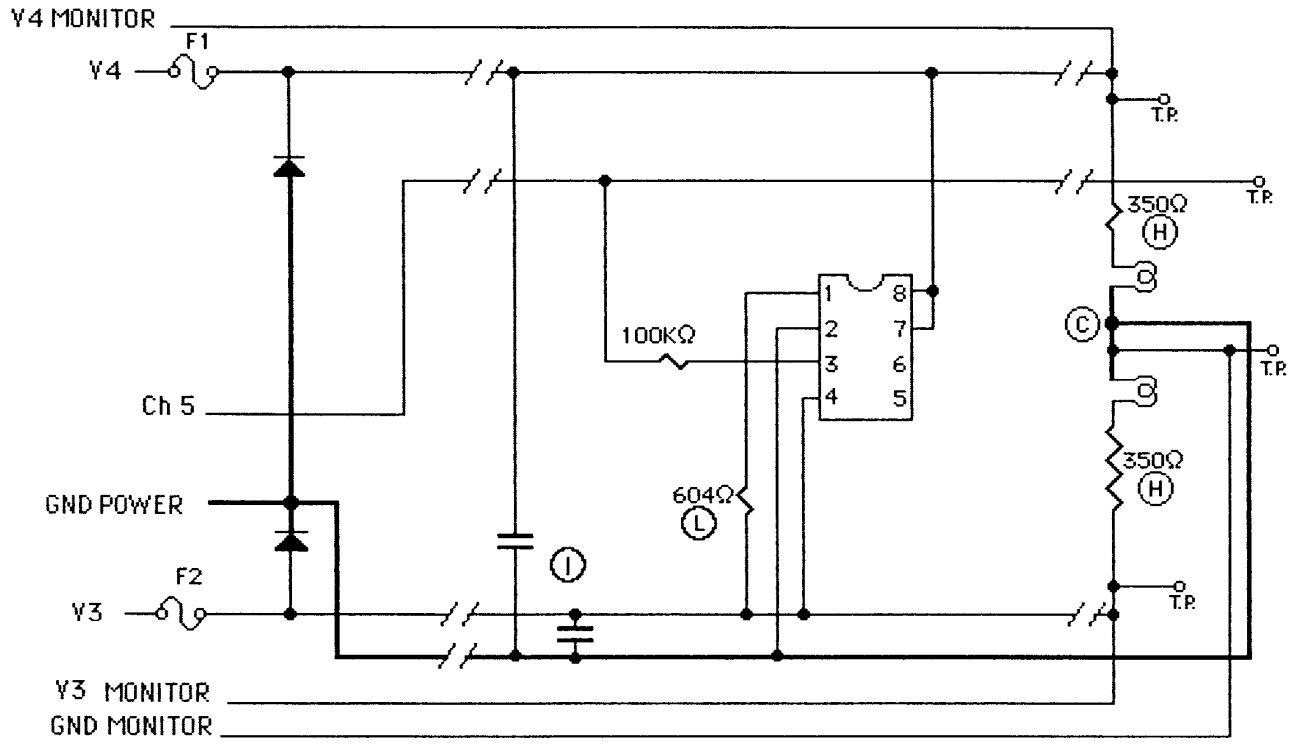
NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = +169 ° C maximum for N8 pkg at 150°C Ta.
3. Tj = +167 ° C maximum for J8 pkg at 150°C Ta.
4. Burn-in Voltages:V1 = +15V to +16.5V
   V2 = -15V to -16.5V
   V4M = +1.9V to +2.3V
5. USE ALL OTHER INFORMATION ON # 04-06-0006



PACKAGE

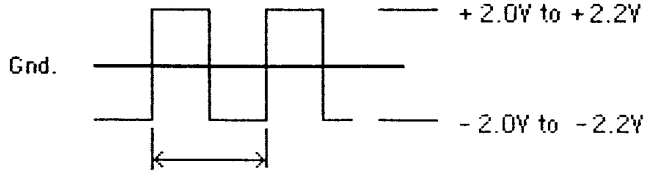
FIGURE 9

DYNAMIC BURN-IN CIRCUIT
OPTION 2, CERDIP / 8 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 155 °C maximum.
3. Ta = 125 °C.
4. Burn-in Voltages: V4= + 15V to + 16.5V
   V3= - 15V to - 16.5V
5. CH. 5 = Square wave,



Frequency, 900hz (1.11ms) to 1100hz (909µs)

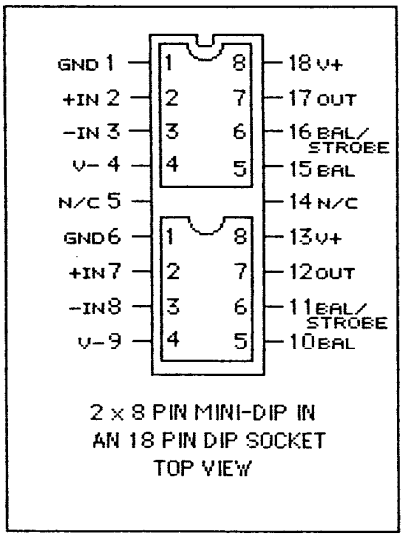
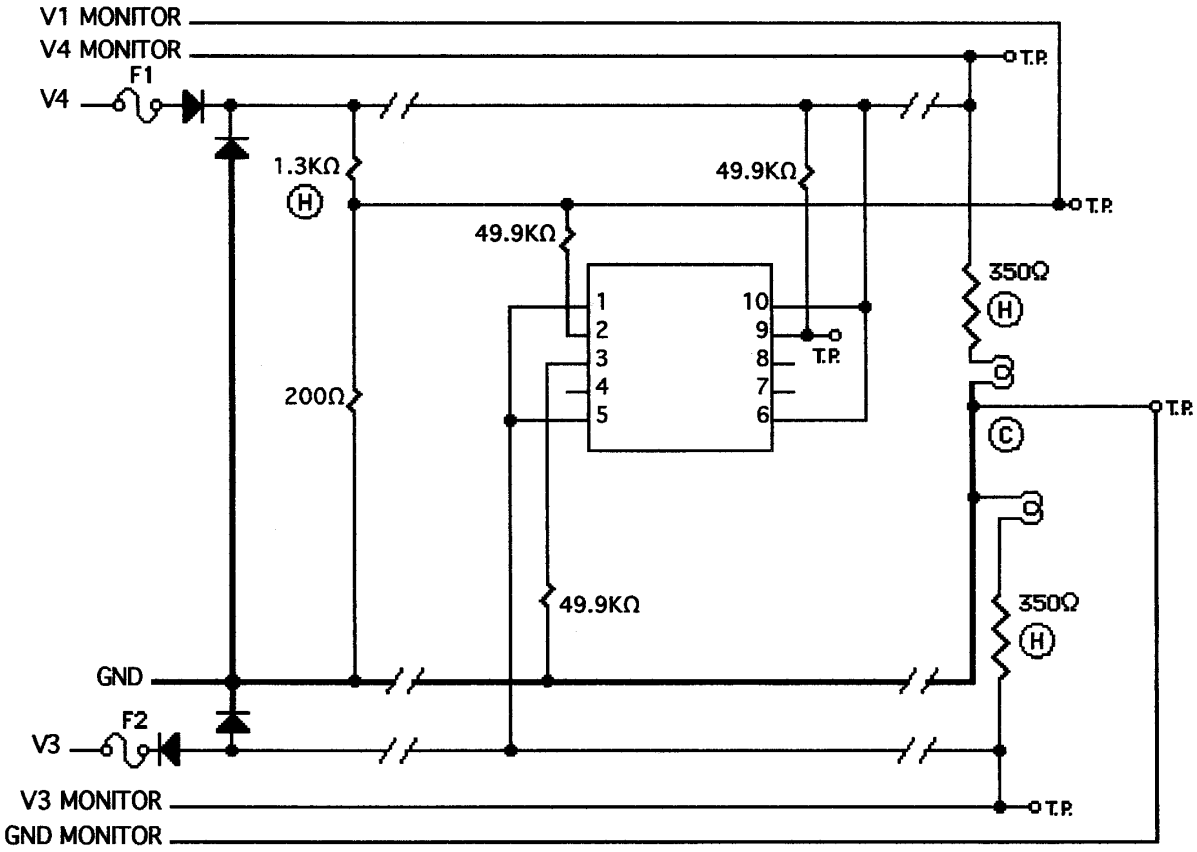
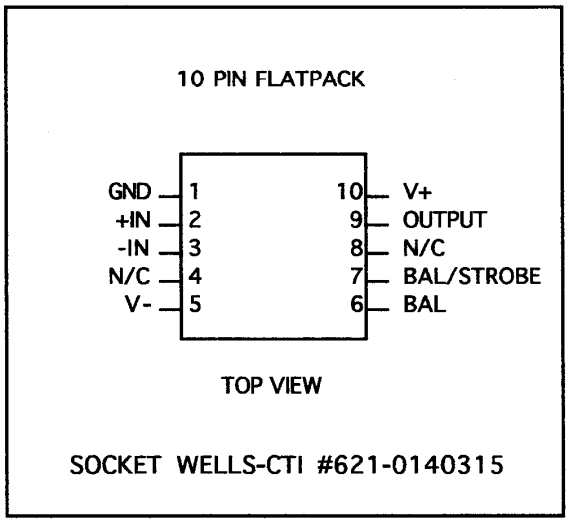


FIGURE 10

STATIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD



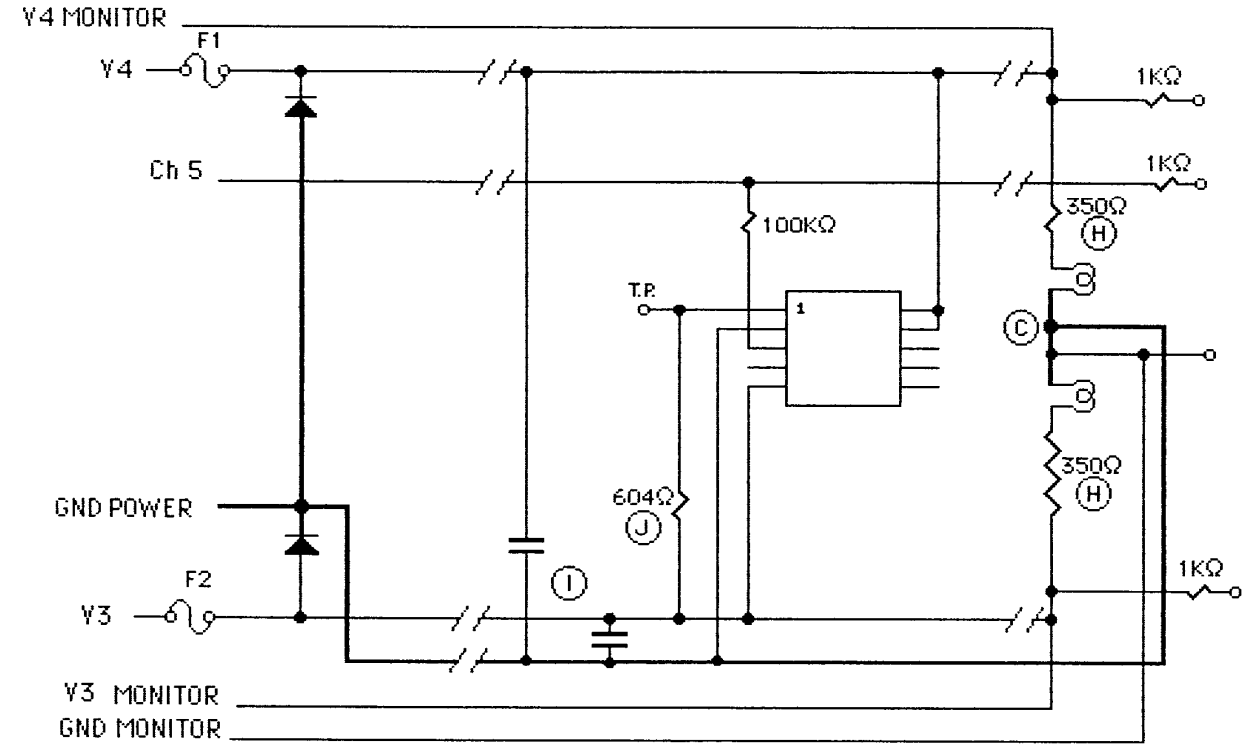
NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 172 °C maximum at Ta = 150 °C.
3. Tj = 147 °C maximum at Ta = 125 °C.
4. Burn-in Voltages: V4 = +15V to +16.5V
   V3 = -15V to -16.5V
   V1M = +1.9V to +2.3V



PACKAGE AND PINOUT

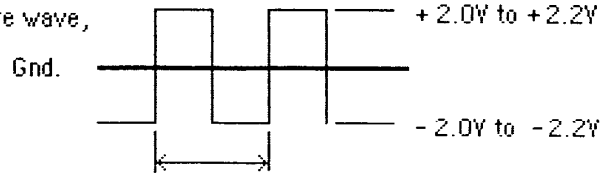
FIGURE 11

DYNAMIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD

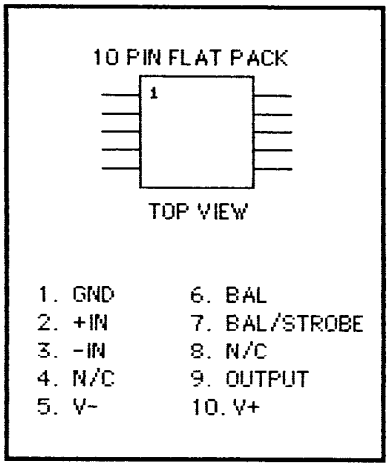


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 171 °C maximum.
3. Ta = 125 °C.
4. Burn-in Voltages: V4= + 15V to + 16.5V
   V3= - 15V to - 16.5V
5. CH. 5 = Square wave,



Frequency, 900hz (1.11ms) to 1100hz (909µs)



PACKAGE

FIGURE 12

TOTAL DOSE BIAS CIRCUIT

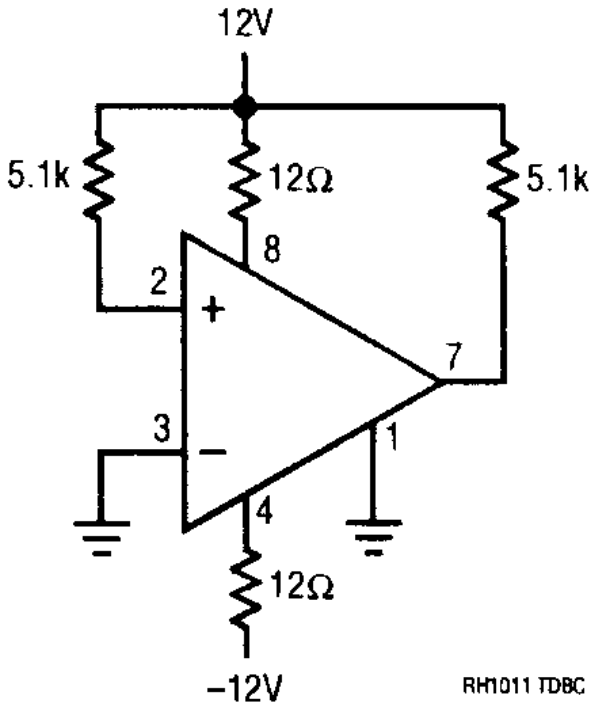


FIGURE 13

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE 10

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_A \le 125°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage		3			1.5	1			3.0	2,3	mV
		$R_S \le 50k\Omega$	4			2.0	1			3.0	2,3	mV
I_{OS}	Input Offset Current		3,4			4	1			20	2,3	nA
I_B	Input Bias Current		3			50	1			80	2,3	nA
			4			65	1			80	2,3	nA
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift	$T_{MIN} \le T \le T_{MAX}$	5,9							25		µV/°C
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L = 1k\Omega$, $-10V \le V_{OUT} \le 14.5V$		200			4					V/mV
		$V_S = 5V$, $R_L = 500\Omega$, $0.5V \le V_{OUT} \le 4.5V$		50			4					V/mV
CMRR	Common Mode Rejection Ratio			90			1					dB
	Input Voltage Range	$V_S = \pm 15V$	8,9	−14.5		13		−14.5		13		V
		V_S = Single 5V	8,9	0.5		3.0		0.5		3.0		V
t_d	Response Time		6,9			250						ns
V_{OL}	Output Saturation Voltage	$V_{IN}^- = 5mV$, $I_{SINK} = 8mA$	11			0.4	1			0.5	2,3	V
		$I_{SINK} = 50mA$				1.5	1			1.5	2,3	V
	Output Leakage Current	$V_{IN}^+ = 5mV$, $V_{GND} = -15V$, $V_{OUT} = 20V$				10	1			500	2,3	nA
	Positive Supply Current		11			4.0	1					mA
	Negative Supply Current		11			2.5	1					mA
	Strobe Current	Minimum to Ensure Output Transistor is Turned Off	7,9,11	500								µA
	Input Capacitance				6							pF

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE 10

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	MAX	20Krad(Si) MIN	MAX	50Krad(Si) MIN	MAX	100Krad(Si) MIN	MAX	200Krad(Si) MIN	MAX	UNITS
V_{OS}	Input Offset Voltage				1.5		1.5		1.5		2.5		4	mV
I_{OS}	Input Offset Current				4		4		4		20		50	nA
I_B	Input Bias Current				50		100		150		200		300	nA
A_{VOL}	Large-Signal Voltage Gain	$R_L = 1k\Omega$, $-10V \le V_{OUT} \le 14.5V$		200		200		150		100		50		V/mV
CMRR	Common Mode Rejection Ratio			90		90		90		90		86		dB
	Input Voltage Range	$V_S = \pm 15V$	8,9	−14.5	13	−14.5	13	−14.5	13	−14.5	13	−14.5	13	V
		V_S = Single 5V		0.5	3.0	0.5	3.0	0.5	3.0	0.5	3.0	0.5	3.0	V
V_{OL}	Output Saturation Voltage	$V_{IN}^- = 5mV$, $I_{SINK} = 8mA$	11		0.4		0.4		0.4		0.4		0.4	V
		$I_{SINK} = 50mA$			1.5		1.5		1.5		1.5		1.5	V
	Output Leakage Current	$V_{IN}^+ = 5mV$, $V_{GND} = -15V$ $V_{OUT} = 20V$			10		10		100		100		100	nA

SPECIAL NOTES:
TABLE II IS CONTINUED ON THE FOLLOWING PAGE.
DATA SHEET NOTES FOR TABLE I AND TABLE II FOLLOW TABLE II.

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE 10 (CONTINUED)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	10Krad(Si) MAX	20Krad(Si) MIN	20Krad(Si) MAX	50Krad(Si) MIN	50Krad(Si) MAX	100Krad(Si) MIN	100Krad(Si) MAX	200Krad(Si) MIN	200Krad(Si) MAX	UNITS
	Positive Supply Current		11		4.0		4.0		4.0		4.0		4.0	mA
	Negative Supply Current		11		2.5		2.5		2.5		2.5		2.5	mA
	Strobe Current	Minimum to Ensure Output Transistor is Turned Off	7,9,11	500		500		500		500		500		µA
	Input Capacitance				6 (Typ)		6 (Typ)		6 (Typ)		6 (Typ)		6 (Typ)	pF

Note 1: Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection discussion in the LT®1011 data sheet.

Note 2: T_{JMAX} = 150°C.

Note 3: Output is sinking 1.5mA with V_{OUT} = 0V.

Note 4: These specifications apply for all supply voltages from a single 5V to ±15V, the entire input voltage range and for both high and low output states. The high state is $I_{SINK} \geq 100\mu A$, $V_{OUT} \geq (V^+ - 1V)$ and the low state is $I_{SINK} \leq 8mA$, $V_{OUT} \leq 0.8V$. Therefore, this specication defines a worst-case error band that includes effects due to common mode signals, voltage gain and output load.

Note 5: Drift is calculated by dividing the offset difference measured at minimum and maximum temperatures by the temperature difference.

Note 6: Response time is measured with a 100mV step and 5mV overdrive. The output load is a 500Ω resistor tied to 5V. Time measurement is taken when the output crosses 1.4V.

Note 7: Do not short the STROBE pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500µA will strobe the RH1011 if speed is not important. External leakage on the STROBE pin in excess of 0.2µA when the strobe is "off" can cause offset voltage shifts.

Note 8: See graph, Input Offset Voltage vs Common Mode Voltage on the LT1011 data sheet.

Note 9: Guaranteed by design, characterization or correlation to other tested parameters.

Note 10: V_S = ±15V, V_{CM} = 0V, R_S = 0Ω, T_A = 25°C, V_{GND} = V^-, output at Pin 7, unless otherwise noted.

Note 11: V_{GND} = 0V.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-1.5	1.5	-0.5	0.5	mV
$+I_B$	-50	50	-5.0	5.0	nA
$-I_B$	-50	50	-5.0	5.0	nA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5, 6
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3, 4, 5, 6
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.