

REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	05/08/00
A	<ul style="list-style-type: none"> • PAGE 3, PARAGRAPH 3.7.1, CHANGED THE DOSAGE RATE FROM “APPROXIMATELY 20 RADS PER SECOND” TO “LESS THAN OR EQUAL TO 10 RADS PER SECOND”. • PAGE 4, PARAGRAPH 6.1 CHANGED QUALITY ASSURANCE PROVISIONS TO STATE THAT LTC IS QML CERTIFIED AND THAT RAD HARD CANDIDATES ARE ASSEMBLED ON QUALIFIED ON CLASS S MANUFACTURING LINES. • PAGE 11, TABLES I AND II ARE ON PAGE 11. TABLE II IS CONTINUED ON PAGE 12. • CONVERSION OF SPECIFICATION FROM WORD PERFECT TO MICROSOFT WORD. 	04/16/03
B	DATA SHEET REVISED. <ul style="list-style-type: none"> • PAGE 3, PARAGRAPH 3.4, REVISED TO MATCH THE DATA SHEET. • PAGE 8, FIGURE 3, REVISED TO MATCH THE DATA SHEET. • PAGE 11, TABLE I, II REVISED TO MATCH THE DATA SHEET. 	09/20/04
C	<ul style="list-style-type: none"> • PAGE 3, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC. 	03/21/05
D	<ul style="list-style-type: none"> • PAGE 3, PARAGRAPH 3.7.1 CHANGED VERBIAGE. 	05/05/08
E	<ul style="list-style-type: none"> • PAGE 13, CHANGED RH CANNED SAMPLE TABLE III FOR QUALIFYING DICE SALES ADDED TEMPERATURE CYCLE, CONSTANT ACCELERATION & REMOVED PIND TEST. 	02/10/09
F	Page 2, amended section 3.3, <u>Special Handling of Dice</u> , to more accurately describe our current procedures and requirements.	03/30/12
G	Page 13, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from “15%” to “10%”.	07/02/13
H	Updated Die Sales table on pg 13.	5/20/15
I	To remove source and change Linear to Analog	2/2/21

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13			
INDEX	REVISION	H	H	H	H	H	H	H	H	H	H	H	H	H			
REVISION	PAGE NO.																
INDEX	REVISION																
											ANALOG DEVICES INC.						
	ORIG										TITLE: MICROCIRCUIT, LINEAR, RH1011 VOLTAGE COMPARATOR DICE						
	DSGN																
	ENGR																
	MFG																
	CM																
	QA																
	PROG								SIZE	CAGE CODE	DRAWING NUMBER	REV					
										64155	05-08-5149	I					
APPLICATION	FUNCT	SIGNOFFS		DATE	CONTRACT:												

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1.0 SCOPE:

- 1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

- 2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

- 2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

- 3.1 General Description: This specification details the requirements for the RH1011 VOLTAGE COMPARATOR DICE and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

- 3.2 Part Number: RH1011 Dice

- 3.3 **Special Handling of Dice:** Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Analog Devices Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

ADI recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

Supply Voltage (Pin 8 to Pin 4)	36V
Output to Negative Supply (Pin 7 to Pin 4)	35V
Ground to Negative Supply (Pin 1 to Pin 4)	30V
Differential Input Voltage	+35V
Voltage at Strobe Pin (Pin 6 to Pin 8)	5V
Input Voltage $\frac{1}{}$	EQUAL TO SUPPLIES
Output Short Circuit Duration	10 sec
Operating Temperature Range	-55°C to +125°C
T _{jmax}	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

1/ Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection discussion in the LT1011 data sheet.

- 3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.
- 3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in Figure 1.
- 3.7 Radiation Hardness Assurance (RHA):
- 3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.
- 3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.
- 3.7.3 Total dose bias circuit is specified in Figure 2.
- 3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at Ta = +25°C to the limits shown in Table I herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.
- 3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a minimum of 4KÅ.
- 3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.
- 3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.
- 4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.

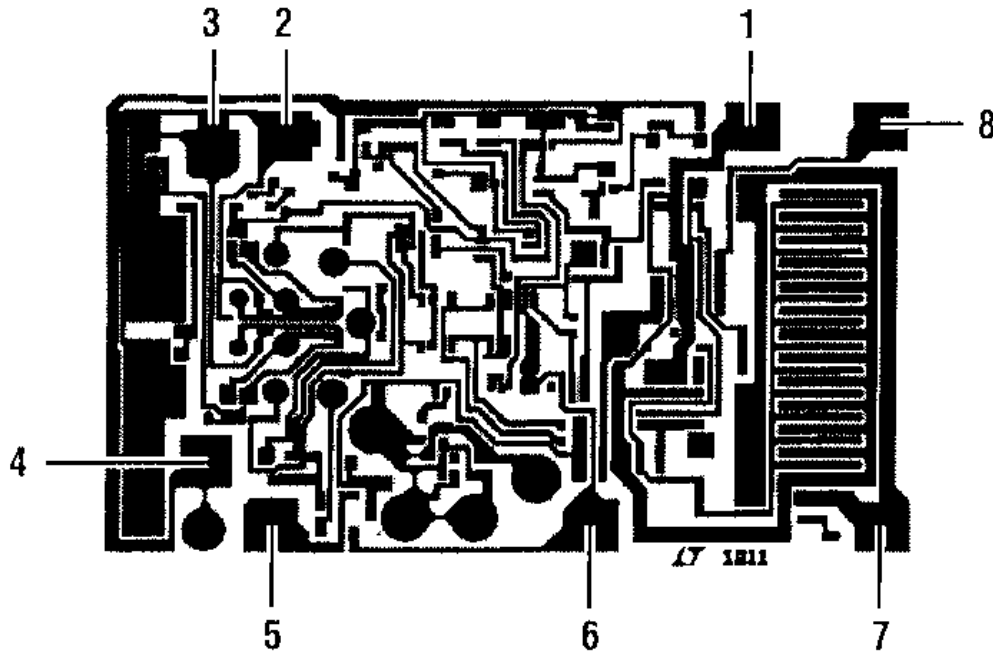
- 5.0 SAMPLE ELEMENT EVALUATION: A sample from each wafer supplying dice shall be assembled and subjected to element evaluation per Table III herein.
- 5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.
- 5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in Table I and Table II herein.
- 5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.
- 5.4 Part Marking of Element Evaluation Sample Includes:
- 5.4.1 LTC Logo
 - 5.4.2 LTC Part Number
 - 5.4.3 Date Code
 - 5.4.4 Serial Number
 - 5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A
 - 5.4.6 Diffusion Lot Number
 - 5.4.7 Wafer Number
- 5.5 Burn-In Requirement: Burn-In circuit for TO5 package is specified in Figure 3.
- 5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with Figure 4.
- 5.7 Terminal Connections: The terminal connections shall be as specified in Figure 5.
- 5.8 Lead Material and Finish: The lead material and finish shall be Kovar with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.
- 6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)
- 6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.
- 6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with Table III herein.
- 6.3 Screening: Screening requirements shall be in accordance with Table III herein.
- 6.4 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

- 6.4.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.
- 6.4.2 100% attributes (completed element evaluation traveler).
- 6.4.3 Element Evaluation variables data, including Burn-In and Op Life
- 6.4.4 SEM photographs (3.10 herein)
- 6.4.5 Wafer Lot Acceptance Report (3.9 herein)
- 6.4.6 A copy of outside test laboratory radiation report if ordered
- 6.4.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6.4.1 and 6.4.7 will be delivered as a minimum, with each shipment.

- 7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS



Die Size: 80 x 48 mils
Thickness: 12 mils
Backside Metal: Gold

PAD FUNCTION

1. Ground	5. Balance
2. +IN	6. Balance/Strobe
3. -IN	7. Output
4. V^-	8. V^+

Note: Backside (substrate) may be connected to V^- or no connection

FIGURE 1

TOTAL DOSE BIAS CIRCUIT

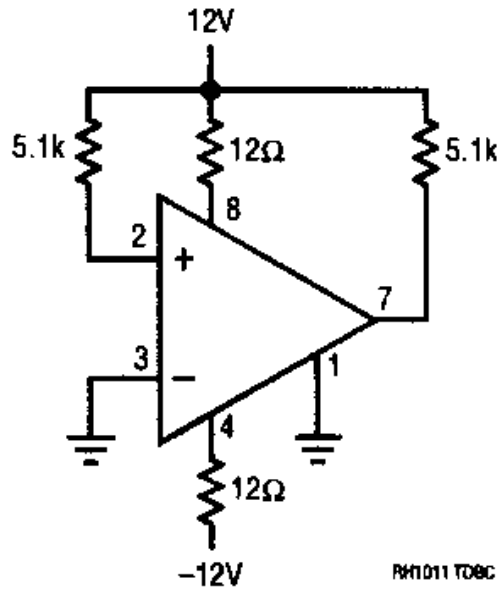
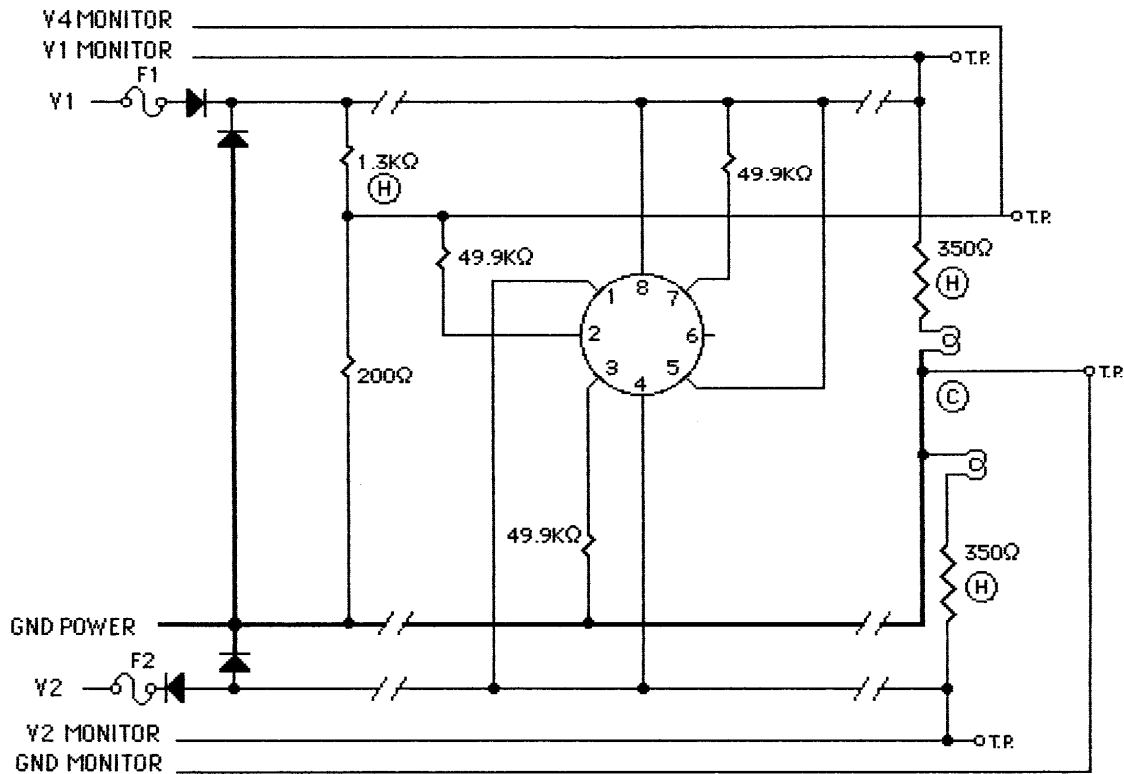


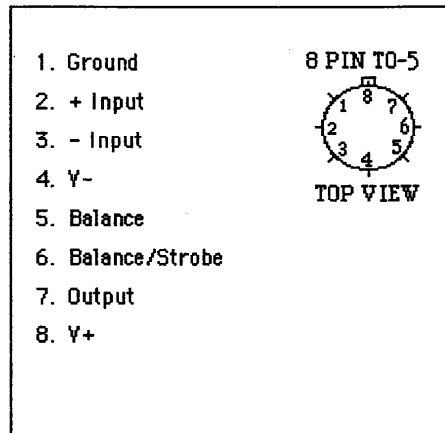
FIGURE 2

BURN-IN CIRCUIT



NOTES:

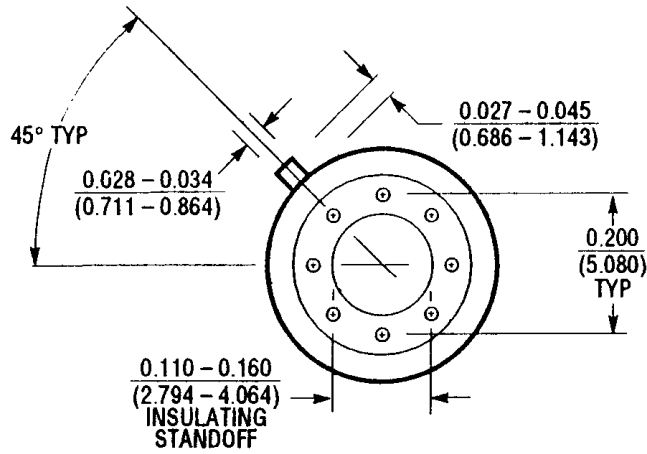
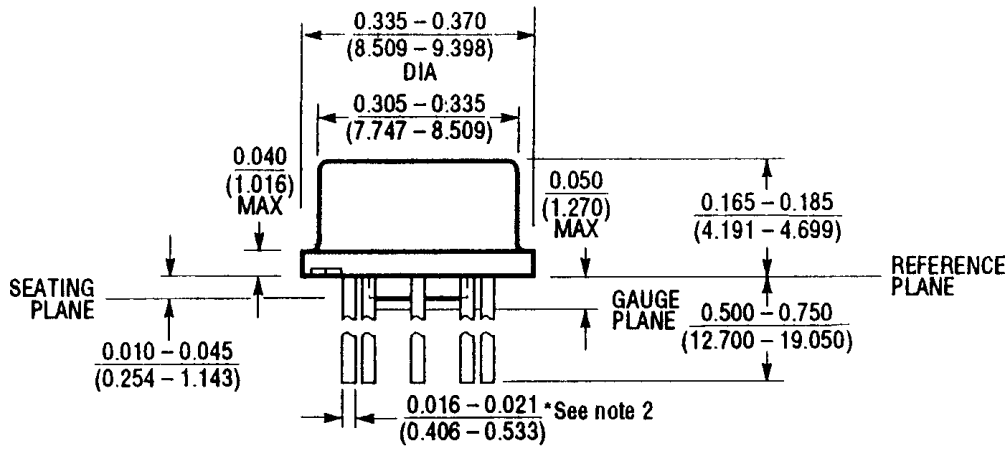
1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = +160^\circ \text{C}$ maximum.
3. $T_a = +125^\circ \text{C}$.
4. Burn-in Voltages: $V_1 = +15\text{V}$ to $+16.5\text{V}$
 $V_2 = -15\text{V}$ to -16.5V
 $V_{4M} = +2.0\text{V}$ to $+2.2\text{V}$
5. USE ALL OTHER INFORMATION ON # 04-06-0004



PACKAGE

FIGURE 3

TO5, 8 LEADS, CASE OUTLINE



NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

$\theta_{ja} = +150^{\circ}\text{C/W}$

$\theta_{jc} = +40^{\circ}\text{C/W}$

FIGURE 4

TERMINAL CONNECTIONS

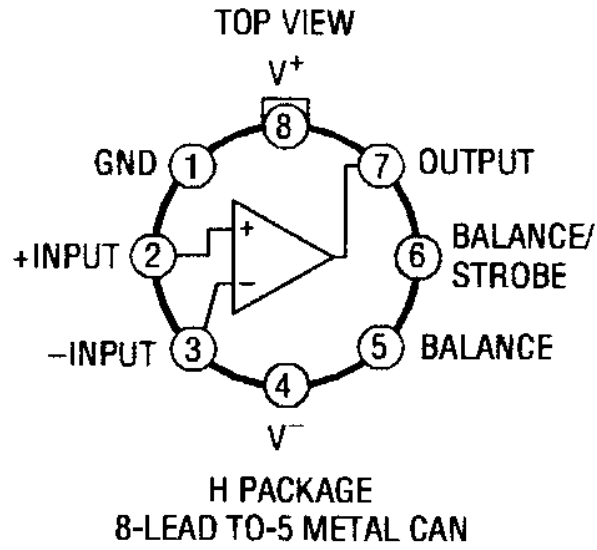


FIGURE 5

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation

$$V_S = \pm 15V, V_{CM} = 0V, R_S = 0\Omega, T_J = 25^\circ C, V_{GND} = 0V$$

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1) $R_S \leq 50k$ (Note 2)		1.5 2.0	mV mV
I_{OS}	Input Offset Current	(Note 2)		4	nA
I_B	Input Bias Current	(Note 1) (Note 2)		50 65	nA nA
A_{VOL}	Large-Signal Voltage Gain	$R_L = 1k$ to 15V, $-10V \leq V_{OUT} \leq 14.5V$ $R_L = 500\Omega$ to 5V, $0.5V \leq V_{OUT} \leq 4.5V$	200 50		V/mV V/mV
CMRR	Common Mode Rejection Ratio		90		dB
	Input Voltage Range	$V_S = \pm 15V$ $V_S = \text{Single } 5V$	-14.5 0.5	13 3	V V
V_{OL}	Output Saturation Voltage	$V_{IN} = 5mV$, $I_{SINK} = 8mA$ $I_{SINK} = 50mA$		0.4 1.5	V V
	Output Leakage Current	$V_{IN} = 5mV$, $V_{GND} = -15V$ $V_{OUT} = 20V$		10 500	nA nA
	Positive Supply Current			4	mA
	Negative Supply Current			2.5	mA
	Strobe Current	Minimum to Ensure Output Transistor Is Off	500		μA

Note 1: Output is sinking 1.5mA with $V_{OUT} = 0V$.

Note 2: These specifications apply for all supply voltages from a single 5V to $\pm 15V$, the entire input voltage range and for both high and low output states. The high state is $I_{SINK} \geq 100\mu A$, $V_{OUT} \geq (V^+ - 1V)$ and the low state is $I_{SINK} \leq 8mA$, $V_{OUT} \leq 0.8V$. Therefore, this specification

defines a worst-case error band that includes effects due to common mode signals, voltage gain and output load.

Note 3: Please refer to LTC standard product data sheets for all other applicable information.

TABLE II ELECTRICAL CHARACTERISTICS – (Post-Irradiation) SEE NOTE 10

$$V_S = \pm 15V, V_{CM} = 0V, R_S = 0\Omega, T_J = 25^\circ C, V_{GND} = V^-, \text{OUTPUT AT PIN 7, UNLESS OTHERWISE NOTED}$$

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si)		20Krad(Si)		50Krad(Si)		100Krad(Si)		200Krad(Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Input Offset Voltage			1.5	1.5	1.5	1.5	2.5	4					mV
I_{OS}	Input Offset Current			4	4	4	20	50						nA
I_B	Input Bias Current			50	100	150	200	300						nA
A_{VOL}	Large-Signal Voltage Gain	$R_L = 1k\Omega$, $-10V \leq V_{OUT} \leq 14.5V$		200	200	150	100	50						V/mV
CMRR	Common Mode Rejection Ratio			90	90	90	90	86						dB
	Input Voltage Range	$V_S = \pm 15V$ $V_S = \text{Single } 5V$	8,9	-14.5 0.5	13 3.0	-14.5 0.5	13 3.0	-14.5 0.5	13 3.0	-14.5 0.5	13 3.0	-14.5 0.5	13 3.0	V V
V_{OL}	Output Saturation Voltage	$V_{IN}^- = 5mV$, $I_{SINK} = 8mA$ $I_{SINK} = 50mA$	11	0.4 1.5	0.4 1.5	0.4 1.5	0.4 1.5	0.4 1.5						V V
	Output Leakage Current	$V_{IN}^+ = 5mV$, $V_{GND} = -15V$ $V_{OUT} = 20V$		10	10	100	100	100						nA

SPECIAL NOTE: TABLE II AND APPLICABLE NOTES ARE CONTINUED ON THE FOLLOWING PAGE.

TABLE II ELECTRICAL CHARACTERISTICS – (Post-Irradiation)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si)		20Krad(Si)		50Krad(Si)		100Krad(Si)		200Krad(Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Positive Supply Current			4.0		4.0		4.0		4.0		4.0		mA
	Negative Supply Current			2.5		2.5		2.5		2.5		2.5		mA
	Strobe Current	Minimum to Ensure Output Transistor is Truned Off	7,9	500		500		500		500		500		μ A
	Input Capacitance			6 (Typ)		6 (Typ)		6 (Typ)		6 (Typ)		6 (Typ)		pF

Note 7: Do not short the STROBE pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500 μ A will strobe the RH1011 if speed is not important. External leakage on the STROBE pin in excess of 0.2 μ A when the strobe is "off" can cause offset voltage shifts.

Note 8: See graph, Input Offset Voltage vs Common Mode Voltage on the LT1011 data sheet.

Note 9: Guaranteed by design, characterization or correlation to other tested parameters.

Note 10: $V_S = \pm 15V$, $V_{CM} = 0V$, $R_S = 0$, $T_A = 25^\circ C$, $V_1 = -15V$, output at Pin 7, unless otherwise noted.

NOTES 1 THROUGH 6 DO NOT PERTAIN TO THE ELECTRICAL CHARACTERISTICS FOR DICE THEREFORE HAVE BEEN REMOVED.



RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

TABLE III RH ELEMENT EVALUATION TABLE QUALIFICATION OF DICE SALES

SUBGROUP	CLASS			OPERATION	MIL-STD-883		QUANTITY (ACCEPT NUMBER)
	K/S	V	H/B		METHOD	CONDITION	
1	X	X		SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25°C)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
	X	X		BOND PULL MONITOR	2011		
5	X	X		STABILIZATION BAKE	1008	C	ASSEMBLED PARTS ONLY
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
	X	X		GROSS LEAK	1014	C	
6	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			45(0)
	X	X		PRE BURN-IN/ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X	X		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs.	1015	+ 125°C MINIMUM 240 HOURS	
	X	X		POST BURN-IN/ELECT. READ & RECORD @ 25°C			
	X	X		POST BURN-IN/ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X	X		TOTAL IRRADIATION DOSE	1019	A	
	X	X		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	X	X		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005	+ 125°C MINIMUM 1000 HOURS	
	X	X		POST OP-LIFE ELECT. (R & R @ 25°C, +125°C DR, +150°C, -55°C			
7	X	X	X	WIRE BOND EVALUATION	2011		15(0) OR 25(1) - # of wires

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Subgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.