ANALOG DEVICES, INC.

DOCUMENT TITLE: RH1016M, ULTRAFAST PRECISION 10ns COMPARATOR
DOCUMENT NUMBER: 05-08-5222

REV. & APPROVAL	ECN No. & ISSUE DATE	CHANGE
Ø	538358 (06-18-08)	1. INITIAL RELEASE
A	19-C51571 T.PHAMNGUYEN (05-03-19)	1. THIS REQUEST CAME IN 11/2014 BUT THE ECN WAS NEVER COMPLETED. REMOVED "OPTION 1" IN SECTION 3.2.1 CHANGED LTC FOOTER TO ANALOG DEVICE INC. CHANGED ALL LTC REFERENCE TO ADI
B	21-C51723 R.SOARES (03-19-21)	1. TO CHANGE LINEAR TO ANALOG AND REMOVE SOURCE

REV. CHANGES DENOTED BY "REDLINED" AREAS

DCBS:
CONTROLLED: MASTER CONTROL

CONTROLLED HILLVIEW:

NON-CONTROLLED:

FORM# 00-03-0103B

REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/18/08
A	Removed "Option 1" in section 3.2.1 Changed LTC footer to Analog Device Inc. Changed all LTC reference to ADI	04/10/19
B	**To change Linear to Analog and remove source**	**3/19/21**

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12					
INDEX	REVISION	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**	**A**					
REVISION	PAGE NO.																	
INDEX	REVISION																	

				ANALOG DEVICES INC.			
	ORIG			TITLE: **MICROCIRCUIT, LINEAR, RH1016, ULTRAFAST PRECISION 10ns COMPARATOR**			
	DSGN						
	ENGR						
	MFG						
	CM						
	QA			SIZE	CAGE CODE	DRAWING NUMBER	REV
	PROG				**64155**	**05-08-5222**	**B**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:			

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1016M Reference processed to space level manufacturing flow.

3.2 Part Number: **RH1016MW (Glass Sealed Flatpack, 10 Leads)**

3.3 Part Marking Includes:

a. LTC Logo

b. ADI Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:
(Note 1)

Positive Supply Voltage **(Note 5)**	7V
Negative Supply Voltage	-7V
Differential Input Voltage **(Note 7)**	±5V
+IN,-IN and LATCH ENABLE Current **(Note 7)**	±10mA
Output Circuit (Continuous) **(Note 7)**	±20mA
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

(**For Notes 1, 5, 7 see page 11)**

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and Table II.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in Table IV herein.

3.8 Burn-In Requirement: Burn-in circuit is specified in Figure 4 .

3.9 Delta Limit Requirement: Delta limit parameters are specified in Table III herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 2.

3.10.3 Lead Material and Finish: The lead material and finish for Option 1 shall be Alloy 42 with lead finish hot solder dip (Finish litter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 3.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and **3.4** of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs **3.1, 3.1.1,** and **3.4** of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1 Group B, Subgroup 2c = 10%

Group B, Subgroup 3 = 10%

Group B, Subgroup 4 = 5%

Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)

Group B, subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.5.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.5.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.5.3 Burn-In Variables Data and Deltas (if applicable)

4.5.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.5.5 Generic Group D data (4.4.3 herein)

4.5.6 SEM photographs (3.13 herein)

4.5.7 Wafer Lot Acceptance Report (3.13 herein)

4.5.8 X-Ray Negatives and Radiographic Report

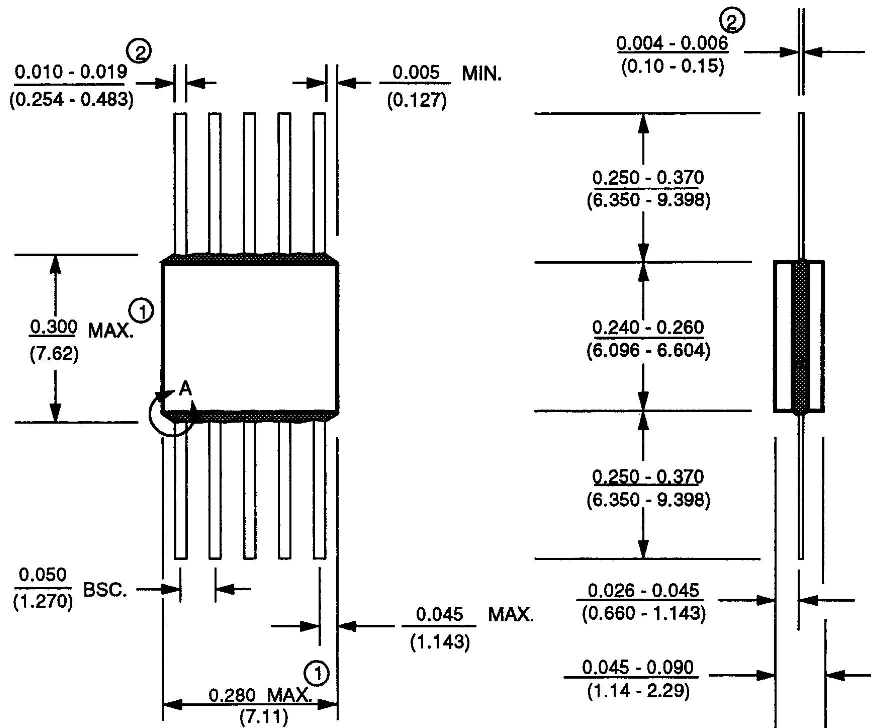
4.5.9 A copy of outside test laboratory radiation report if ordered

4.5.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.5.1 and 4.5.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as “No Charge Data”.

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

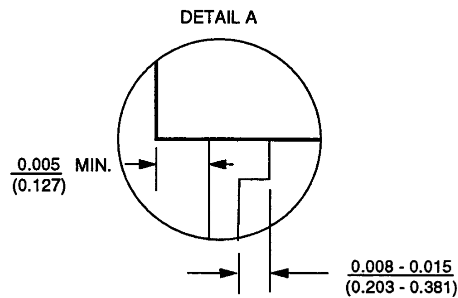
(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



NOTES:

① THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN

② INCREASE DIMENSIONS BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED)



θja = +170°C/W
θjc = +40°C/W

FIGURE 1

TERMINAL CONNECTIONS

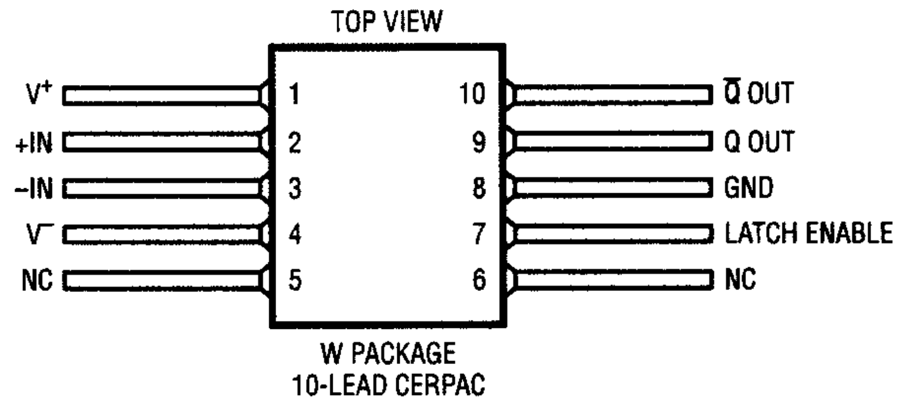


FIGURE 2

TOTAL DOSE BIAS CIRCUIT

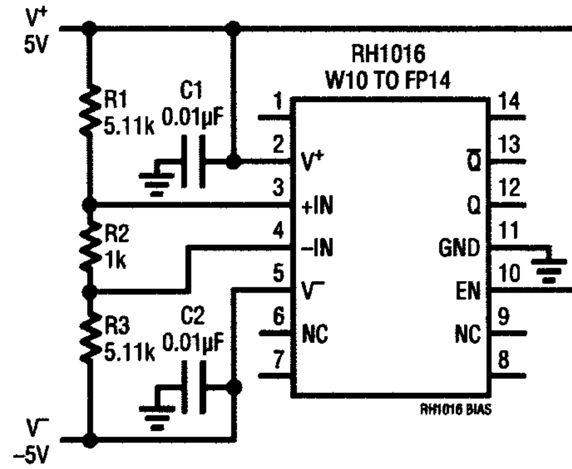
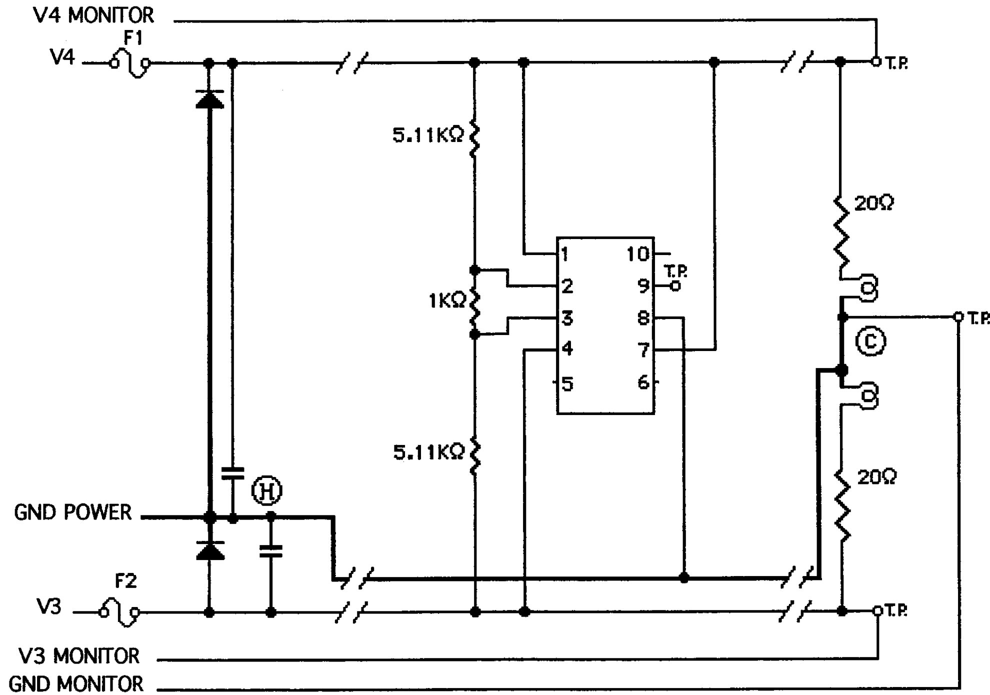


FIGURE 3

STATIC BURN-IN CIRCUIT
OPTION 2, GLASS SEALED FLATPACK / 10 LEAD



NOTES:
1. Unless otherwise specified, component tolerances
2. shall be per military specification.
3. Tj = +173 °C maximum.
4. Ta = +125 °C minimum.
   Burn-in voltages: V4 = +5.5V to +6.0V
   V3 = -5.5V to -6.0V

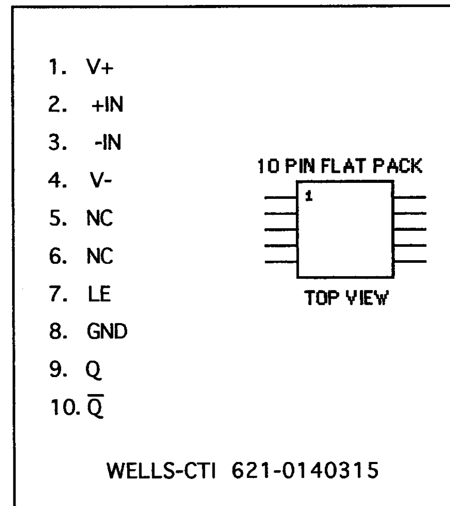


FIGURE 4

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION)

$V^+ = 5V$, $V^- = -5V$, $V_{OUT(Q)} = 1.4V$, $V_{LATCH} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_A \le 125°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$	2		1	±3	1			±4	2, 3	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift								4			μV/°C
I_{OS}	Input Offset Current		2		0.3	1	1			1.3	2, 3	μA
I_B	Input Bias Current		3		5	10	1			13	2, 3	μA
	Input Voltage Range		6					–3.75		3.5		V
		Single 5V Supply	6					1.25		3.5		V
CMRR	Common Mode Rejection	$-3.75V \le V_{CM} \le 3.5V$					1	80	90		2, 3	dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \le V^+ \le 5.4V$		60	75		1	54			2, 3	dB
		Negative Supply $-7V \le V^- \le -2V$		80	100		1	80			2, 3	dB
A_V	Small-Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		1400	3000		4					V/V
V_{OH}	Output High Voltage	$V^+ \ge 4.6V$, $I_{OUT} = 1mA$					1	2.65	3.2		2, 3	V
		$I_{OUT} = 10mA$					1	2.40	3		2, 3	V
V_{OL}	Output Low Voltage	$I_{SINK} = 4mA$					1		0.3	0.55	2, 3	V
I^+	Positive Supply Current						1		25	35	2, 3	mA
I^-	Negative Supply Current						1		3	5	2,3	mA
V_{IH}	LATCH Pin High Input Voltage							2				V
V_{IL}	LATCH Pin Low Input Voltage									0.8		V
I_{IL}	LATCH Pin Current	$V_{LATCH} = 0V$					1			500	2, 3	μA
t_{PD}	Propagation Delay	$\Delta V_{IN} = 100mV$, OD = 5mV	4		10	14	4			16	5	ns
		$\Delta V_{IN} = 100mV$, OD = 20mV	4		9	12	4			15	5	ns

See Footnotes after table II.

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION)

(Postirradiation) T_A = 25°C, V^+ = 5V, V^- = –5V, $V_{OUT(Q)}$ = 1.4V, V_{LATCH} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDTIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$	2		±4		±4.5		±5		±5.5		±6	mV
I_{OS}	Input Offset Current		2		2		2.5		5		8		12	µA
I_B	Input Bias Current		3		12		12		14		17		20	µA
	Input Voltage Range		6	–3.75	3.5	–3.75	3.5	–3.75	3.5	–3.75	3.5	–3.75	3.5	V
		Single 5V Supply	6	1.25	3.5	1.25	3.5	1.25	3.5	1.25	3.5	1.25	3.5	V
CMRR	Common Mode Rejection Ratio	$-3.75V \le V_{CM} \le 3.5V$		80		77		74		70		65		dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \le V^+ \le 5.4V$		60		58		56		53		50		dB
		Negative Supply $-7V \le V^- \le -2V$		78		76		74		72		70		dB
A_V	Small-Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		1300		1200		1100		1000		900		V/V
V_{OH}	Output High Voltage	$V^+ \ge 4.6V$, I_{OUT} = 1mA		2.65		2.65		2.64		2.63		2.60		V
		I_{OUT} = 10mA		2.40		2.40		2.39		2.38		2.35		V
V_{OL}	Output Low Voltage	I_{SINK} = 4mA			0.55		0.55		0.56		0.57		0.6	V
I^+	Positive Supply Current				35		35		35		35		35	mA
I^-	Negative Supply Current				5		5		5		5		5	mA
I_{IL}	LATCH Pin Current	V_{LATCH} = 0V			525		575		650		725		800	µA
t_{PD}	Propagation Delay	ΔV_{IN} = 100mV, OD = 5mV	4		16		16		16		16		16	ns
		ΔV_{IN} = 100mV, OD = 20mV	4		14		14		14		14		14	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 3: Input bias current (I_B) is defined as the average of the two input currents.

Note 4: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The RH1016 is sample tested with a 1V step and 500mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} limits shown can be guaranteed with this test if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to overdrive.

Note 5: Electrical specifications apply only up to 5.4V.

Note 6: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization. See the LT1016 data sheet for discussion of input voltage range for supplies other than ±5V or 5V.

Note 7: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
VOS	-3	3	-1	1	mV
I_B	-10	10	-5	5	uA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5
GROUP A TEST REQUIREMENTS (METHOD 5005)	1*, 2, 3, 4, 5
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cool down as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.