REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	03/06/09
A	Page 2, amended section 3.3, Special Handling of Dice, to more accurately describe our current procedures and requirements.	03/30/12
B	Page 13, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from “15%” to “10%”.	07/02/13
C	Updated Die Sales table on pg 13.	05/20/15
D	**To remove source inspection and change Linear to Analog**	**2/2/21**

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13			
INDEX	REVISION	**C**	**C**	**C**	**C**	**C**	**C**	**C**	**C**	**C**	**C**	**C**	**C**	**C**			
REVISION	PAGE NO.																
INDEX	REVISION																

APPLICATION	FUNCT	SIGNOFFS	DATE
	ORIG		
	DSGN		
	ENGR		
	MFG		
	CM		
	QA		
	PROG		

ANALOG DEVICES INC.

TITLE:

MICROCIRCUIT, LINEAR, RH1016M ULTRAFAST™ PRECISION 10ns COMPARATOR DICE

SIZE	CAGE CODE	DRAWING NUMBER	REV
	64155	**05-08-5242**	**D**

CONTRACT:

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1016M, DICE and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number: **RH1016M, Dice**

3.3 **Special Handling of Dice:** Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Analog Devices Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

ADI recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

Positive Supply Voltage (Note 5)	7V
Negative Supply Voltage	-7V
Differential Input Voltage (Note 7)	±5V
+IN,-IN and LATCH ENABLE Current (Note7)	±10mA
Output Current (Continuous) (Note 7)	±20mA
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec.)	300°C

3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.

3.7 Radiation Hardness Assurance (RHA):

3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.7.3 Total dose bias circuit is specified in **Figure 2**.

3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at Ta = +25°C to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.

3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ.**

3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.

4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.

5.0 SAMPLE ELEMENT EVALUATION: A sample from **each wafer supplying dice** shall be assembled and subjected to element evaluation per **Table III** herein.

5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.

5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in **Table I** and **Table II** herein.

5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.

5.4 Part Marking of Element Evaluation Sample Includes**:**

5.4.1 LTC Logo

5.4.2 LTC Part Number

5.4.3 Date Code

5.4.4 Serial Number

5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A

5.4.6 Diffusion Lot Number

5.4.7 Wafer Number

5.5 Burn-In Requirement: Burn-In circuit for 10 lead cerpac package is specified in **Figure 3**.

5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with **Figure 4.**

5.7 Terminal Connections: The terminal connections shall be as specified in **Figure 5.**

5.8 Lead Material and Finish: The lead material and finish shall be alloy 42 with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with **Table III** herein.

6.3 Screening: Screening requirements shall be in accordance with **Table III** herein.

6.3.1

6.4 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

6.4.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.

6.4.2 100% attributes (completed element evaluation traveler).

6.4.3 Element Evaluation variables data, including Burn-In and Op Life

6.4.4 SEM photographs (3.10 herein)

6.4.5 Wafer Lot Acceptance Report (3.9 herein)

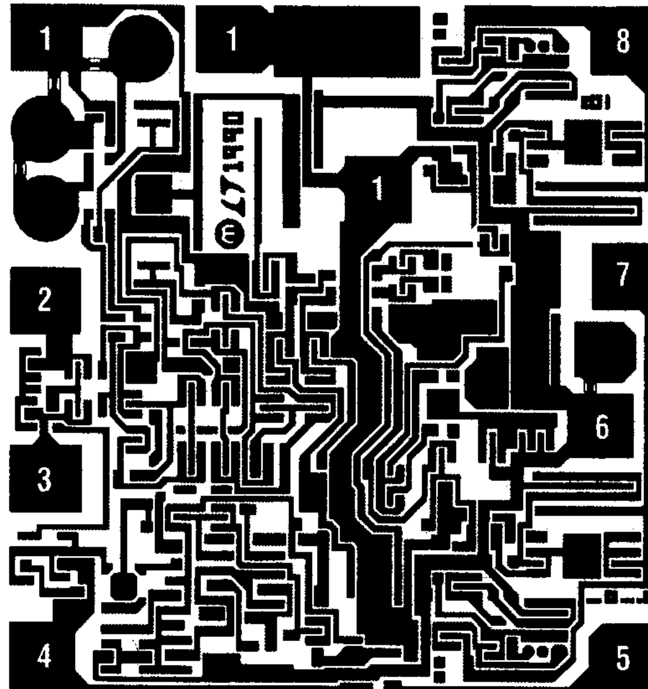
6.4.6 A copy of outside test laboratory radiation report if ordered

6.4.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6.4.1 and 6.4.7 will be delivered as a minimum, with each shipment.

7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS



PAD FUNCTION

1. V^+
2. +IN
3. –IN
4. V^-
5. LATCH ENABLE
6. GND
7. Q OUT
8. $\overline{Q}$ OUT

56mils × 58mils
Backside Connection is V^-

FIGURE 1

TOTAL DOSE BIAS CIRCUIT

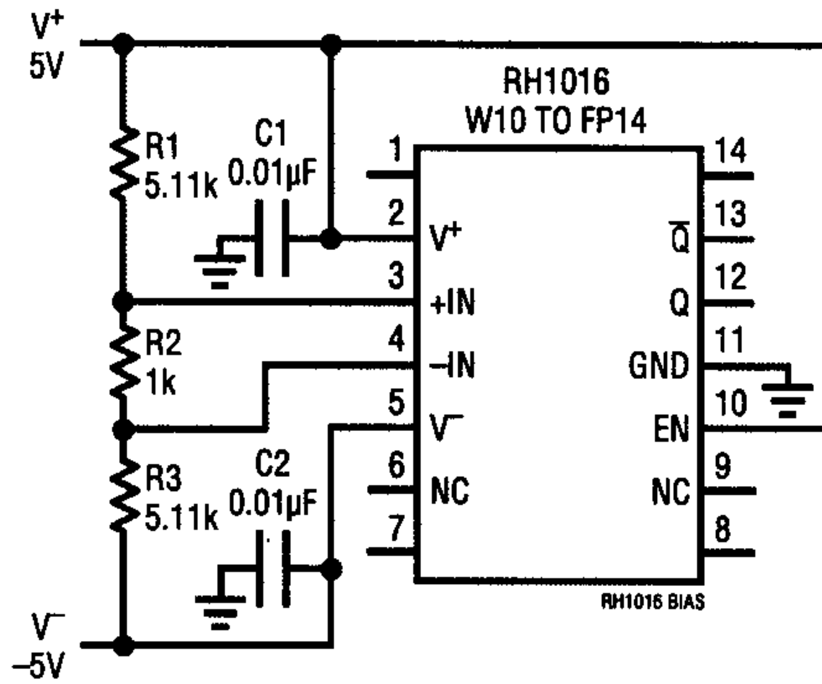
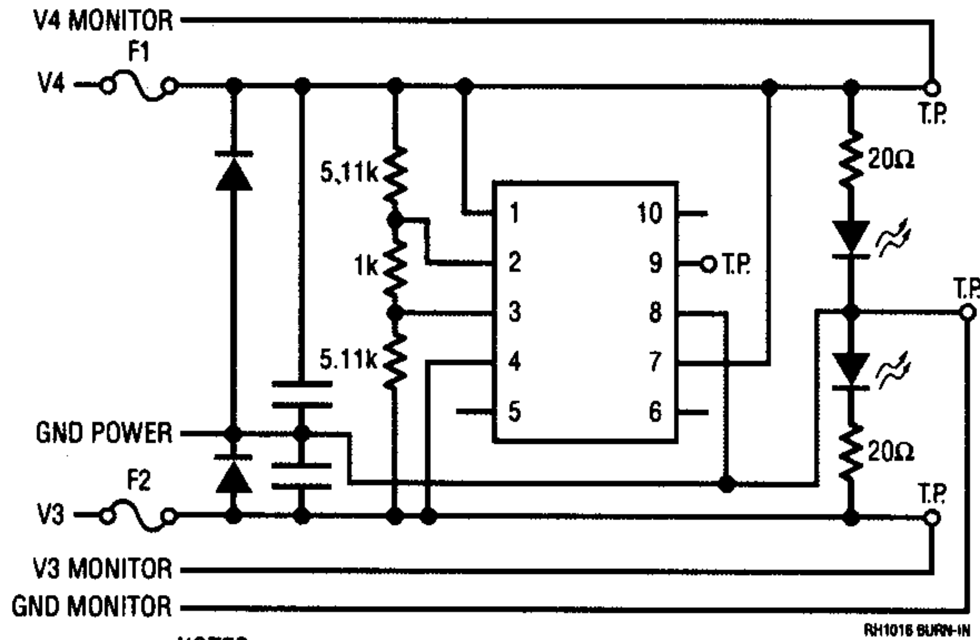


FIGURE 2

BURN-IN CIRCUIT

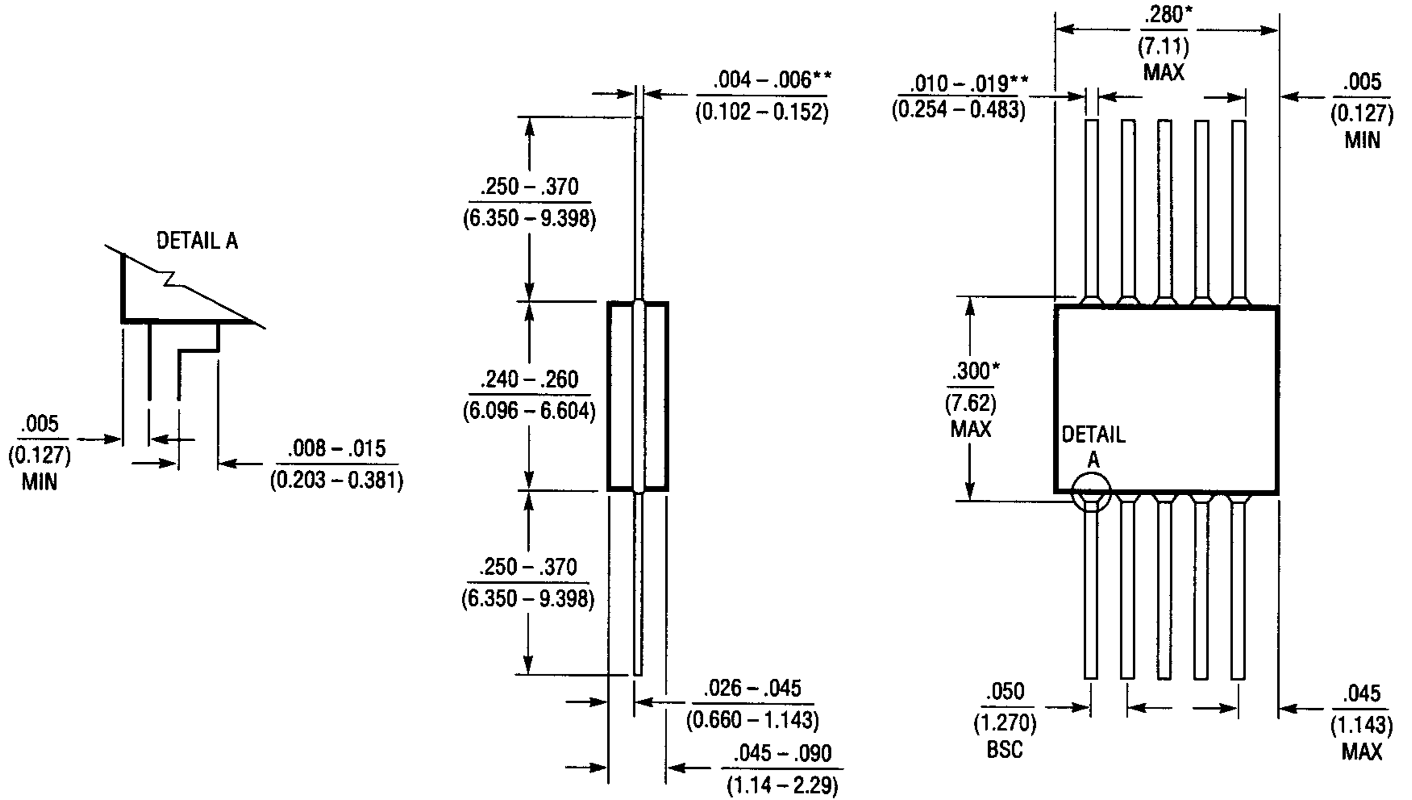


NOTES:
1. UNLESS OTHERWISE SPECIFIED, COMPONENT TOLERANCES SHALL BE PER MILITARY SPECIFICATION.
2. T_J = 161°C MAXIMUM
3. T_C = 139°C MINIMUM
4. T_A = 100°C MINIMUM

BURN-IN VOLTAGES: V4 = 5.5V TO 6V
V3 = –5.5V TO –6V

FIGURE 3

(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



θja = +170°C/W
θjc = +40°C/W

FIGURE 4

TERMINAL CONNECTIONS

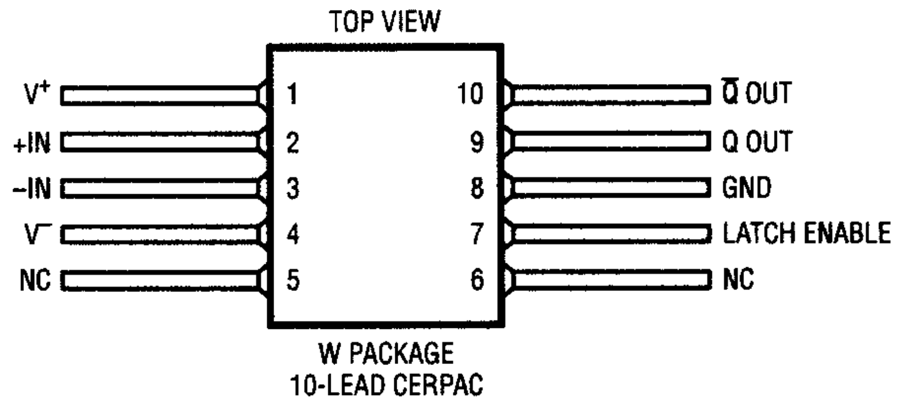


FIGURE 5

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation (Note 1)

T_A = 25°C. V^+ = 5V, V^- = –5V, $V_{OUT(Q)}$ = 1.4V, V_{LATCH} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$ (Note 1)		±3	mV
I_{OS}	Input Offset Current	(Note 1)		1	μA
I_B	Input Bias Current	(Note 2)		10	μA
	Input Voltage Range	(Note 3) Single 5V Supply (Note 3)	–3.75 1.25	3.5 3.5	V V
CMRR	Common Mode Rejection	$-3.75V \leq V_{CM} \leq 3.5V$	80		dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \leq V^+ \leq 5.4V$ Negative Supply $-7V \leq V^- \leq -2V$	60 80		dB dB
A_V	Small-Signal Voltage Gain	$1V \leq V_{OUT} \leq 2V$	1400		V/V
V_{OH}	Output High Voltage	$V^+ \geq 4.6V$, I_{OUT} = 1mA I_{OUT} = 10mA	2.80 2.60		V V
V_{OL}	Output Low Voltage	I_{SINK} = 4mA		0.5	V
I^+	Positive Supply Current			35	mA
I^-	Negative Supply Current			5	mA
V_{IH}	Latch Pin High Input Voltage		2.0		V
V_{IL}	Latch Pin Low Input Voltage			0.8	V
I_{IL}	Latch Pin Current	V_{LATCH} = 0V		500	μA

Note 1: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

Note 3: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization. See the LT1016 data sheet for discussion of input voltage range for supplies other than ±5V or 5V.

TABLE II ELECTRICAL CHARACTERISTICS – Post-Irradiation (Note 5)

(Postirradiation) T_A = 25°C, V^+ = 5V, V^- = –5V, $V_{OUT(Q)}$ = 1.4V, V_{LATCH} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$	2		±4		±4.5		±5		±5.5		±6	mV
I_{OS}	Input Offset Current		2		2		2.5		5		8		12	μA
I_B	Input Bias Current		3		12		12		14		17		20	μA
	Input Voltage Range		6	–3.75	3.5	–3.75	3.5	–3.75	3.5	–3.75	3.5	–3.75	3.5	V
		Single 5V Supply	6	1.25	3.5	1.25	3.5	1.25	3.5	1.25	3.5	1.25	3.5	V
CMRR	Common Mode Rejection Ratio	$-3.75V \le V_{CM} \le 3.5V$		80		77		74		70		65		dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \le V^+ \le 5.4V$		60		58		56		53		50		dB
		Negative Supply $-7V \le V^- \le -2V$		78		76		74		72		70		dB
A_V	Small-Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		1300		1200		1100		1000		900		V/V
V_{OH}	Output High Voltage	$V^+ \ge 4.6V$, I_{OUT} = 1mA		2.65		2.65		2.64		2.63		2.60		V
		I_{OUT} = 10mA		2.40		2.40		2.39		2.38		2.35		V
V_{OL}	Output Low Voltage	I_{SINK} = 4mA			0.55		0.55		0.56		0.57		0.6	V
I^+	Positive Supply Current				35		35		35		35		35	mA
I^-	Negative Supply Current				5		5		5		5		5	mA
I_{IL}	LATCH Pin Current	V_{LATCH} = 0V			525		575		650		725		800	μA
t_{PD}	Propagation Delay	ΔV_{IN} = 100mV, OD = 5mV	4		16		16		16		16		16	ns
		ΔV_{IN} = 100mV, OD = 20mV	4		14		14		14		14		14	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 3: Input bias current (I_B) is defined as the average of the two input currents.

Note 4: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The RH1016 is sample tested with a 1V step and 500mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} limits shown can be guaranteed with this test if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to overdrive.

Note 5: Electrical specifications apply only up to 5.4V.

Note 6: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization. See the LT1016 data sheet for discussion of input voltage range for supplies other than ±5V or 5V.

Note 7: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

TABLE III RH ELEMENT EVALUATION TABLE QUALIFICATION OF DICE SALES

RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS K/S	CLASS V	CLASS H/B	OPERATION	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY (ACCEPT NUMBER)
1	X	X		SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25°C)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
	X	X		BOND PULL MONITOR	2011		
5	X	X		STABILIZATION BAKE	1008	C	ASSEMBLED PARTS ONLY
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
	X	X		GROSS LEAK	1014	C	
6	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			45(0)
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125ºC or +150ºC, -55ºC			
	X	X		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs.	1015	+ 125ºc MINIMUM 240 HOURS	
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25ºC			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125ºC or +150ºC, -55ºC			
		X		TOTAL IRRADIATION DOSE	1019	A	
	X	X		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	X	X		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005	+ 125ºc MINIMUM 1000 HOURS	
	X	X		POST OP-LIFE ELECT. (R & R @ 25ºC, +125ºC OR +150ºC, -55ºC			
7	X	X	X	WIRE BOND EVALUATION	2011		15(0) OR 25(1) - # of wires

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Surgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.