REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/12/96
A	PAGE 18, TABLE II, DELETED VOS PARAMETER AND CHANGED +IB AND –IB DELTA LIMITS.	04/15/97
B	RELAXATION OF MAX VOS AT 25°C, FROM 180 µV to 300 µV, TABLE 1, PAGE 16; RELAXATION OF MAX VOS AT MIL TEMPERATURES, FROM 500 µV to 700 µV , TABLE IA, PAGE 17. LTC P/N'S CORRECTED, PAGE 2.	07/31/97
C	• PAGE 2, ADDED PARAGRAPHS 3.2.1, 3.2.2, 3.2.3. ADDED "(SEE PARAGRAPH 3.2) TO PARAGRAPH 3.3.b. • PAGE 3, ADDED PARAGRAPHS 3.8.1, 3.8.2, 3.8.3. • PAGE 4, PARAGRAPH 4.4.2, GROUP B INSPECTION WAS REDEFINED. • PAGE 5, PARAGRAPH 4.4.3, GROUP D INSPECTION WAS REDEFINED.	12/01/97
D	• PAGE 4, AMENDED PARAGRAPH 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES.	04/08/98
E	• CHANGED PACKAGE ON OPTION 3 FROM RH1056AMWB BOTTOM BRAZED FLATPACK TO RH1056AMW GLASS SEALED FLATPACK.	05/15/98
F	• PAGE 7,8,9, FIGURE 1,2,3 CHANGED 0JA AND 0JC.	09/28/99
G	• PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, 3.2.3 HAD FIGURES 1, 2, AND 3 REMOVED. • PAGE 4, PARAGRAPH 3.7, CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III" TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER "TABLE II", LINE 2. • PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE 11A OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-885". • PAGE 6, PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883'.	11/17/99

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
INDEX	REVISION	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T		
REVISION	PAGE NO.																	
INDEX	REVISION																	

				ANALOG DEVICES INC.
	ORIG			
	DSGN			TITLE:
	ENGR			**MICROCIRCUIT, LINEAR,**
	MFG			**RH1056A, PRECISION, HIGH SPEED, JFET**
	CM			**INPUT OPERATIONAL AMPLIFIER**
	QA			SIZE / CAGE CODE / DRAWING NUMBER / REV
	PROG			/ **64155** / **05-08-5019** / **U**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
H	• PAGE 9, CHANGED THETA JA TO 0JA=170°C/W AND THETA JC TO 0JC=40°C/W FROM 0JA=225°C/W AND 0JC=18°C/W PER PACKAGE ENGINEER.	09/05/00
J	• PAGE 3: PARAGRAPH 3.2.1 ADDED “OPTION 1”, PARAGRAPH 3.2.2, ADDED “OPTION 2”, PARAGRAPH 3.2.3, ADDED “OPTION 3”. • PAGE 4: PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.9, TABLE II CHANGED TO TABLE III. PARAGRAPH 3.10.3, ADDED “DEVICE OPTIONS 1, 2, AND 3” TO LINE 1. PARAGRAPH 3.11.1 WAS CHANGED FROM “…dosage rate of approximately 20 Rads per second” TO “…dosage rate of less than or equal to 10 Rads per second”. • PAGE 5: PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 7 THROUGH 16, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 8: CASE OUTLINE REVISED. LEAD DIMENSION CHANGED FROM .068 TO 0.065. • PAGE 9: CASE OUTLINE UPDATED TO MEET THE GUIDELINES OF MIL-STD-1835B. • PAGE 10, MOVED FIGURES 4, 5 AND 6 TO BETTER FIT THE PAGE. • PAGE 17, MOVED TABLES I AND II TO SAME PAGE. DATA SHEET REVISED: PRE-IRRAD TABLE I, VOS HAD A SUBGROUP CHANGE FROM SUBGROUP 1 TO SUBGROUP 4. NOTES WERE MADE NUMBERS INSTEAD OF ALPHAS FOR BOTH TABLE I AND TABLE II. • THIS SPECIFICATION IS NOW 18 PAGES INSTEAD OF 19 PAGES.	01/15/03
K	• PAGE 4, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/16/05
L	• PAGE 17, CHANGED SLEW RATE IN TABLE I AND TABLE II PER REVISED DATA SHEET.	09/19/06
M	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 • PAGE 4, PARAGRAPH 3.10.3 ADDED OPTION 3 IS ALLOY 42 FOR FLATPACK.	10/04/07
N	• PAGE 4, PARAGRAPH 3.10 3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT. PARAGRAPH 3.11.1 CHANGED VERBIAGE.	05/01/08
P	• PAGE 5, PARAGRAPH 4.4.2 CHANGED VERBIAGE. • PAGE 8, FIGURE 2 NOTE 2 ADDED TO LEAD THICKNESS. REMOVED THROUGH OUT SPEC RH1056AMJ8 OBSOLETE OPTION.	06/27/08
R	• PAGE 14, 15: CHANGED DATASHEET TABLE I $V_{OS,}$ & NOTES, AND TABLE 2; PAGE 15: TABLE IV, WIDENED V_{OS} LIMITS FOR B5, B6, D3, AND D4 (PER PRODUCT ENGINEER)	04/02/09
S	• PAGE 15, TABLE III, DELTA LIMIT REQUIREMENTS: CORRECTED +IB AND –IB DELTA MIN’S FROM -5.0 pA TO -50 pA AND DELTA MAX’S FROM 5.0 pA TO 50 pA.	5/10/10
T	• PAGE 8, ADDED θ_{ja} = +170°C/W and θ_{jc} = +40°C/W TO THE W10 CASE OUTLINE FOR THERMAL RESISTANCE.	01/31/11
U	• **TO CHANGE LINEAR TO ANALOG AND REMOVE SOURCE**	**3/23/21**

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1056A, PRECISION, HIGH SPEED, JFET INPUT OPERATIONAL AMPLIFIER, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH1056AMH (TO5 Metal Can, 8 Leads)

3.2.2 Option 2 – RH1056AMW (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage	±20V
Differential Input Voltage	±40V
Input Voltage	±20V
Output Short Circuit Duration	INDEFINITE
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and **Table II.**

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 5; Dynamic Burn-In, Figure 6

3.8.2 Option 2 (Glass Sealed Flatpack) : Static Burn-In / Dynamic Burn-In, Figure 7.

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 3, Figure 4.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar and options 2 are Alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 8.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1 Group B, Subgroup 2c = 10%
Group B, Subgroup 3 = 10%
Group B, Subgroup 4 = 5%
Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)
Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.5.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.5.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.5.3 Burn-In Variables Data and Deltas (if applicable)

4.5.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.5.5 Generic Group D data (4.4.3 herein)

4.5.6 SEM photographs (3.13 herein)

4.5.7 Wafer Lot Acceptance Report (3.13 herein)

4.5.8 X-Ray Negatives and Radiographic Report

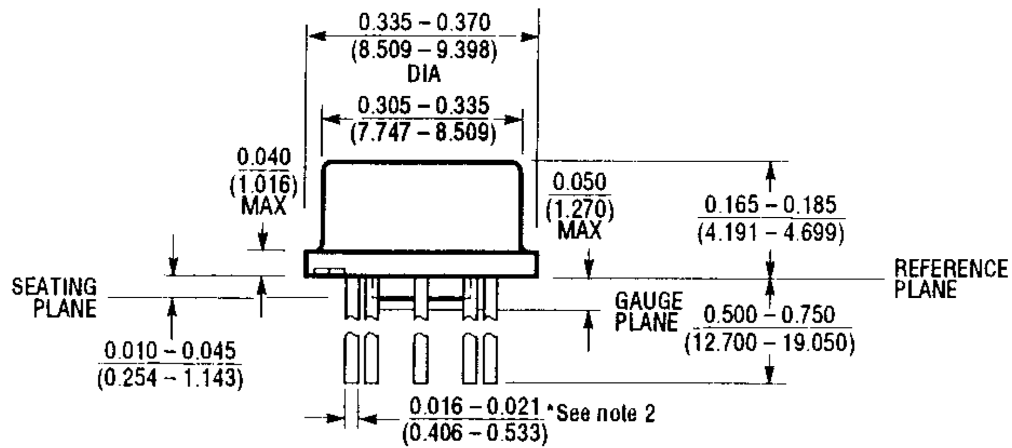
4.5.9 A copy of outside test laboratory radiation report if ordered

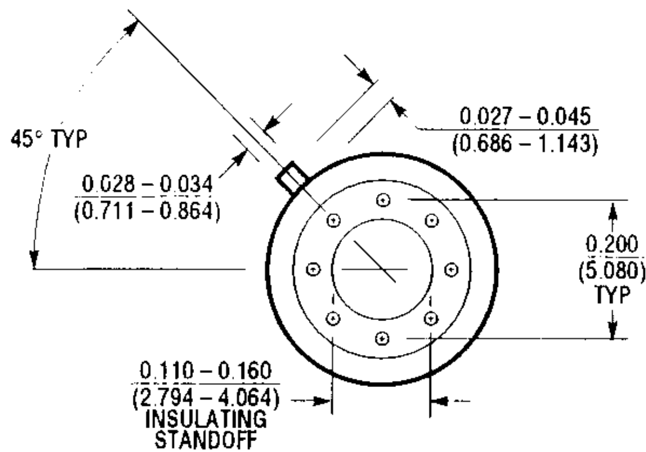
4.5.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.5.1 and 4.5.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as “No Charge Data”.

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1
(H) TO5 / 8 LEADS CASE OUTLINE





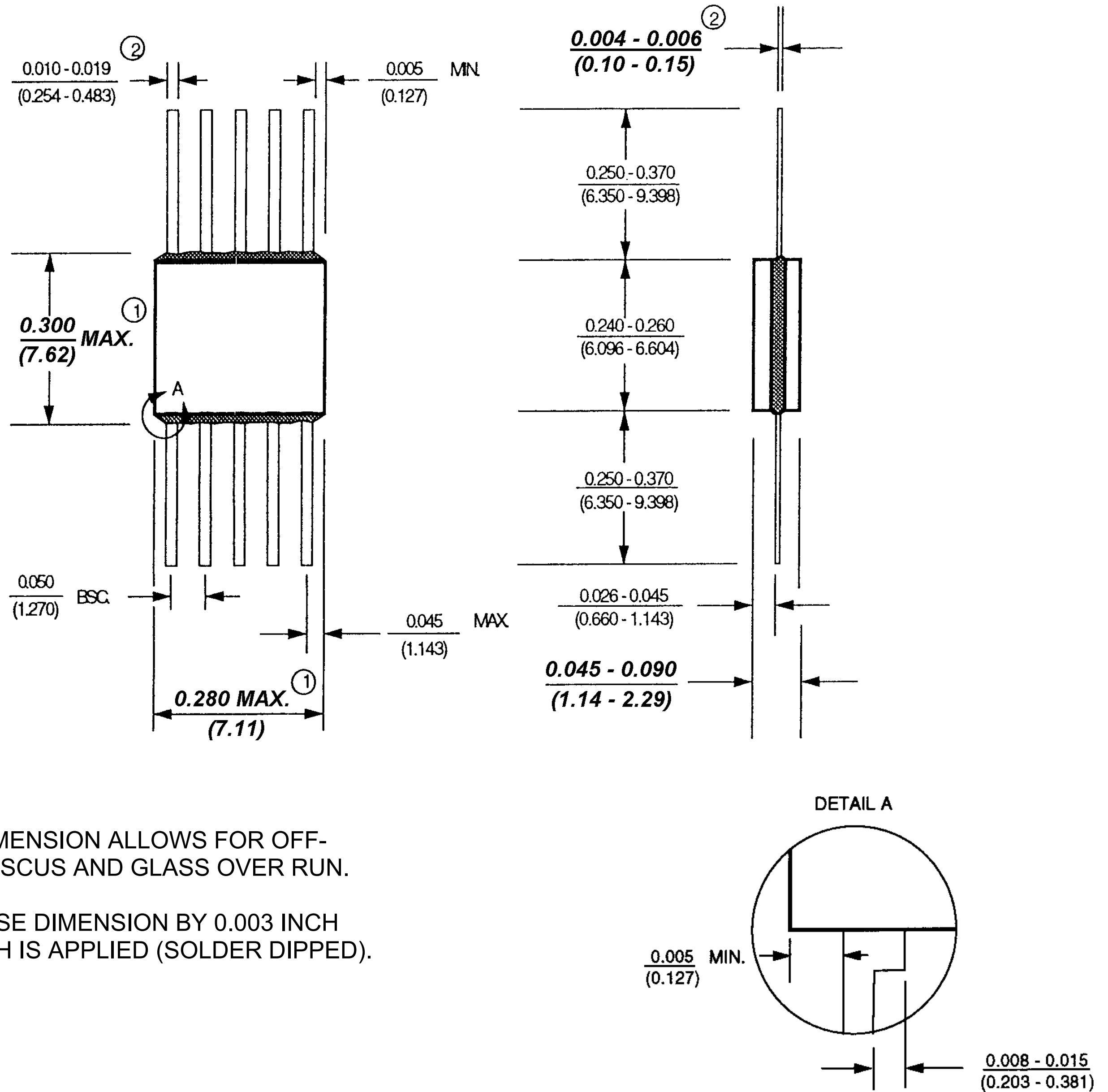
NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

θ_{ja} = +150°C/W

θ_{jc} = +40°C/W

FIGURE 1

DEVICE OPTION # 2
(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

θ_{ja} = +170°C/W

θ_{jc} = +40°C/W

FIGURE 2

TERMINAL CONNECTIONS

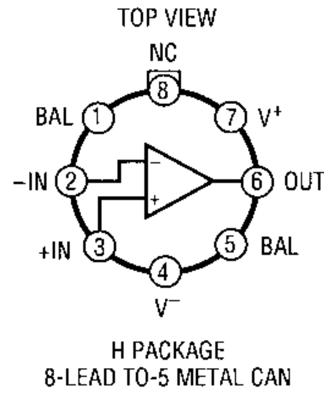


FIGURE 3

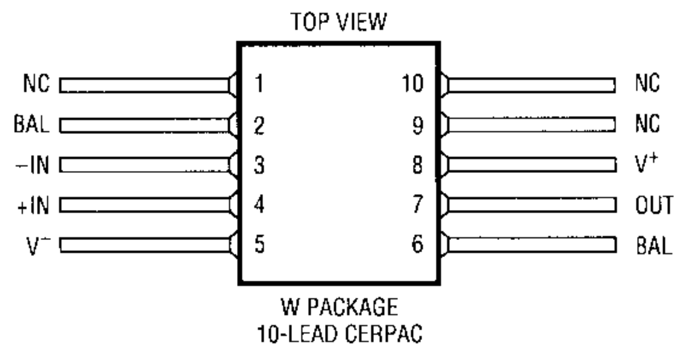
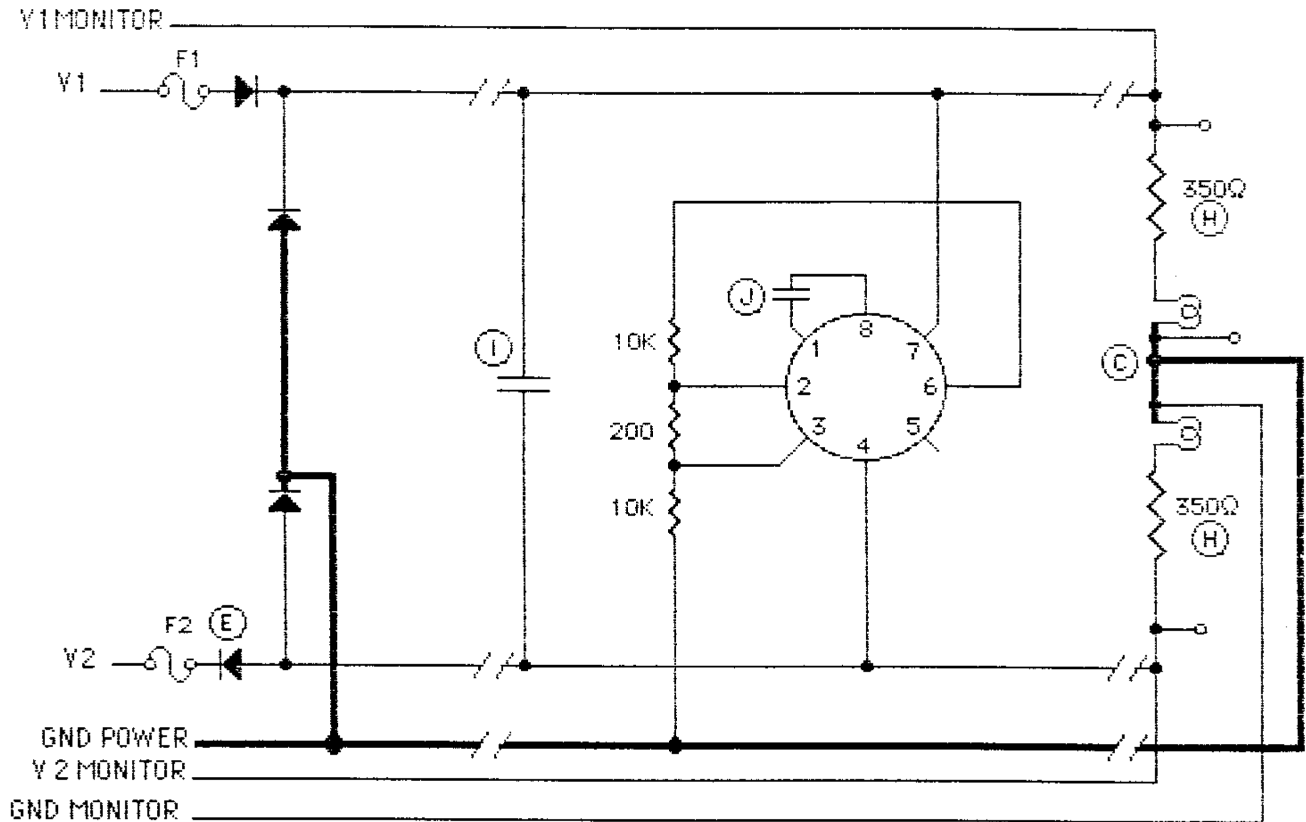


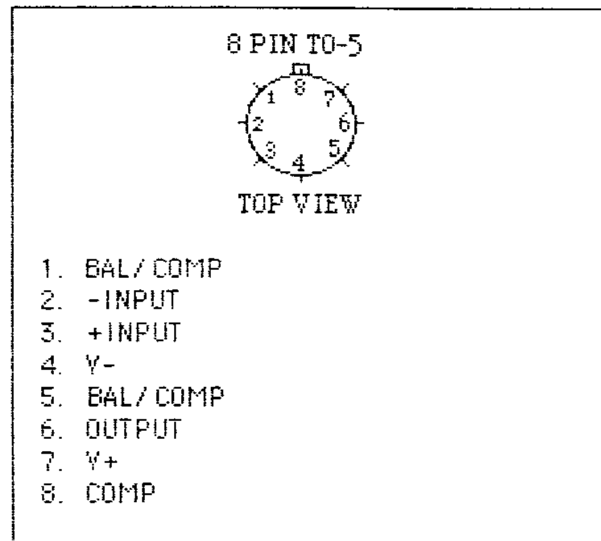
FIGURE 4

STATIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS



NOTES:

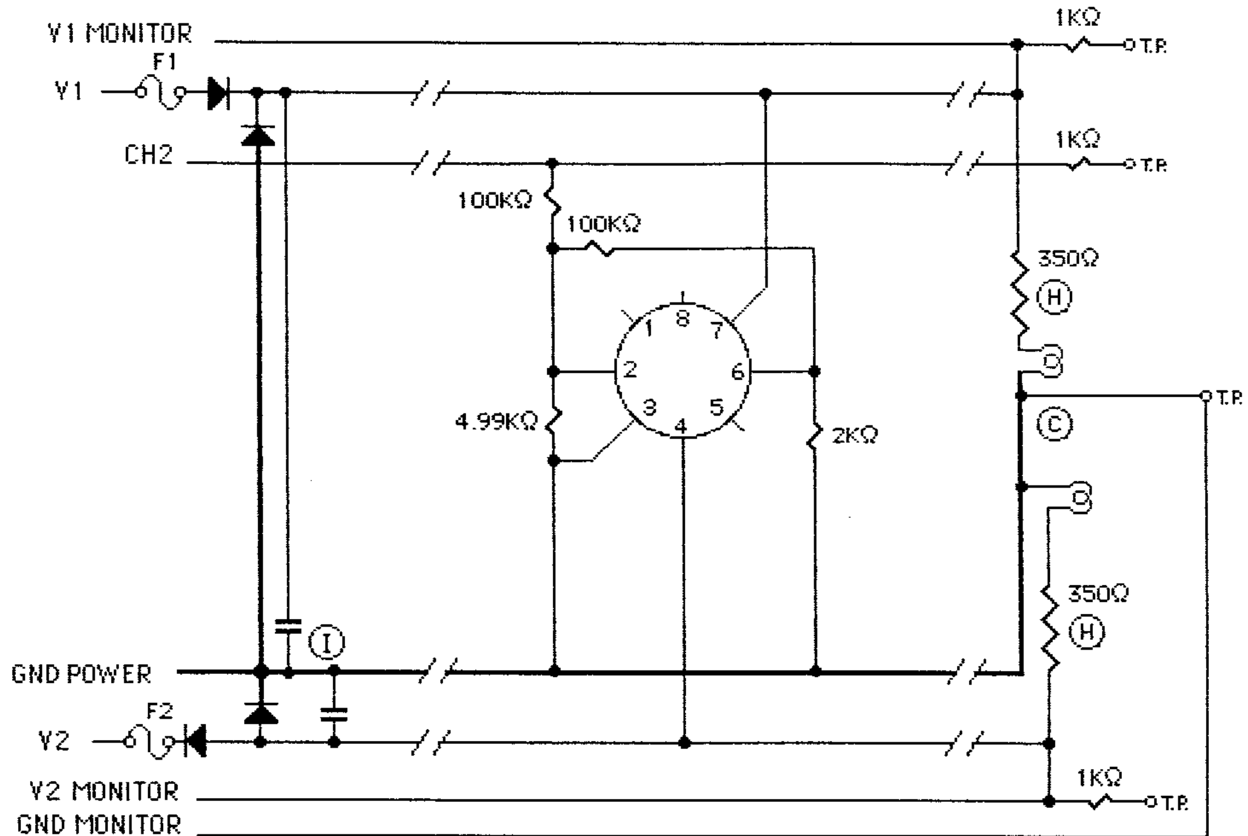
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj maximum = Varies with device being burned in.
3. Ta = 150 °C.
4. Burn-in voltages; V1 = +20V to +22V
   V2 = -20V to -22V



PACKAGE AND PINOUT

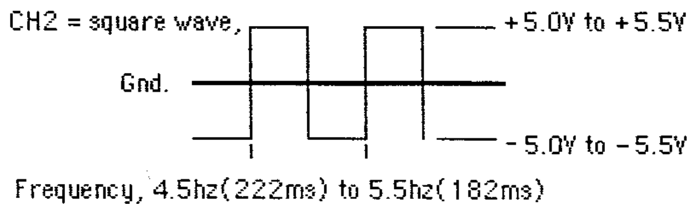
FIGURE 5

DYNAMIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS

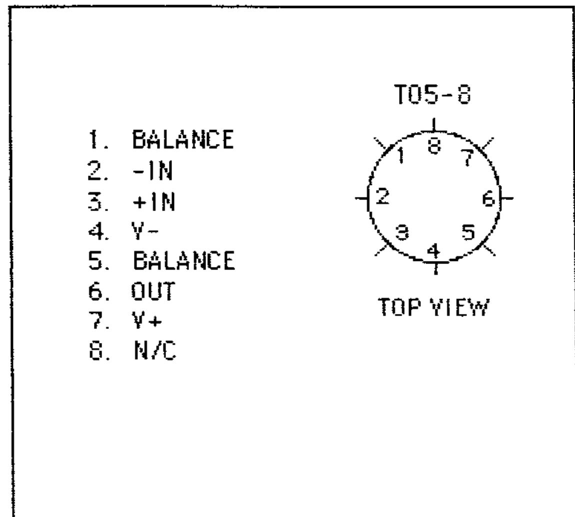


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 163 °C maximum.
3. Ta = 150 °C.
4. Burn-in Voltages:: V1 = + 20V to + 22V
   V2 = - 20V to - 22V



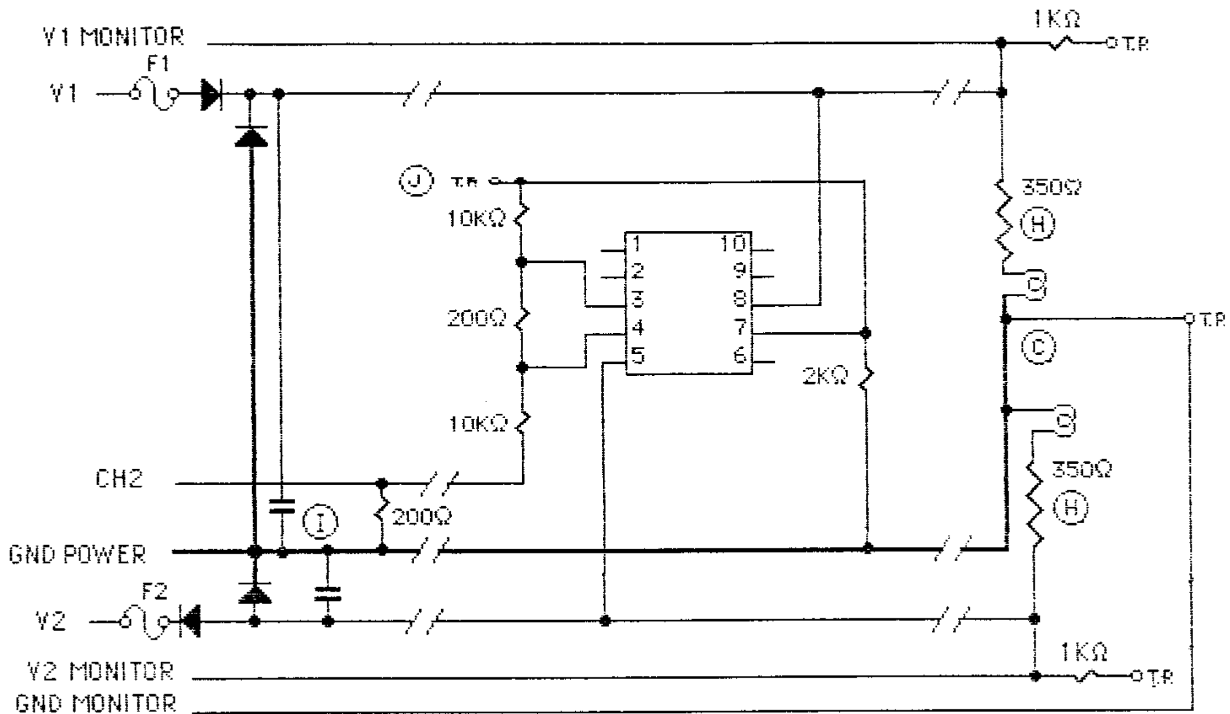
Frequency, 4.5hz(222ms) to 5.5hz(182ms)



PACKAGE AND PINOUT

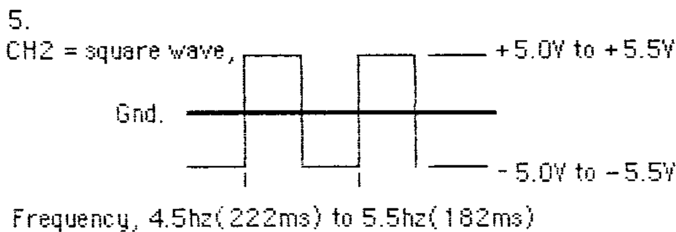
FIGURE 6

STATIC/DYNAMIC BURN-IN CIRCUIT
OPTION 2, GLASS SEALED FLATPACK / 10 LEAD

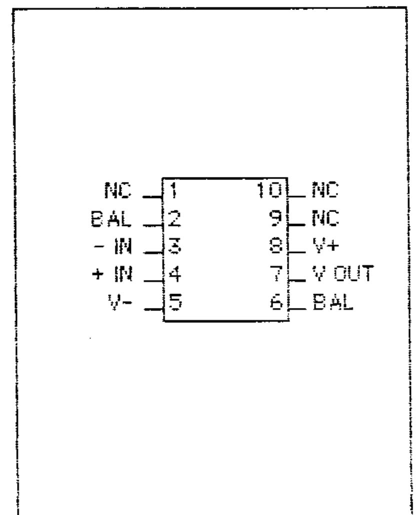


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 168 °C maximum.
3. Ta = 125 °C.
4. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V
5.



BOARD TO BE USED FOR BOTH STATIC AND DYNAMIC BURN-IN. ENSURE THAT CHANNEL TWO IS PRESENT FOR DYNAMIC BURN-IN. ENSURE THAT CHANNEL TWO IS NOT PRESENT FOR STATIC BURN-IN.



PACKAGE AND PINOUT

FIGURE 7

TOTAL DOSE BIAS CIRCUIT

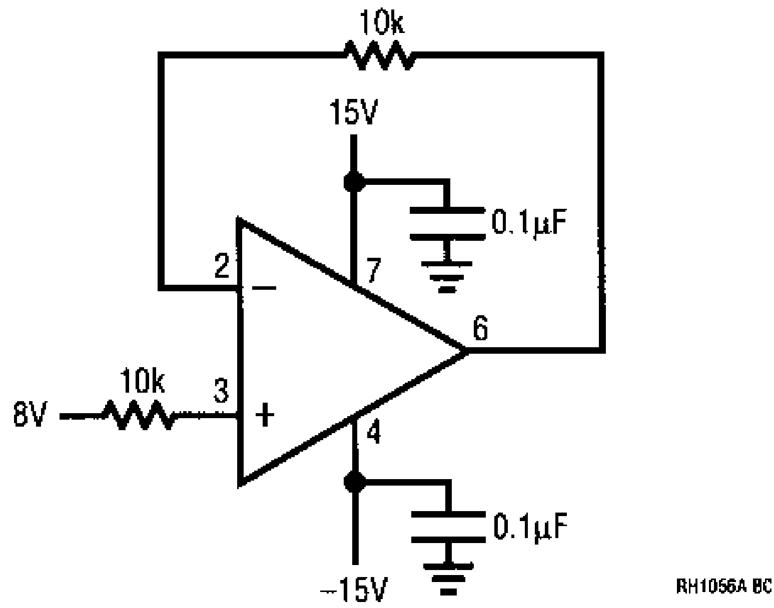


FIGURE 8

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE (3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_A \le 125°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage	RH1056AMW RH1056AMH	2			300 300	4 4			900 1100	2, 3 2, 3	µV µV
I_{OS}	Input Offset Current	Fully Warmed Up $T_A = 125°C$	4 4			10	1			 1.5	 2	pA nA
I_B	Input Bias Current	Fully Warmed Up $T_A = 125°C$	4			50	1			 3.0	 2	pA nA
R_{IN}	Input Resistance				10^{12}							Ω
A_{VOL}	Large-Signal Voltage Gain	$V_S = ±15V, V_O = ±10V, R_L = 2k$ $V_S = ±15V, V_O = ±10V, R_L = 1k$		150 130			4 4	40			5,6	V/mV V/mV
V_O	Output Voltage Swing	$V_S = ±15V, R_L = 2k$		±12			4	±12			5,6	V
V_{CM}	Input Common Mode Voltage Range	$V_S = ±15V$		±11			1	±11			2,3	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±11V$ $V_{CM} = ±10.5V$		86			1	 85			 2,3	dB dB
PSRR	Power Supply Rejection Ratio	$V_S = ±10V$ to $±18V$ $V_S = ±10V$ to $±17V$		90			1	 88			 2,3	dB dB
I_S	Supply Current	$V_S = ±15V$				6.5	1					mA
SR	Slew Rate	AV = 1, $V_S = ±15V$		10			7					V/µs
GBW	Gain-Bandwidth Product	$V_S = ±15V$			6.5							MHz
e_n	Input Noise Voltage Density	$V_S = ±15V$, f = 10Hz $V_S = ±15V$, f = 1kHz			28 14							fA/√Hz fA/√Hz
i_n	Input Noise Current Density	$V_S = ±15V$, f = 10Hz $V_S = ±15V$, f = 1kHz			1.8 1.8							fA/√Hz fA/√Hz
C_{IN}	Input Capacitance				4				4			pF

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE (5)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si) MIN	MAX	20KRAD (Si) MIN	MAX	50KRAD (Si) MIN	MAX	100KRAD (Si) MIN	MAX	200KRAD (Si) MIN	MAX	UNITS
V_{OS}	Input Offset Voltage		2		300		300		370		570		870	µV
I_{OS}	Input Offset Current		4		±10		±50		±150		±250		±350	pA
I_B	Input Bias Current		4		±50		±250		±500		±1000		±2000	pA
A_{VOL}	Large-Signal Voltage Gain	$V_O = ±10V, R_L \ge 2k$ $V_O = ±10V, R_L \ge 1k$		150 130		150 130		150 130		100 87		75 65		V/mV V/mV
V_O	Output Voltage Swing	$R_L \ge 2k$		±12		±12		±12		±12		±12		V
V_{CM}	Input Common Mode Voltage Range	$V_S = ±15V$		±11		±11		±11		±11		±11		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±11V$		86		86		86		86		86		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±10V$ to $±18V$		90		90		90		90		90		dB
I_S	Supply Current				7		7		7		7		7	mA
SR	Slew Rate	$A_V = 1, V_S = ±15V$		10		10		9		9		9		V/µs
C_{IN}	Input Capacitance			3(Typ)		3(Typ)		3(Typ)		3(Typ)		3(Typ)		pF

ALL NOTES FOR THE ELECTRICAL CHARACTERISTICS ARE ON THE NEXT PAGE (15).

TABLE I AND TABLE II ELECTRICAL CHARACTERISTICS NOTES

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage. Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power, (b) at T_A = 25°C only, with the chip heated to approximately 45°C to account for chip temperature rise when the device is fully warmed up.

Note 3: Unless otherwise stated, V_S = ±15V; and V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0V.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + (\theta_{JA} \bullet P_D)$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 5: Unless otherwise stated, V_S = ±15V, V_{CM} = 0V and T_A = 25°C.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
$+I_B$	-50	50	**-50**	**50**	pA
$-I_B$	-50	50	**-50**	**50**	pA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6, 7
Group A Test Requirements (Method 5005)	1,2,3,4,5,6, 7
Group B and D for Class S, and Class C and D for Class B** End Point Electrical Parameters (Method 5005)	1

*PDA applies to subgroup 1. See PDA Test Notes.
**For D3, D4, B5 and B6 V_{OS} Limit as follows

W Package	H Package
500µV	700µV

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.