REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	09/16/06
A	• PAGE 3, PARAGRAPH 3.7.1 CHANGED VERBIAGE. • PAGE 4, PARAGRAPH 5.8 CHANGED ALLOY 42 TO KOVAR REQUIRED FOR TO5 PACKAGE.	05/06/08
B	• PAGE 12, TABLE II WAS AMENDED DUE TO DATA SHEET CHANGE. • PAGE 13, TABLE III WAS CHANGED FOR QUALIFYING DICE SALES ADDED TEMPERATURE CYCLE, CONSTANT ACCELERATION & REMOVED PIND TEST.	04/01/09
C	Page 2, amended section 3.3, Special Handling of Dice, to more accurately describe our current procedures and requirements.	03/30/12
D	Page 13, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from "15%" to "10%".	07/02/13
E	Updated Die Sales table on pg 13.	6/1/15
F	To remove SI and to change Linear to Analog.	2/19/21

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13			
INDEX	REVISION	F	F	F	F	F	F	F	F	F	F	F	F	F			
REVISION	PAGE NO.																
INDEX	REVISION																

				ANALOG DEVICES INC.			
	ORIG						
	DSGN			TITLE: MICROCIRCUIT, LINEAR, RH1056A PRECISION HIGH SPEED JFET INPUT OPERATIONAL AMPLIFIER DICE			
	ENGR						
	MFG						
	CM						
	QA			SIZE	CAGE CODE	DRAWING NUMBER	REV
	PROG				64155	05-08-5212	F
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:			

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1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1056A, DICE and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number: RH1056A, Dice,

3.3 Special Handling of Dice: Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Analog Devices Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

ADI recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

Supply Voltage	±20V
Differential Input Voltage	±40V
Input Voltage	±20V
Output Short Circuit Duration	INDEFINITE
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in Figure 1.

3.7 Radiation Hardness Assurance (RHA):

3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.7.3 Total dose bias circuit is specified in Figure 2.

3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at Ta = +25°C to the limits shown in Table I herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.

3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a minimum of 4KÅ.

3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.

4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.

5.0 SAMPLE ELEMENT EVALUATION: A sample from each wafer supplying dice shall be assembled and subjected to element evaluation per Table III herein.

5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.

5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in Table I and Table II herein.

5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.

5.4 Part Marking of Element Evaluation Sample Includes:

5.4.1 LTC Logo

5.4.2 LTC Part Number

5.4.3 Date Code

5.4.4 Serial Number

5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A

5.4.6 Diffusion Lot Number

5.4.7 Wafer Number

5.5 Burn-In Requirement: Burn-In circuit for TO5 package is specified in Figure 3.

5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with Figure 4.

5.7 Terminal Connections: The terminal connections shall be as specified in Figure 5.

5.8 Lead Material and Finish: The lead material and finish shall be Kovar with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with Table III herein.

6.3 Screening: Screening requirements shall be in accordance with Table III herein.

6.4 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

6.4.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.

6.4.2 100% attributes (completed element evaluation traveler).

6.4.3 Element Evaluation variables data, including Burn-In and Op Life

6.4.4 SEM photographs (3.10 herein)

6.4.5 Wafer Lot Acceptance Report (3.9 herein)

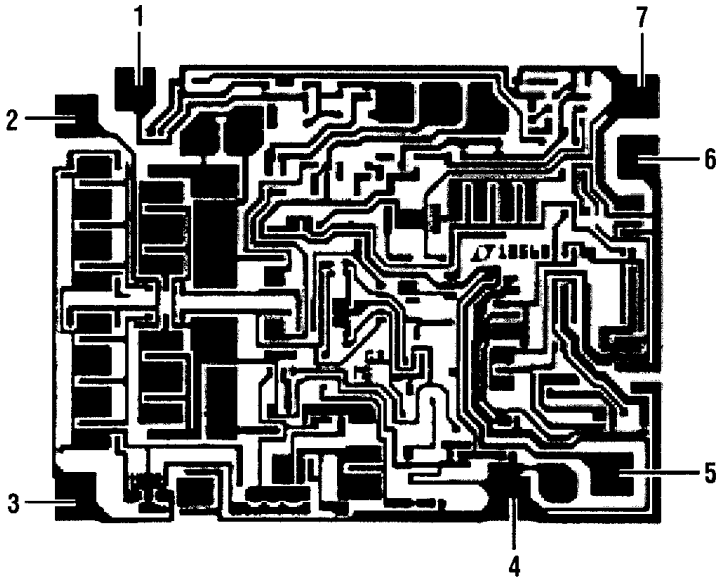
6.4.6 A copy of outside test laboratory radiation report if ordered

6.4.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6. 4.1 and 6. 4.7 will be delivered as a minimum, with each shipment.

7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS



59mils × 78mils,
Backlap: 12mils
Backside (substrate) is an alloyed gold layer.

PAD FUNCTION

1. BALANCE
2. – IN
3. + IN
4. V^-
5. BALANCE
6. OUT
7. V^+

FIGURE 1

TOTAL DOSE BIAS CIRCUIT

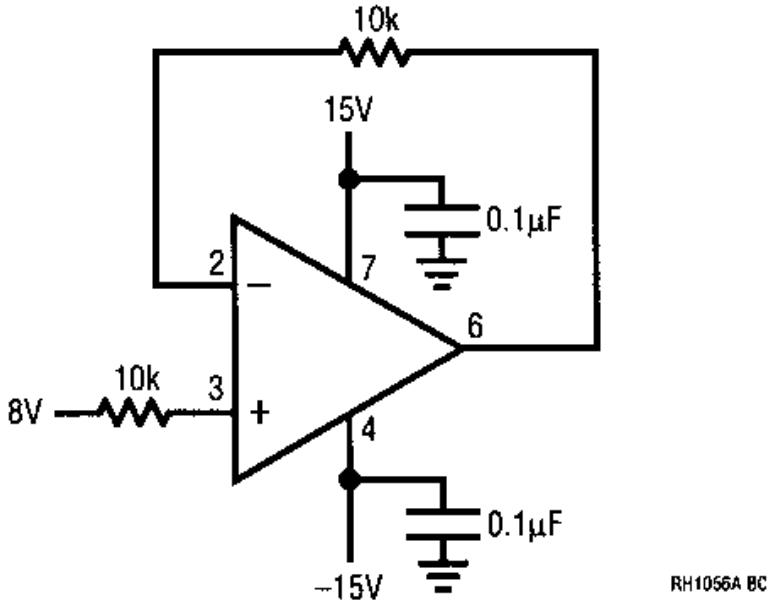
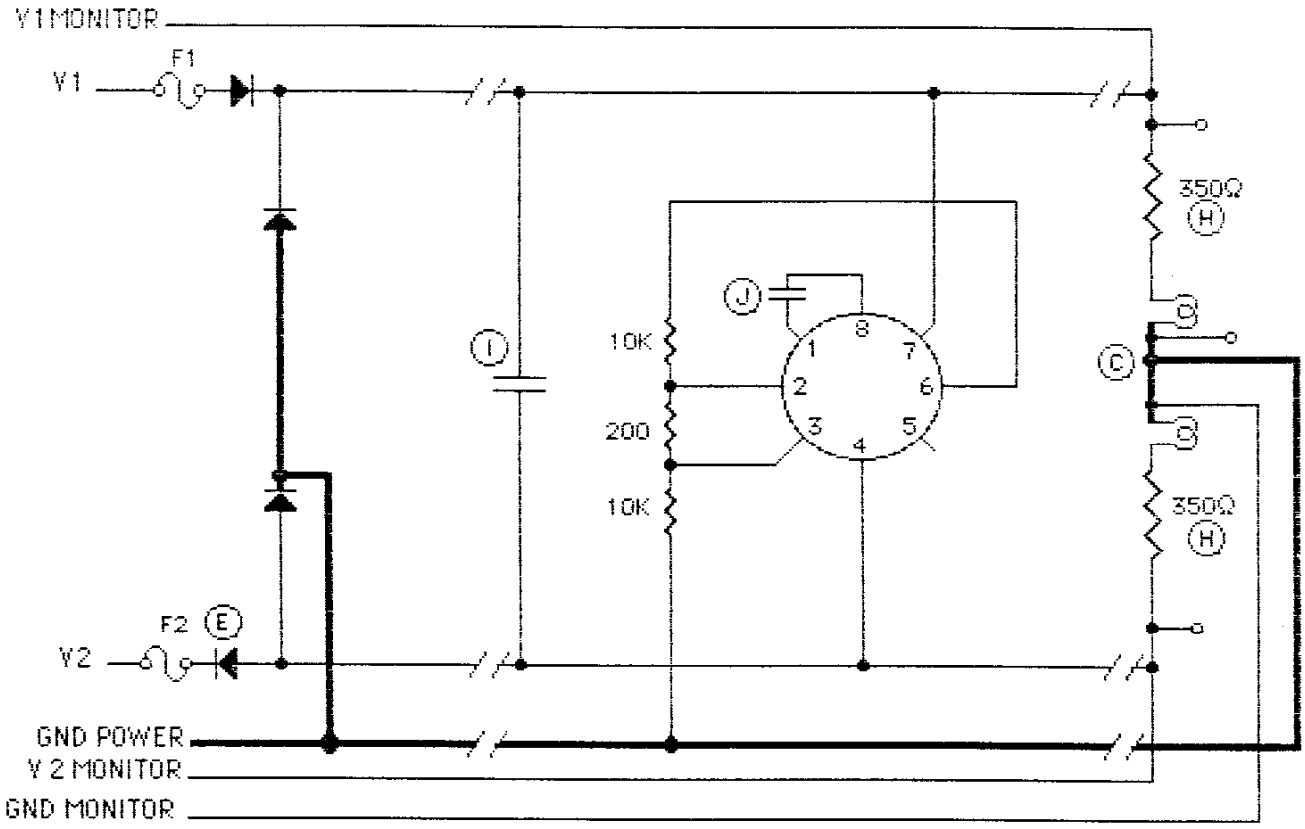


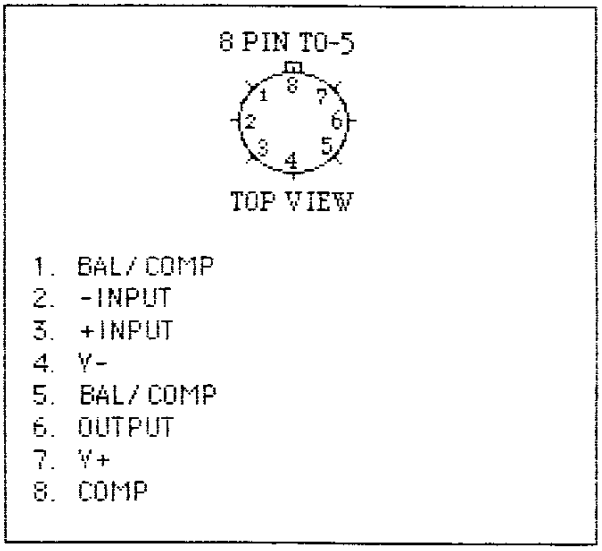
FIGURE 2

BURN-IN CIRCUIT TO5, METAL CAN 8 LEAD



NOTES:

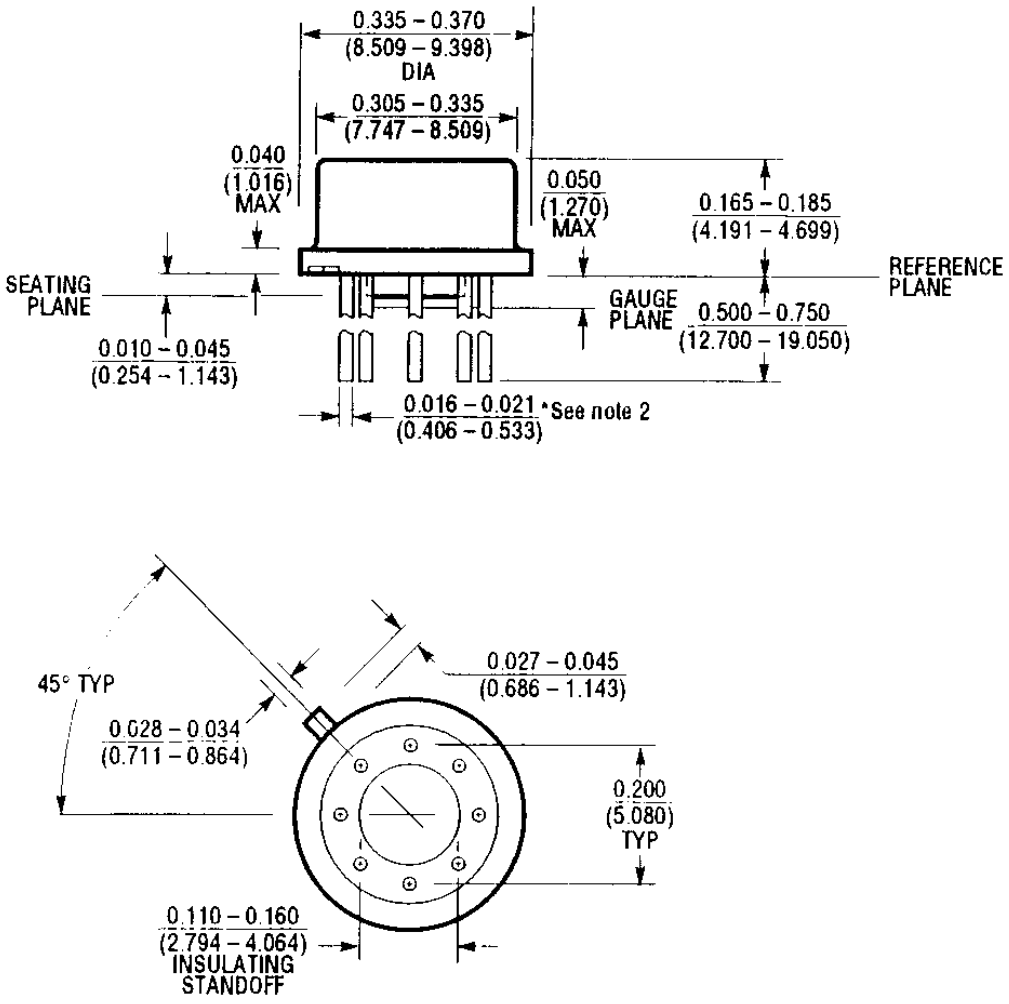
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj maximum = Varies with device being burned in.
3. Ta = 150 °C.
4. Burn-in voltages; V1 = +20V to +22V
   V2 = -20V to -22V



PACKAGE AND PINOUT

FIGURE 3

TO5, 8 LEADS, CASE OUTLINE

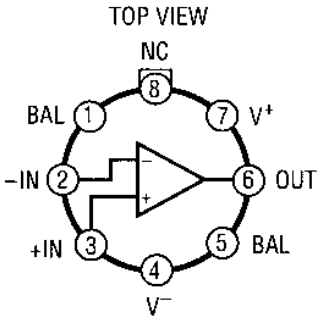


NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

FIGURE 4

θja = +150°C/W
θjc = +40°C/W

TERMINAL CONNECTIONS



H PACKAGE
8-LEAD TO-5 METAL CAN

FIGURE 5

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 3)		0.5	mV
I_{OS}	Input Offset Current	(Note 4)		50	pA
I_B	Input Bias Current	(Note 4)		200	pA
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 2k	120		V/mV
V_{OUT}	Output Voltage Swing	R_L = 2k, V_S = ±15V	±12		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V, V_S = ±15V	86		dB
PSRR	Power Supply Rejection Ratio	VS = ±10V to ±18V	88		dB
SR	Slew Rate	(Note 5)	10		V/µs
I_S	Supply Current			6	mA

Note 1: Dice are probe tested at 25°C to the limits shown. Final specs, after assembly cannot be guaranteed at the die level due to yield loss and assembly shifts. For absolute maximum ratrings, typical specifications, performance curves and finished product specifications, please refer to the standard product data sheet.

Note 2: For dice tested to tighter limits than those listed above and/or, lot qualification based on sample lot assembly and testing, please contact LTC Marketing.

Note 3: V_S = ±15V, T_A = 25°C, V_{CM} = 0V, unless otherwise noted.

Note 4: This is not a reflection of actual I_{OS} and I_B. Typical values are 5pA and 20pA respectively at final test. JFETs sensitivity to light at wafer sort requires a loose limit.

Note 5: Tested at a gain of "5".

TABLE II ELECTRICAL CHARACTERISTICS – Post-Irradiation (Note 5)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si) MIN	10KRAD (Si) MAX	20KRAD (Si) MIN	20KRAD (Si) MAX	50KRAD (Si) MIN	50KRAD (Si) MAX	100KRAD (Si) MIN	100KRAD (Si) MAX	200KRAD (Si) MIN	200KRAD (Si) MAX	UNITS
V_{OS}	Input Offset Voltage		2		300		300		370		570		870	µV
I_{OS}	Input Offset Current		4		±10		±50		±150		±250		±350	pA
I_B	Input Bias Current		4		±50		±250		±500		±1000		±2000	pA
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V, $R_L \geq 2k$ V_O = ±10V, $R_L \geq 1k$		150 130		150 130		150 130		100 87		75 65		V/mV V/mV
V_O	Output Voltage Swing	$R_L \geq 2k$		±12		±12		±12		±12		±12		V
V_{CM}	Input Common Mode Voltage Range	V_S = ±15V		±11		±11		±11		±11		±11		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V		86		86		86		86		86		dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±18V		90		90		90		90		90		dB
I_S	Supply Current				7		7		7		7		7	mA
SR	Slew Rate	A_V = 1, V_S = ±15V		10		10		9		9		9		V/µs
C_{IN}	Input Capacitance			3(Typ)		3(Typ)		3(Typ)		3(Typ)		3(Typ)		pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage. Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power, (b) at T_A = 25°C only, with the chip heated to approximately 45°C to account for chip temperature rise when the device is fully warmed up.

Note 3: Unless otherwise stated, V_S = ±15V; and V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0V.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + (\theta_{JA} \bullet P_D)$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 5: Unless otherwise stated, V_S = ±15V, V_{CM} = 0V and T_A = 25°C.

LINEAR TECHNOLOGY

RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS K/S	CLASS V	CLASS H/B	OPERATION	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY (ACCEPT NUMBER)
1	X	X		SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25ºC)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
	X	X		BOND PULL MONITOR	2011		
5	X	X		STABILIZATION BAKE	1008	C	ASSEMBLED PARTS ONLY
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
	X	X		GROSS LEAK	1014	C	
6	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			45(0)
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125ºC or +150ºC, -55ºC			
	X	X		BURN-IN: +125ºC/240 hrs. or +150ºC/120 hrs.	1015	+ 125ºc MINIMUM 240 HOURS	
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25ºC			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125ºC or +150ºC, -55ºC			
		X		TOTAL IRRADIATION DOSE	1019	A	
	X	X		PRE OP-LIFE ELECTRICAL @ 25ºC READ & RECORD			
	X	X		OPERATING LIFE: +125ºC/1000 hrs. or +150ºC/500 hrs.	1005	+ 125ºc MINIMUM 1000 HOURS	
	X	X		POST OP-LIFE ELECT. (R & R @ 25ºC, +125ºC OR +150ºC, -55ºC			
7	X	X	X	WIRE BOND EVALUATION	2011		15(0) OR 25(1) - # of wires

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Surgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.