REVISION RECORD

REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/14/96
A	• PAGE 2, ADDED PARAGRAPHS 3.2.1, 3.2.2, AND 3.2.3. PARAGRAPH 3.3.b: ADDED "(SEE PARAGRAPH 3.2)". • PAGE 3, ADDED PARAGRAPHS 3.8.1, 3.8.2, AND 3.8.3. PARAGRAPH 3.10.3, OPTION 3, REDEFINED. PARAGRAPH 3.12: WAFER LOT ACCEPTANCE REDEFINED. • PAGE 4, PARAGRAPH 4.4.2, GROUP B INSPECTION WAS REDEFINED. PARAGRAPH 4.4.3, GROUP D INSPECTION WAS REDEFINED. PARAGRAPH 4.5, SOURCE INSPECTION, REDEFINED. • PAGE 6, FIGURES 1, TO5 CASE OUTLINES, ADDED θja AND θjc. • PAGE 7, FIGURE 2, CERDIP CASE OUTLINES, ADDED θja AND θjc. • PAGE 8, FIGURE 3, BB FLATPACK CASE OUTLINES, ADDED θja AND θjc. • PAGE 16, TABLE IA, ELECTRICAL CHARACTERISTICS, (POST-IRRADIATION) CHANGE AVOL FOR 10K RAD FROM "100V/mV" TO "1000V/mV". CHANGE VOUT UNIT FROM "mV" TO "V".	12/01/97
B	• PAGE 4, AMENDED PARAGRAPH 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES.	04/08/98
C	• CHANGED OPTION 3 TO RH1078MW (GLASS SEAL FLATPACK 10 LEAD)	02/08/99
D	• PAGE 6,7,8, FIGURE 1,2,3, CHANGED θJA AND θJC.	09/24/99
E	• PAGE 3, PARAGRAPH 3.2.1, 3.2.2, 3.2.3 HAD FIGURES 1, 2, AND 3 REMOVED. • PAGE 4, PARAGRAPH 3.7, CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER "TABLE II", LINE 2. • PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IIA OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-883". PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883".	01/04/00

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
INDEX	REVISION	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**	**K**
REVISION	PAGE NO.	18																
INDEX	REVISION	**K**																

APPLICATION	FUNCT	SIGNOFFS	DATE
	ORIG		
	DSGN		
	ENGR		
	MFG		
	CM		
	QA		
	PROG		

ANALOG DEVICES INC.

TITLE:
MICROCIRCUIT, LINEAR, RH1078M, MICROPOWER, DUAL, SINGLE SUPPLY PRECISION OP AMP

SIZE	CAGE CODE	DRAWING NUMBER	REV
	64155	**05-08-5020**	**L**

CONTRACT:

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
F	• PAGE 9, CHANGED THETA JA TO ΘJA=170°C/W AND THETA JC TO ΘJC=40°C/W FROM ΘJA=225°C/W AND ΘJC=18°C/W PER PACKAGE ENGINEER.	09/05/00
G	• PAGE 3: PARAGRAPH 3.2.1 ADDED “OPTION 1”, PARAGRAPH 3.2.2, ADDED “OPTION 2”, PARAGRAPH 3.2.3, ADDED “OPTION 3”. • PAGE 4: PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.9, TABLE II CHANGED TO TABLE III. PARAGRAPH 3.10.3, ADDED “DEVICE OPTIONS 1, 2, AND 3” TO LINE 1. PARAGRAPH 3.11.1 WAS CHANGED FROM “…dosage rate of approximately 20 Rads per second” TO “…dosage rate of less than or equal to 10 Rads per second”. • PAGE 5: PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 7 THROUGH 17, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 8: CASE OUTLINE REVISED. LEAD DIMENSION CHANGED FROM .068 TO 0.065. • PAGE 9: CASE OUTLINE UPDATED TO MIL-STD-1835. • PAGE 10, MOVED FIGURES TO BETTER FIT THE PAGE. • PAGE 11, CORRECTED THE TO5 BURN-IN CIRCUIT’S T_J TO +134°C MAXIMUM, AND T_A TO +125°C. • PAGE 12, CORRECTED THE CERDIP BURN-IN CIRCUIT’S T_J TO +134°C MAXIMUM, AND T_A TO +125°C. REPLACED DYNAMIC CIRCUIT WITH STATIC. • PAGE 13 REPLACED DYNAMIC ONLY CIRCUIT WITH STATIC / DYNAMIC.	05/14/03
H	• PAGE 4, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/15/05
J	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 • PAGE 4, PARAGRAPH 3.10.3 ADDED OPTION 3 IS ALLOY 42 FOR FLATPACK.	10/04/07
K	• PAGE 4 PARAGRAPH 3.10.3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT. PARAGRAPH 3.11.1 CHANGED VERBIAGE.	5/1/08
L	• **TO CHANGE LINEAR TO ANALOG AND REMOVE SOURCE**	**3/23/21**

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1078M, MICROPOWER, DUAL, SINGLE SUPPLY PRECISION OP AMP, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH1078MH (TO5 Metal Can, 8 Leads)

3.2.2 Option 2 – RH1078MJ8 (Ceramic Dip, 8 Leads)

3.2.3 Option 3 – RH1078MW (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage . . . . $\pm$22V
Differential Input Voltage . . . . $\pm$30V
Input Voltage . . . . Equal to Positive Supply Voltage
. . . . 0.5v Below Negative Supply Voltage
Output Short Circuit Duration . . . . Indefinite
Operating Temperature Range . . . . -55°C to +125°C
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and **Table II.**

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 7;

3.8.2 Option 2 (Ceramic Dip): Static Burn-In, Figure 8;

3.8.3 Option 3 (Glass Sealed Flatpack) : Static/Dynamic Burn-In, Figure 9;

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar and options 2, 3 are Alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 10.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1 Group B, Subgroup 2c = 10%
Group B, Subgroup 3 = 10%
Group B, Subgroup 4 = 5%
Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)
Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each

assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.5.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.5.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.5.3 Burn-In Variables Data and Deltas (if applicable)

4.5.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.5.5 Generic Group D data (4.4.3 herein)

4.5.6 SEM photographs (3.13 herein)

4.5.7 Wafer Lot Acceptance Report (3.13 herein)

4.5.8 X-Ray Negatives and Radiographic Report

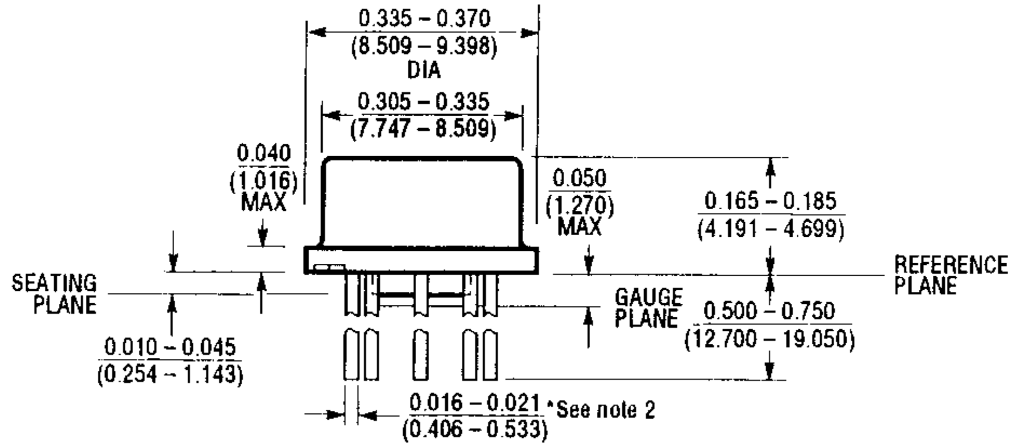
4.5.9 A copy of outside test laboratory radiation report if ordered

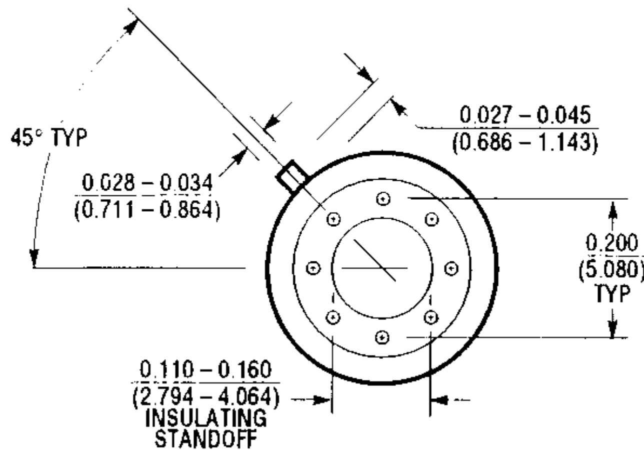
4.5.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.5.1 and 4.5.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1
(H) TO5 / 8 LEADS CASE OUTLINE





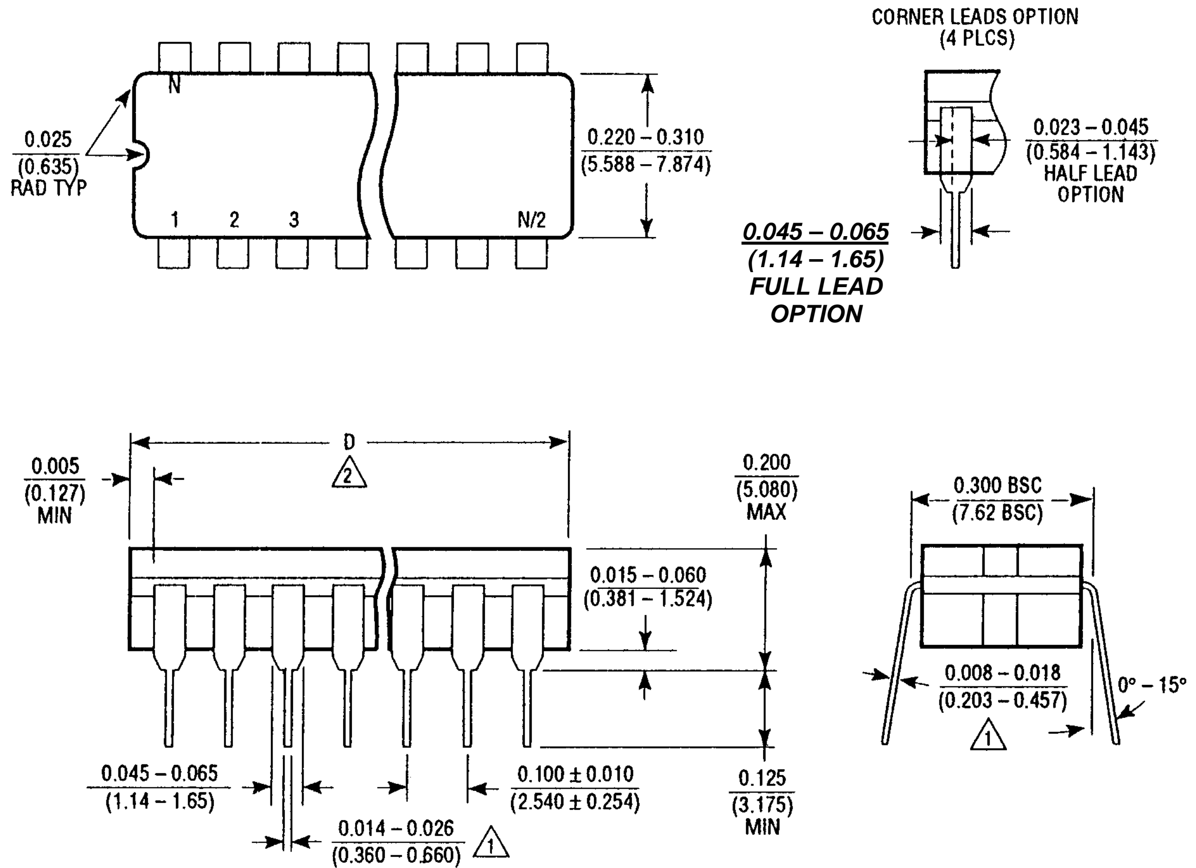
NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

θja = +150°C/W
θjc = +40°C/W

FIGURE 1

DEVICE OPTION # 2
(J8) CERAMIC DIP / 8 LEADS CASE OUTLINE

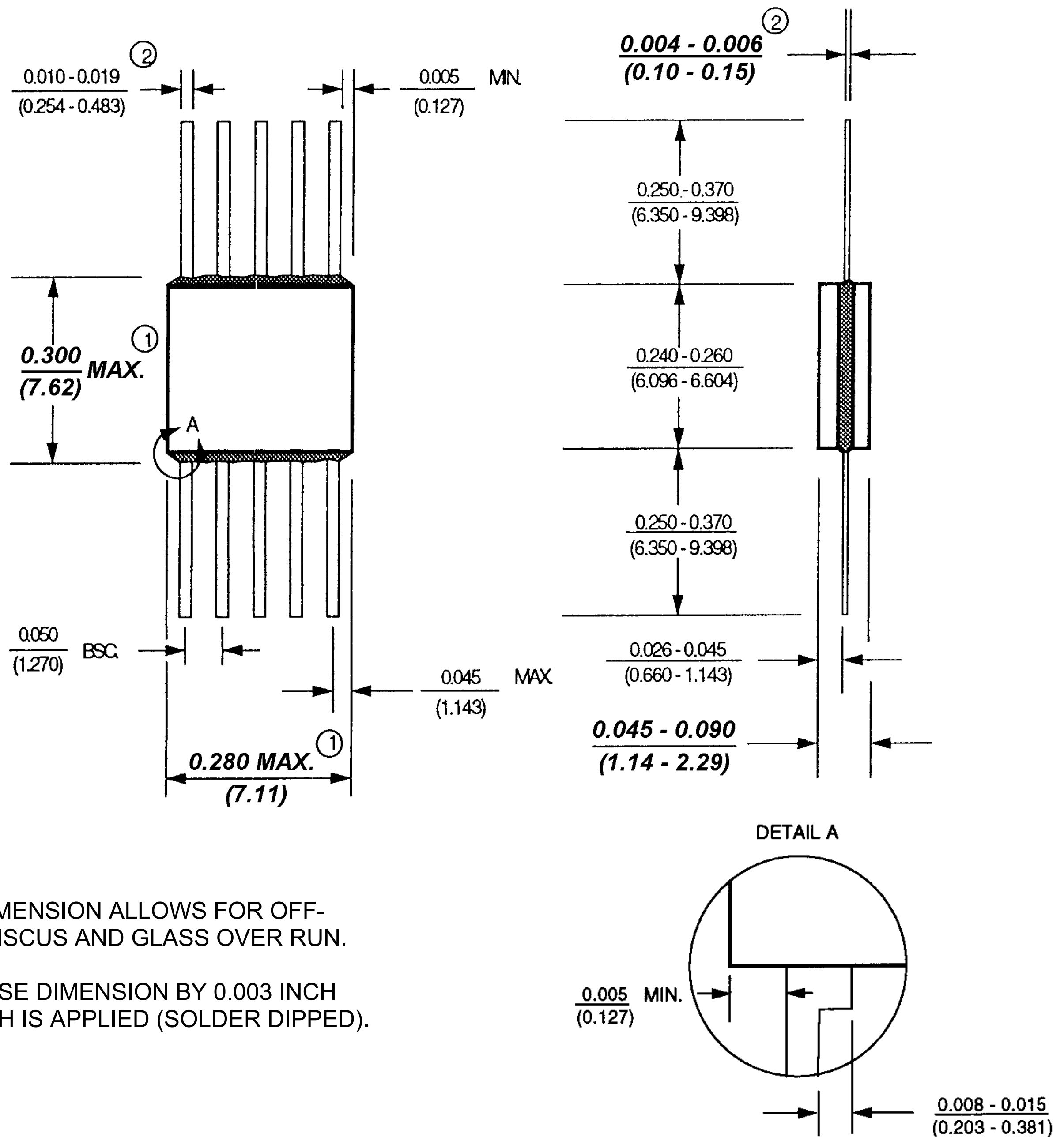


NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
2. 8 LEAD D MAX = .405 (10.287)

θ_{ja} = +110°C/W
θ_{jc} = +30°C/W

FIGURE 2

DEVICE OPTION # 3
(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

$\theta ja = +170°C/W$
$\theta jc = +40°C/W$

FIGURE 3

TERMINAL CONNECTIONS

DEVICE OPTION #1, TO5 8 LEAD METAL CAN

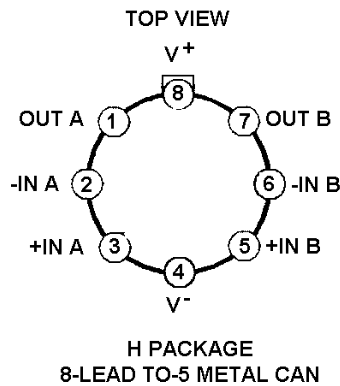


FIGURE 4

DEVICE OPTION #2, 8 LEAD

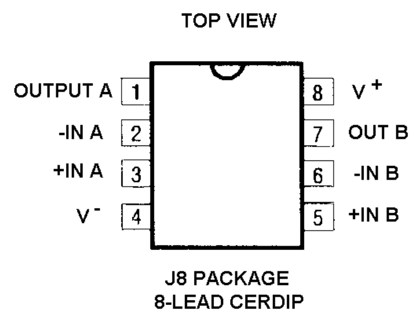


FIGURE 5

DEVICE OPTION #3, GLASS SEALED 10 LEAD FLATPACK

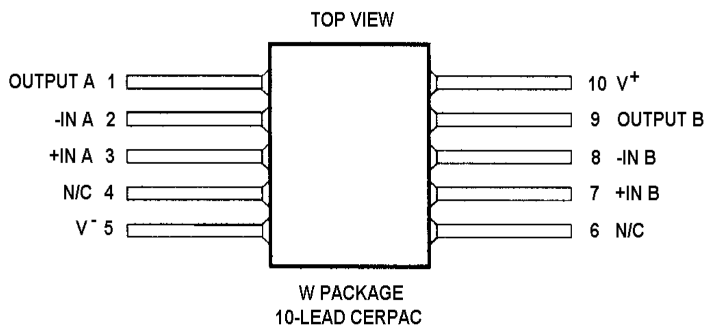
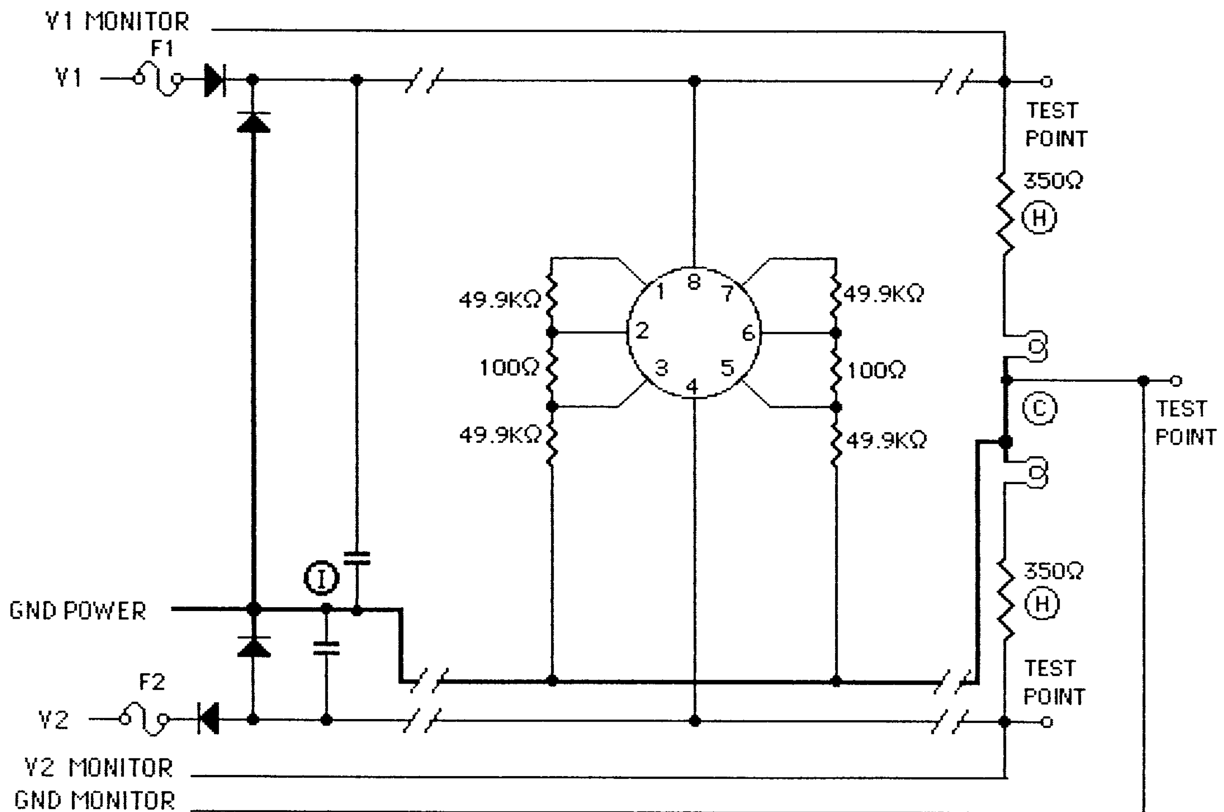


FIGURE 6

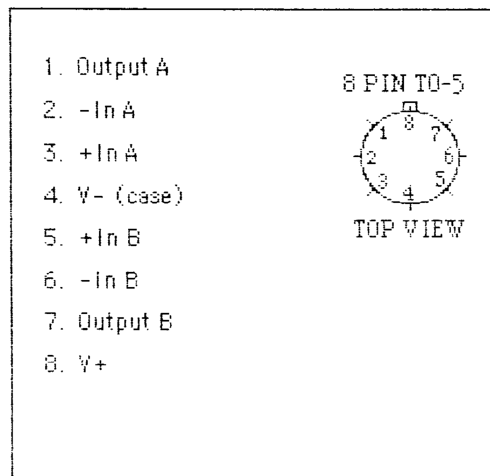
STATIC BURN-IN CIRCUIT

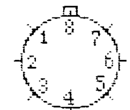
OPTION 1, TO5 METAL CAN / 8 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = +134 °C maximum.
3. Ta = +125 °C.
4. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V

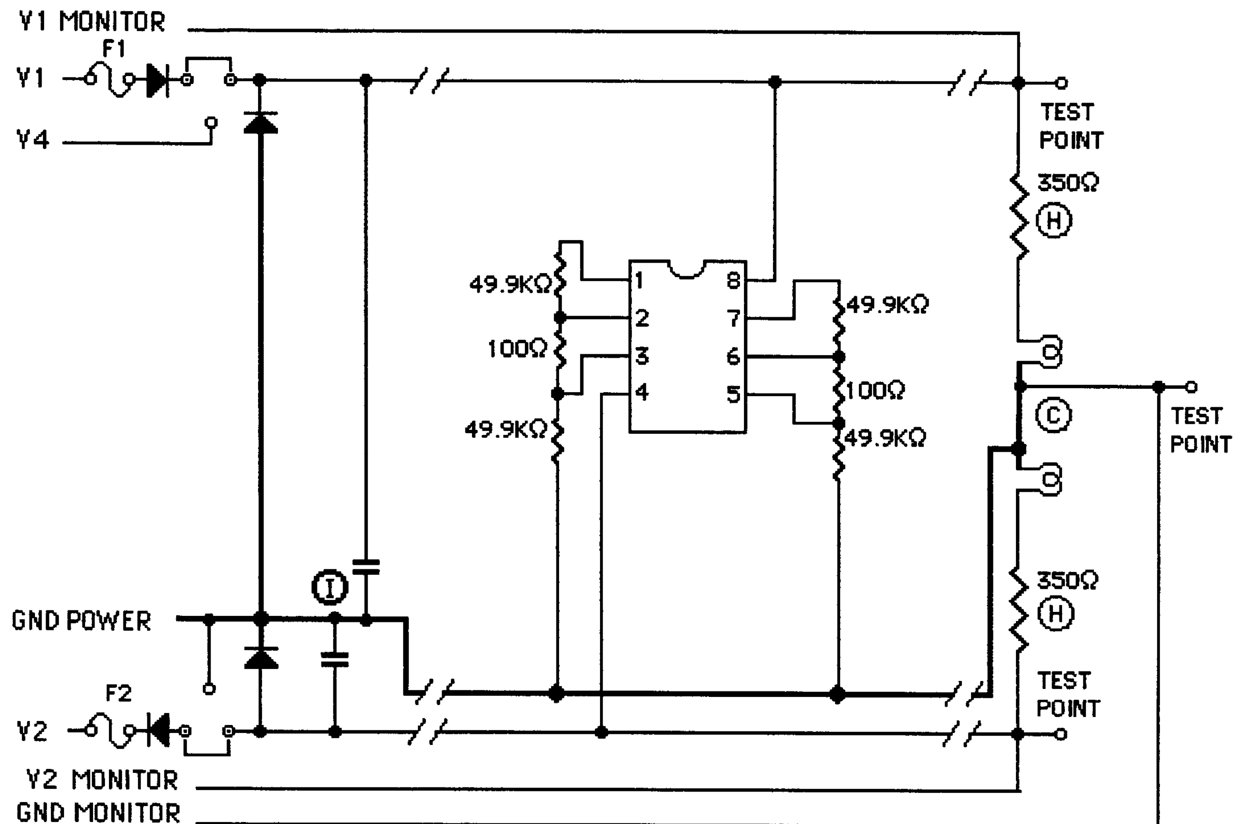


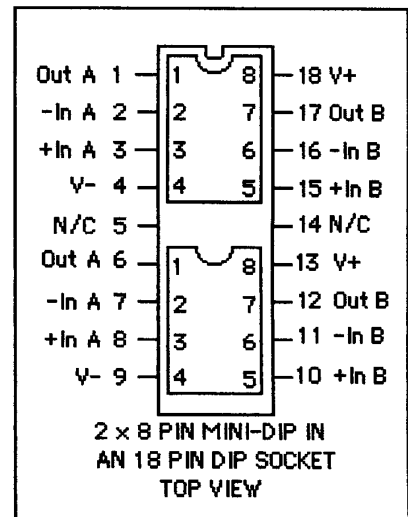


PACKAGE

FIGURE 7

STATIC BURN-IN CIRCUIT
OPTION #2, CERDIP / 8 LEADS





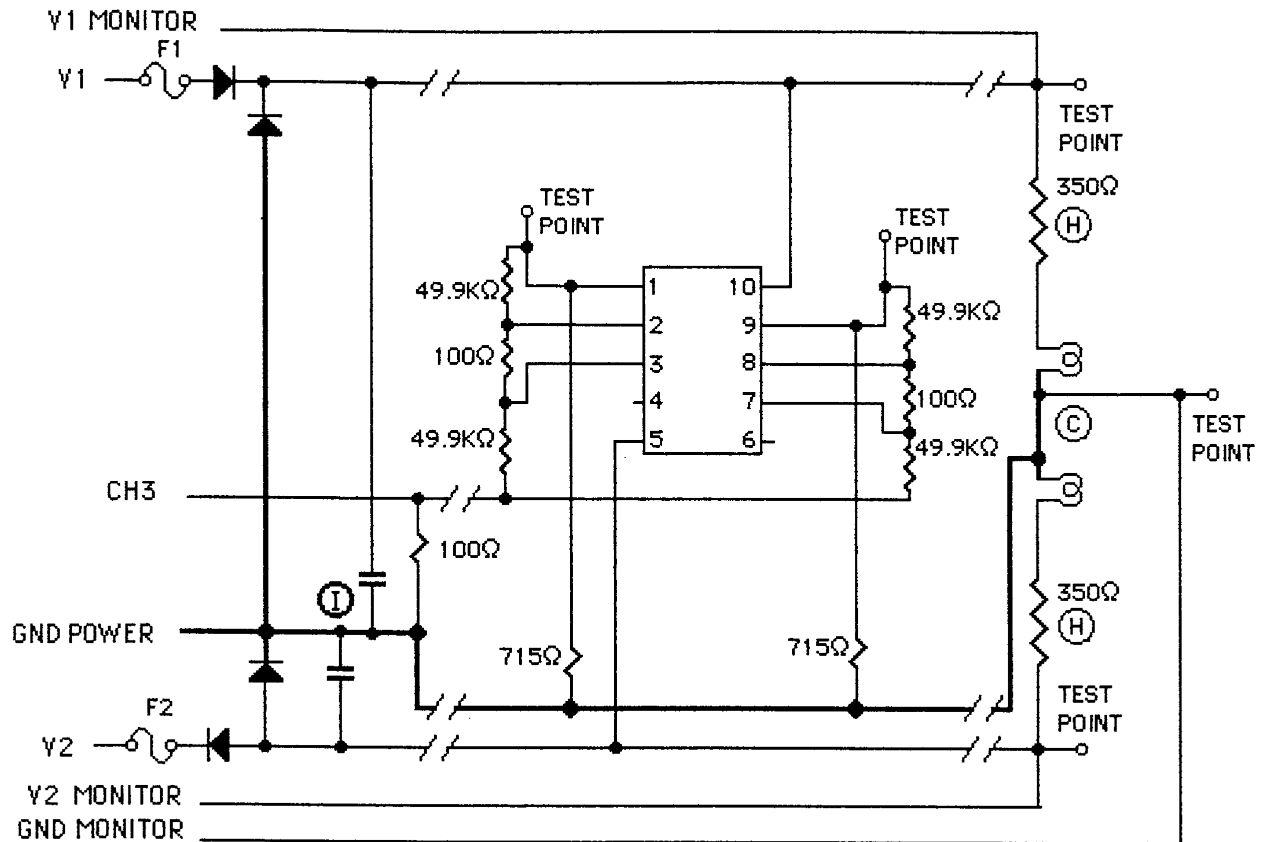
PACKAGE

NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = +134°C maximum.
3. Ta = +125°C.
4. Burn-in Voltages : V1 = +20V to +22V
   V2 = -20V to -22V

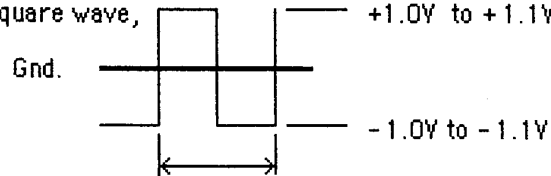
FIGURE 8

STATIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD



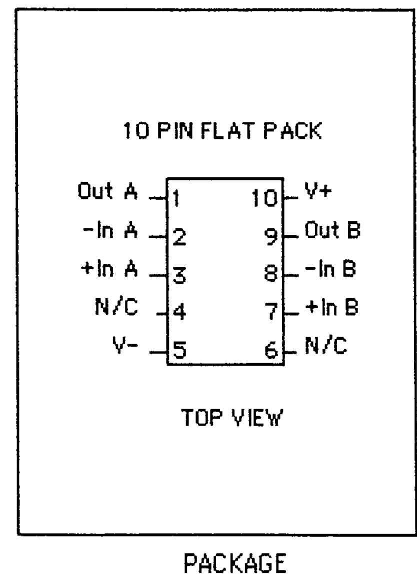
NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 168 °C maximum.
3. Ta = 150°C.
4. Burn-in Voltages: V1 = + 20V to + 22V
   V2 = - 20V to - 22V
5. CH. 3 = Square wave,



Frequency, 4.5hz(222ms) to 5.5hz(182ms)

BOARD TO BE USED FOR BOTH STATIC AND DYNAMIC BURN-IN. ENSURE THAT CHANNEL THREE IS PRESENT FOR DYNAMIC BURN-IN. ENSURE THAT CHANNEL THREE IS NOT PRESENT FOR STATIC BURN-IN.



PACKAGE

FIGURE 9

TOTAL DOSE BIAS CIRCUIT

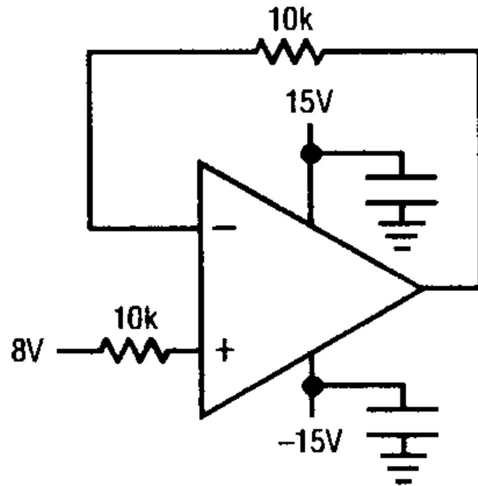


FIGURE 10

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION)

V_S = 5V, V_{CM} = 0.1V, V_{OUT} = 1.4V unless otherwise specified.

				T_A = 25°C			SUB-	−55°C ≤ T_A ≤ 125°C			SUB-	
SYMBOL	**PARAMETER**	**CONDITIONS**	**NOTES**	**MIN**	**TYP**	**MAX**	**GROUP**	**MIN**	**TYP**	**MAX**	**GROUP**	**UNITS**
V_{OS}	Input Offset Voltage					120	4			370	2, 3	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Tempco of Offset Voltage								0.5			µV/°C
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term V_{OS} Stability				0.5							µV/Month
I_{OS}	Input Offset Current					0.8	1			1.5	2, 3	nA
I_B	Input Bias Current					15	1			18	2, 3	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz	1		0.5							µVP-P
	Input Noise Voltage Density	f_0 = 10Hz f_0 = 1kHz	1 1		25 24							nV/√Hz nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz	1		2.6							pAP-P
	Input Noise Current Density	f_0 = 10Hz f_0 = 1kHz	1 1		0.07 0.025							pA/√Hz pA/√Hz
R_{IN}	Input Resistance Differential		2		600							MΩ
	Common Mode		2		5							GΩ
	Input Voltage Range		2 2	3.5 0			1 1	3.20 0.05			2, 3 2, 3	V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.5V V_{CM} = 0.05V to 3.2V		94 			1 	 88			 2, 3	dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V V_S = 3.1V to 12V		100 			1 	 94			 2, 3	dB dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.03V to 4V, No Load V_O = 0.03V to 3.5V, R_L = 50k V_O = 0.05V to 4V, No Load V_O = 0.05V to 3.5V, R_L = 50k		150 120 			1 1 	 80 60			 2, 3 2, 3	V/mV V/mV V/mV V/mV
V_{OUT}	Output Voltage Swing	Output Low, No Load Output Low, 2k to GND Output Low, I_{SINK} = 100µA Output High, No Load Output High, 2k to GND		 4.2 3.5		6 2 130 	4 4 4 4 4	 3.9 3.0		8 170 	5, 6 5, 6 5, 6 5, 6	mV mV mV V V
SR	Slew Rate	A_V = 1, V_S = ±2.5V		0.04			4					V/µs
GBW	Gain-Bandwidth Product	f_0 ≤ 20kHz			200							kHz
I_S	Supply Current	per Amplifier				75	1			95	2, 3	µA
	Channel Separation	ΔV_{IN} = 3V, R_L = 10k			130							dB
	Minimum Supply Voltage		3			2.3						V

NOTE: TABLE I IS CONTINUE ON THE FOLLOWING PAGE. NOTES FOR TABLE I ARE ON THE FOLLOWING PAGE.

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) continued

V_S = ±15V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	TYP	MAX	SUB-GROUP	−55°C ≤ T_A ≤ 125°C MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage					350	4			600	2, 3	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Tempco of Offset Voltage								0.6			µV/°C
I_{OS}	Input Offset Current					0.8	1			1.5	2, 3	nA
I_B	Input Bias Current					15				18	2, 3	nA
	Input Voltage Range			13.5 −15.0			1 1					V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 13.5V, −15V V_{CM} = 13V, −14.9V		97			1	 90			 2, 3	dB dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ±18V		100			1	94			2, 3	dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V, R_L = 50k V_O = ±10V, R_L = 2k V_O = ±10V, R_L = 5k		1000 300			1 1	 150			 2, 3	V/mV V/mV V/mV
V_{OUT}	Output Voltage Swing	R_L = 50k R_L = 2k R_L = 5k		±13 ±11			4 4	 ±11			 5, 6	V V V
SR	Slew Rate			0.06			4					V/µs
I_S	Supply Current	Per Amplifier				100	1			125	2, 3	µA

Note 1: All noise parameters are for V_S = ±2.5V, V_O = 0V.

Note 2: This parameter is guaranteed by design, characterization or correlation to other tested parameters.

Note 3: Power supply rejection ratio is measured at the minimum supply voltage. The op amps actually work at 1.8V supply but with a typical offset skew of −300µV.

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION)

V_S = 5V, 0V, V_{CM} = 0.1V, V_0 = 1.4V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	10KRAD(Si) MIN	10KRAD(Si) MAX	25KRAD(Si) MIN	25KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	75KRAD(Si) MIN	75KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage			120		175		250		500			µV
I_{OS}	Input Offset Current			2		8		13		18			nA
I_B	Input Bias Current			20		40		80		100			nA
	Input Voltage Range		3.5		3.5		3.5		3.5				V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.5V	91		89		87		85				dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V	100		100		98		88				dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 0.03V to 4V, No Load	150		150		100		50				V/mV
		V_O = 0.03V to 3.5V, R_L = 50k	120		50		20		10				V/mV
V_{OUT}	Output Voltage Swing	Output Low, No Load		6		9		13		20			mV
		Output Low, 2k to GND		2		2		2		2			mV
		Output Low, I_{SINK} = 100µA		130		140		150		160			mV
		Output High, No Load	4.2		4.2		4.2		4.2				V
		Output High, 2k to GND	3.5		3.5		3.5		3.5				V
S_R	Slew Rate	A_V = 1, V_S = ±2.5V	0.04		0.03		0.02		0.01				V/µs
I_S	Supply Current	per Amplifier		75		75		75		75			µA

V_S = ±15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	10KRAD(Si) MIN	10KRAD(Si) MAX	25KRAD(Si) MIN	25KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	75KRAD(Si) MIN	75KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage			350		500		650		800		1000	µV
I_{OS}	Input Offset Current			2		8		13		18		23	nA
I_B	Input Bias Current			20		40		80		100		120	nA
	Input Voltage Range		13.5		13.5		13.5		13.5		13.5		V
			−15.0		−15.0		−15.0		−15.0		−15.0		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 13.5V, −15V	94		92		90		88		86		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ±18V	100		100		98		88		78		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = 10V, R_L = 50k	1000		700		400		150		50		V/mV
		V_O = 10V, R_L = 2k	300		200		120		45		15		V/mV
V_{OUT}	Output Voltage Swing	R_L = 50k	±13		±13		±13		±13		±13		V
		R_L = 2k	±11		±11		±11		±11		±10		V
SR	Slew Rate		0.05		0.04		0.03		0.02		0.01		V/µs
I_S	Supply Current	per Amplifier		100		100		100		100		100	µA

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-350	350	-70	70	µV
$+I_B$	-15	0	-1.5	1.5	nA
$-I_B$	-15	0	-1.5	1.5	nA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5, 6
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3, 4, 5, 6
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.