REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	01/22/98
A	ADDED PARAGRAPH 3.3, SPECIAL HANDLING OF DICE, TO PAGE 2. THE PARAGAPHS WERE RENUMBERED AND PARAGRAPHS THAT FOLLOWED WERE RELOCATED TO PAGES 3 THROUGH 5. CORRECTED θja AND θjc FOR TO39 AND TO3 CASE OUTLINES, PAGES 10 AND 11.	07/16/99
B	PAGE 3, PARAGRAPH 3.8 CHANGED VERBIAGE ADDED "HEREIN" AFTER TABLE 1. PAGE 4, PARAGRAPH 5.0 CHANGED VERBIAGE ADDED "HEREIN" AFTER TABLE 3. PARAGRAPH 5.2 ADDED "HEREIN" AFTER TABLE 2. PARAGRAPH 6.2 ADDED "HEREIN" AFTER TABLE 3. PAGE 5, 6.3 CHANGED VERBIAGE ADDED "HEREIN" AFTER TABLE 3.	11/19/99
C	• PAGE 3, PARAGRAPH 3.7.1, CHANGED THE DOSAGE RATE FROM "APPROXIMATELY 20 RADS PER SECOND" TO "LESS THAN OR EQUAL TO 10 RADS PER SECOND". • PAGE 4, PARAGRAPH 6.1 CHANGED QUALITY ASSURANCE PROVISIONS TO STATE THAT LTC IS QML CERTIFIED AND THAT RAD HARD CANDIDATES ARE ASSEMBLED ON QUALIFIED CLASS S MANUFACTURING LINES. • PAGES 6 THROUGH 12, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • CONVERSION OF SPECIFICATION FROM WORD PERFECT TO MICROSOFT WORD.	07/25/02
D	• PAGE 3, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/22/05
E	• PAGE 3 PARAGRAPH 3.7.1 CHANGED VERBIAGE. • PAGE 4 PARAGRAPH 5.8 CHANGED OPTION 2 TO ALLOY 52 PACKAGE REQUIREMENT	05/13/08
F	• PAGE 15, CHANGED RH CANNED SAMPLE TABLE III FOR QUALIFYING DICE SALES ADDED TEMPERATURE CYCLE, CONSTANT ACCELERATION & REMOVED PIND TEST.	02/17/09
G	Page 2, amended section 3.3, Special Handling of Dice, to more accurately describe our current procedures and requirements.	04/05/12
H	Page 15, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from "15%" to "10%".	07/02/13
I	**Updated Die Sales table on pg 15.**	**03/24/15**

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

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INDEX	REVISION	**I**	**I**	**I**	**I**	**I**	**I**	**I**	**I**	**I**	**I**	**I**	**I**	**I**	**I**	**I**	
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				ANALOG DEVICES INC.
	ORIG			
	DSGN			TITLE: **MICROCIRCUIT, LINEAR, RH117H AND RH117K POSITIVE ADJUSTABLE REGULATOR DICE**
	ENGR			
	MFG			
	CM			
	QA			SIZE / CAGE CODE / DRAWING NUMBER / REV
	PROG			**64155** / **05-08-5116** / **K**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH117, Positive Adjustable Regulator Dice and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number:

3.2.1 OPTION 1 – RH117H Dice

3.2.2 OPTION 2 – RH117K Dice

3.3 **Special Handling of Dice**: Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Analog Devices Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

ADI recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	-55°C to 150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.

3.7 Radiation Hardness Assurance (RHA):

3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.7.3 Total dose bias circuit is specified in **Figure 2**.

3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at Ta = +25°C to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.

3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ.**

3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.

4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.

5.0 SAMPLE ELEMENT EVALUATION: A sample from **each wafer supplying dice** shall be assembled and subjected to element evaluation per **Table III** herein.

5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.

5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in **Table I** and **Table II** herein.

5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.

5.4 Part Marking of Element Evaluation Sample Includes**:**

5.4.1 LTC Logo

5.4.2 LTC Part Number

5.4.3 Date Code

5.4.4 Serial Number

5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A

5.4.6 Diffusion Lot Number

5.4.7 Wafer Number

5.5 Burn-In Requirement: Burn-In circuit for TO39 package is specified in **Figure 3** and Burn-In circuit for TO3 package is specified in **Figure 4.**

5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with **Figure 5** and **Figure 6.**

5.7 Terminal Connections: The terminal connections shall be as specified in **Figure 7** and **Figure 8.**

5.8 Lead Material and Finish: The lead material and finish shall be Kovar for device option 1 and Alloy 52 for device option 2, with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with **Table III** herein.

6.3 Screening: Screening requirements shall be in accordance with **Table III** herein.

6.4 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

6.4.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.

6.4.2 100% attributes (completed element evaluation traveler).

6.4.3 Element Evaluation variables data, including Burn-In and Op Life

6.4.4 SEM photographs (3.10 herein)

6.4.5 Wafer Lot Acceptance Report (3.9 herein)

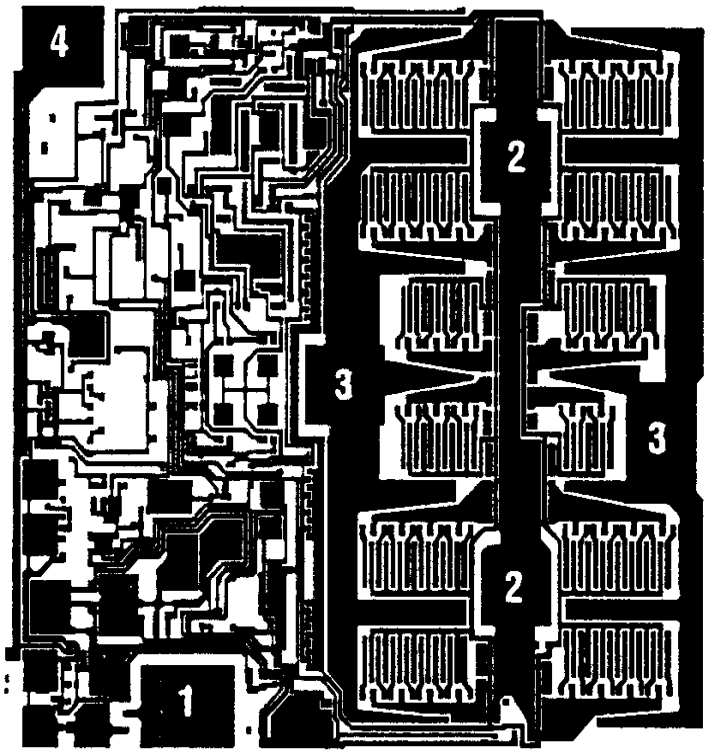
6.4.6 A copy of outside test laboratory radiation report if ordered

6.4.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6. 4.1 and 6. 4.7 will be delivered as a minimum, with each shipment.

7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS
OPTION 1, RH117H DICE AND OPTION 2, RH117K DICE



102 × 96 mils

PAD FUNCTION

1. Adjust
2. V_{OUT}*
3. V_{IN}
4. V_{OUT} Sense
   (Connect to V_{OUT})

*Backside is an alloyed layer. Connect to V_{OUT}.

FIGURE 1

TOTAL DOSE BIAS CIRCUIT

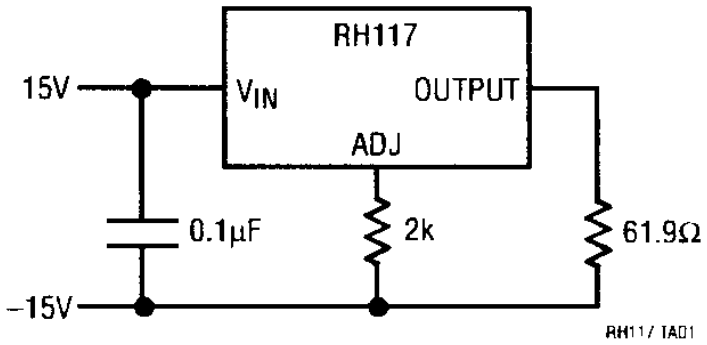
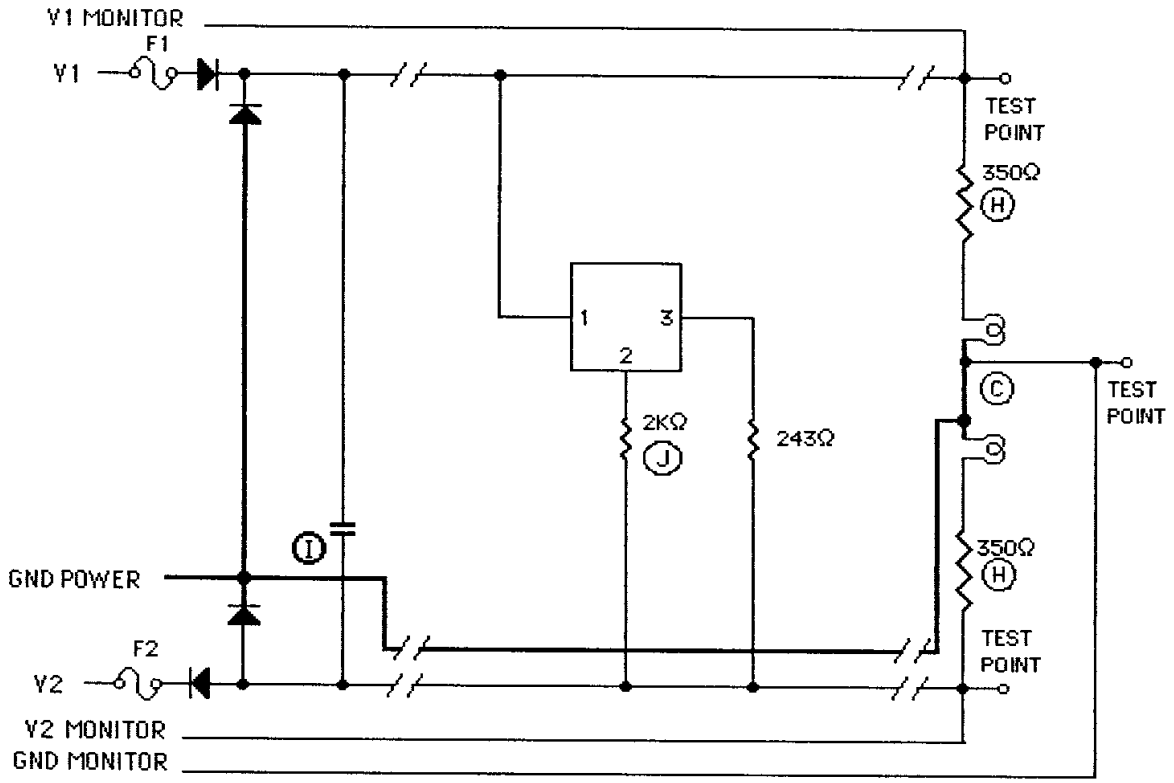


FIGURE 2

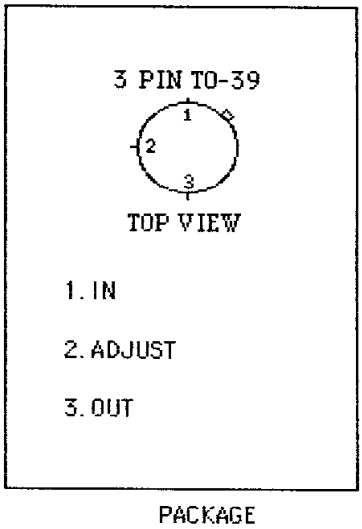
TO39 STATIC BURN-IN CIRCUIT

OPTION 1, T039 METAL CAN / 3 LEADS



NOTES:

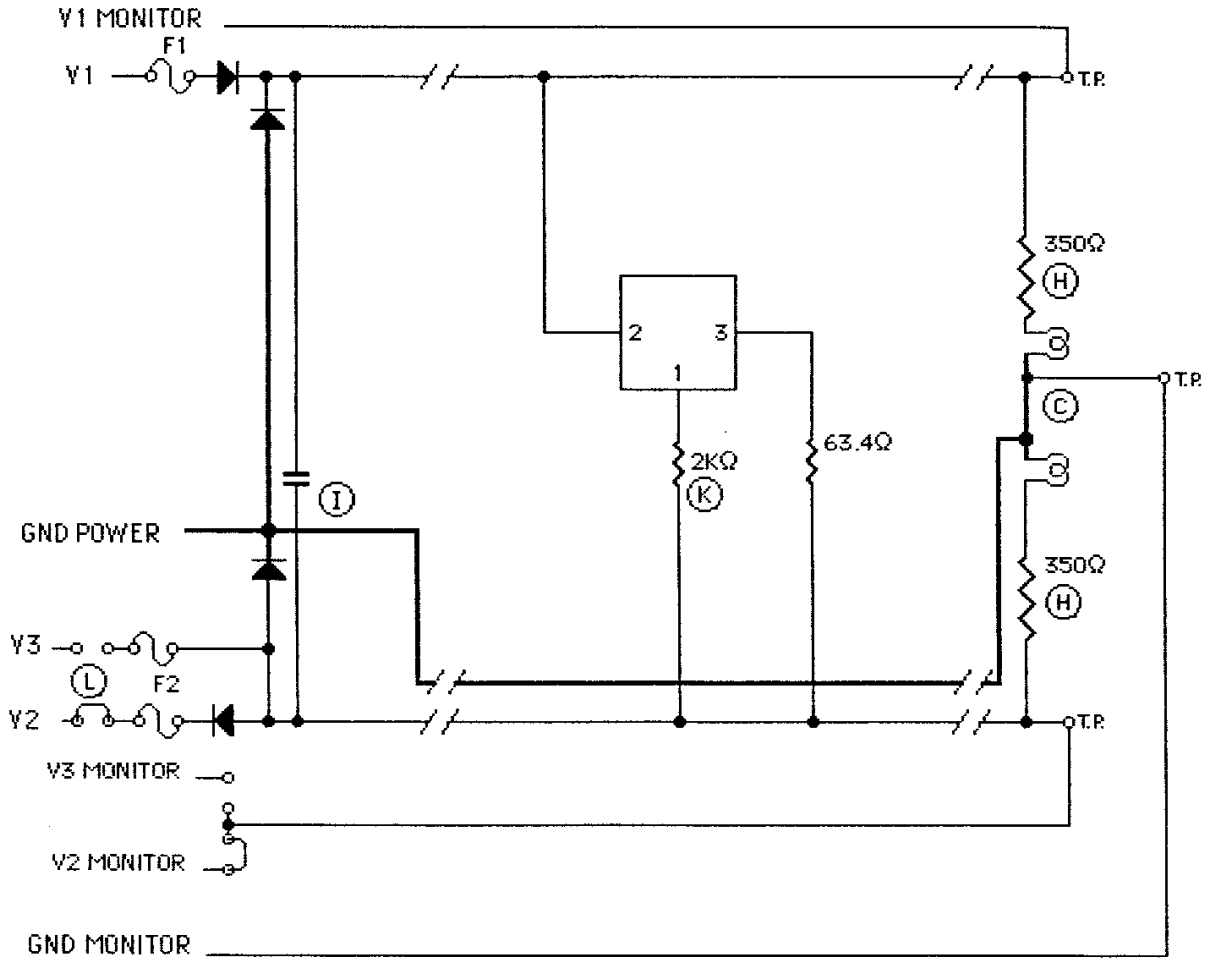
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 148°C maximum at 125°C ambient.
3. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V



PACKAGE

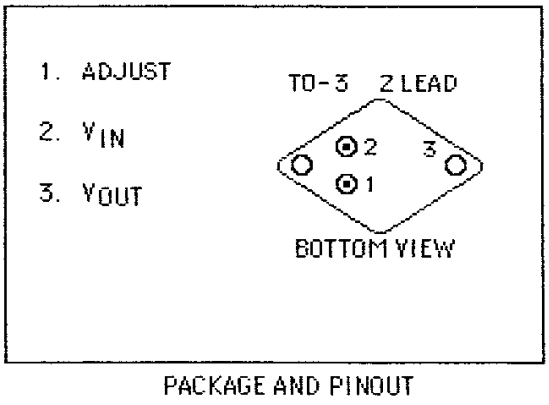
FIGURE 3

STATIC BURN-IN CIRCUIT
OPTION #2, TO3 / 2 LEADS



NOTES:

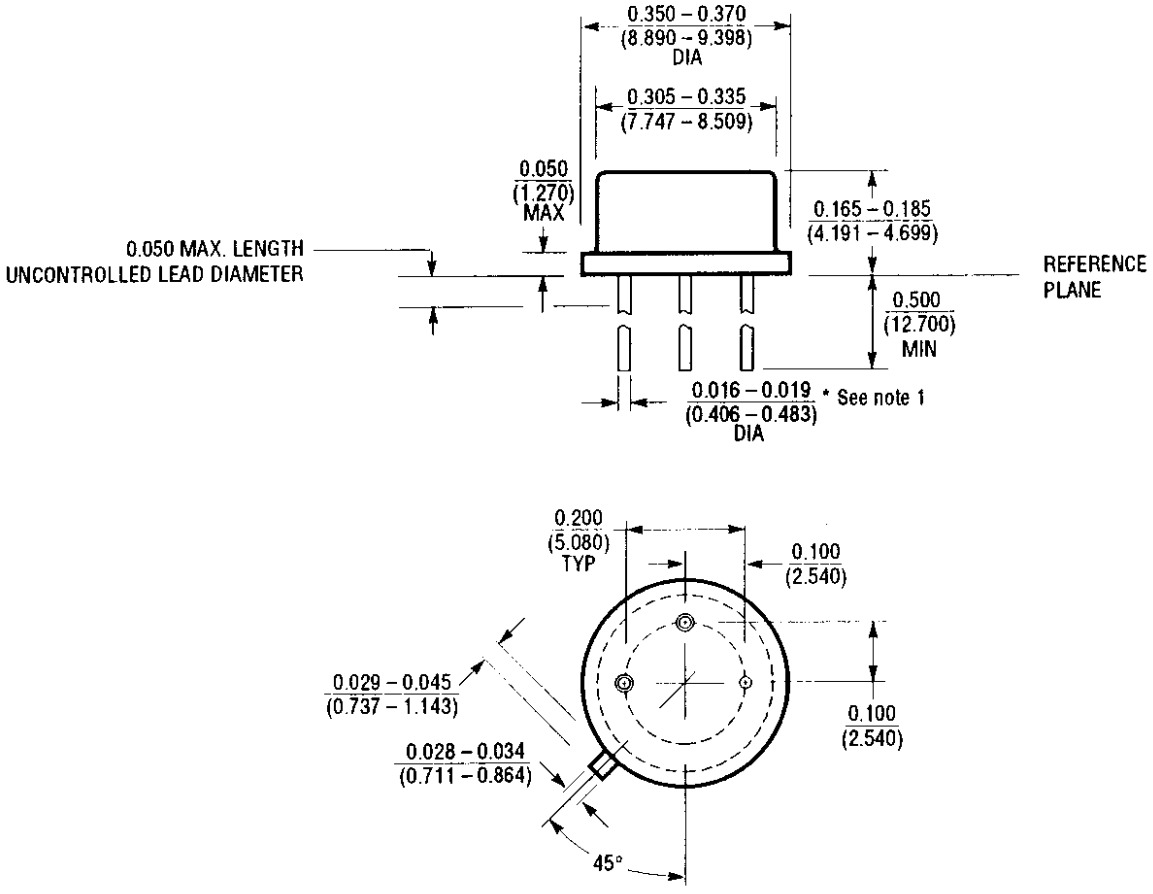
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 150°C maximum at 125°C
3. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V



PACKAGE AND PINOUT

FIGURE 4

DEVICE OPTION # 1
(H) TO39 METAL CAN / 3 LEADS CASE OUTLINE

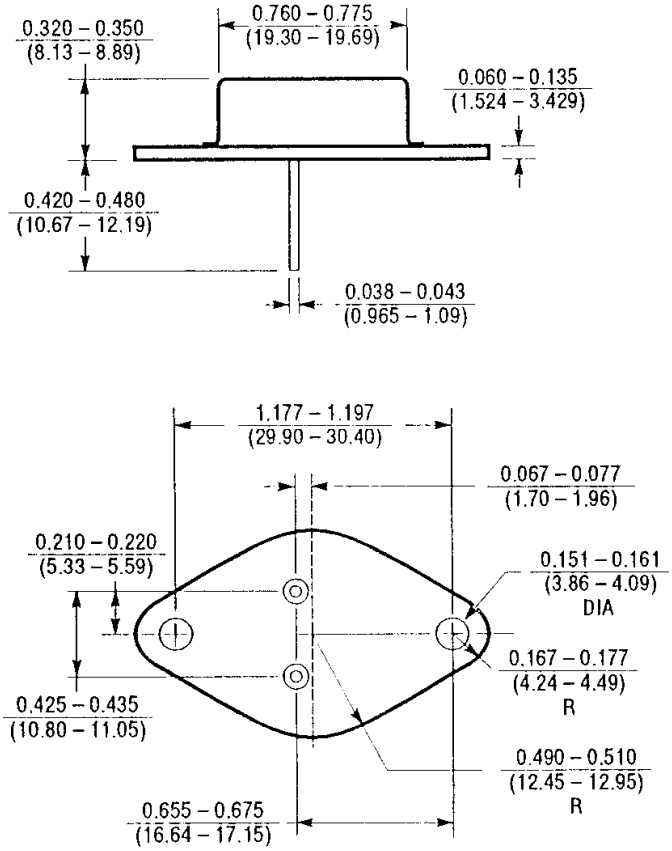


NOTE: 1. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

FIGURE 5

θ_{ja} = +150°C/W
θ_{jc} = +40°C/W

DEVICE OPTION # 2
(K) TO3 METAL CAN / 2 LEADS CASE OUTLINE



θja = +35°C/W
θjc = +3°C/W

FIGURE 6

TERMINAL CONNECTIONS
DEVICE OPTION #1, TO39 / 3 LEAD METAL CAN

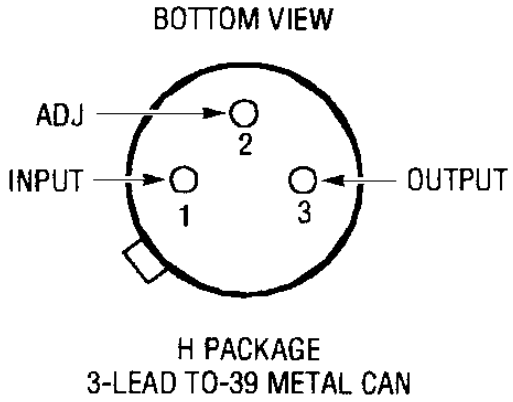


FIGURE 7

DEVICE OPTION #2, TO3 / 2 LEAD METAL CAN

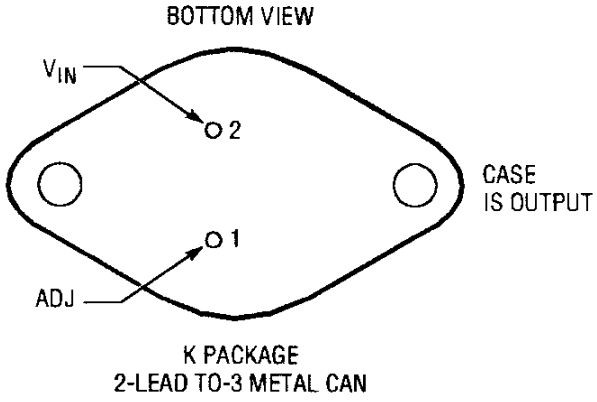


FIGURE 8

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation (Note 4)

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_J = 25°C$ MIN	$T_J = 25°C$ MAX	SUB-GROUP	$-55°C \le T_J \le 150°C$ MIN	$-55°C \le T_J \le 150°C$ MAX	SUB-GROUP	UNITS
V_{REF}	Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$		1.20	1.30	1	1.20	1.30	2,3	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_{OUT} = 10mA$	2		0.02	1		0.05	2,3	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \le 5V$	2		15	1		50	2,3	mV
		$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \ge 5V$	2		0.3	1		1	2,3	%
I_{ADJ}	Adjust Pin Current				100	1		100	2,3	µA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{MAX}$			5	1		5	2,3	µA
		$2.5V \le (V_{IN} - V_{OUT}) \le 40V$, $I_{OUT} = 10mA$			5	1		5	2,3	µA
I_{MIN}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$			5	1		5	2,3	mA
	Current Limit	$(V_{IN} - V_{OUT}) \le 15V$ H Package		0.5		1	0.5		2,3	A
		K Package		1.5		1	1.5		2,3	A
		$(V_{IN} - V_{OUT}) = 40V$ H Package		0.15		1				A
		K Package		0.30		1				A

Note 1: Unless otherwise specified, these specifications apply for $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the H package (TO-39) and $I_{OUT} = 0.5A$ for the K package (TO-3) package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. I_{MAX} is 0.5A for the TO-39 and 1.5A for the TO-3.

Note 2: Regulation is measured at a constant junction temperature using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Dice are probe tested at 25°C to the ($T_J = 25°C$) limits shown except for high current tests. At wafer sort, dice are tested under low current conditons. After assembly, high current tests are sample tested during the element evaluation. This assures high current specifications when assembled in packages approved by Linear Technology. For absolute maximum ratings, typical specifications, performance curves and finished product specifications, please refer to the standard RH data sheet.

TABLE II ELECTRICAL CHARACTERISTICS (POSTIRRADIATION) (Note 4)

T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	UNITS
V_{REF}	Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$		1.20	1.30	1.20	1.30	1.20	1.30	1.20	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$, I_{OUT} = 10mA	2		0.02		0.02		0.02		0.03	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \le 5V$	2		36		42		48		60	mV
		$10mA \le I_{OUT} \le I_{MAX}$, $V_{OUT} \ge 5V$	2		0.72		0.84		0.96		1.20	%
I_{ADJ}	Adjust Pin Current				100		100		100		100	µA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{MAX}$			5		5		5		5	µA
		$3V \le (V_{IN} - V_{OUT}) \le 40V$, I_{OUT} = 10mA			5		5		5		5	µA
I_{MIN}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$			5		5		5		5	mA
	Current Limit	$(V_{IN} - V_{OUT}) \le 15V$ H Package		0.5		0.5		0.5		0.5		A
		K Package		1.5		1.5		1.5		1.5		A
		$(V_{IN} - V_{OUT}) = 40V$ H Package		0.15		0.15		0.15		0.15		A
		K Package		0.30		0.30		0.30		0.30		A

Note 1: Unless otherwise specified, these specifications apply for $V_{IN} - V_{OUT}$ = 5V; and I_{OUT} = 0.1A for the H package (TO-39) and I_{OUT} = 0.5A for the K package (TO-3) package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. I_{MAX} is 0.5A for the TO-39 and 1.5A for the TO-3.

Note 2: Regulation is measured at a constant junction temperature using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Guaranteed by design, characterization or correlation to other tested parameters.

Note 4: T_J = 25°C unless otherwise noted.

TABLE III RH ELEMENT EVALUATION TABLE QUALIFICATION OF DICE SALES

LINEAR TECHNOLOGY

RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS K/S	CLASS V	CLASS H/B	OPERATION	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY (ACCEPT NUMBER)
1	X	X		SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25°C)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
	X	X		BOND PULL MONITOR	2011		
5	X	X		STABILIZATION BAKE	1008	C	ASSEMBLED PARTS ONLY
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
	X	X		GROSS LEAK	1014	C	
6	X	X		FIRST ROOM ELECTRICAL - READ & RECORD			45(0)
		X		(REPLACE ANY ASSEMBLY-RELATED REJECTS)			
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X	X		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs.	1015	+ 125°c MINIMUM 240 HOURS	
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25°C			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
		X		TOTAL IRRADIATION DOSE	1019	A	
	X	X		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	X	X		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005	+ 125°c MINIMUM 1000 HOURS	
	X	X		POST OP-LIFE ELECT. (R & R @ 25°C, + 125°C OR + 150°C, -55°C			
7	X	X	X	WIRE BOND EVALUATION	2011		15(0) OR 25(1) - # of wires

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Surgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.