REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	07/23/96
A	• PAGE 2: ADDED PARAGRAPHS 3.2.1, 3.2.2, AND 3.2.3. PARAGRAPH 3.3.b, ADDED "SEE PARAGRAPH 3.2". • PAGE 3: ADDED PARAGRAPHS 3.8.1, 3.8.2, AND 3.2.3. • PAGE 4: PARAGRAPH 3.12, WAFER LOT ACCEPTANCE, REDEFINED. PARAGRAPH 4.4.2, GROUP B INSPECTION, REDEFINED. • PAGE 5: PARAGRAPH 4.4.3, GROUP D INSPECTION, REDEFINED. PARAGRAPH 4.5, SOURCE INSPECTION, REDEFINED. • PAGE 6: ADDED θja AND θjc TO FIGURE 1, TO5 CASE OUTLINE. • PAGE 7: ADDED θja AND θjc TO FIGURE 2, CERAMIC DIP CASE OUTLINE. • PAGE 8: ADDED θja AND θjc TO FIGURE 3, BOTTOM BRAZED FLATPACK CASE OUTLINE.	12/11/97
B	PAGE 4, AMENDED PARAGRAPHS 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES.	02/23/98
C	PAGE 6, 7, 8, FIGURE 1, 2, 3 CHANGED θja AND θjc.	11/17/99
D	• PAGE 3: PARAGRAPHS 3.2.1, 3.2.2, 3.2.3, 3.2.4, FIGURES 1, 2, 3, AND 4 REMOVED. • PAGE 4: PARAGRAPHS 3.7 AND PARAGRAPH 3.9 CHANGED VERBIAGE IN LINE 2 OF EACH PARAGRAPH. • PAGE 5: PARAGRAPHS 4.3, 4.4.1, 4.4.2.2 CHANGED VERBIAGE IN LINE 2 OF EACH PARAGRAPH. • PAGE 6: PARAGRAPHS 4.4.3.2 CHANGED VERBIAGE IN LINE 1.	11/19/99
E	PAGE 9: CHANGED θja FROM +225°C/W TO +170°C/W AND θjc FROM +40°C/W TO 18°C/W PER PACKAGE ENGINEERING.	09/05/00
F	PAGE 9: CHANGED θja FROM +170°C/W TO 160°C/W PER PACKAGE ENGINEERING. ADDED OPTION 4, W10 LEAD FLATPACK GLASS SEALED.	01/09/01
G	CHANGED DELTA VOS LIMITS FROM ±1.0mV TO ±2.0mV. CONVERSION OF SPECIFICATION FROM WORD PERFECT TO MSWORD. REMOVED BOTTOM BRAZED FLATPACK OPTION AND ALL REFERENCES TO BOTTOM BRAZED FLATPACK.	08/31/01
H	• CONVERSION FROM WORD PERFECT TO MICROSOFT WORD. INCREASED SPEC PAGES TO 21 TOTAL. • PAGE 2, AN ADDITIONAL REVISION RECORD PAGE WAS INSTALLED. CONTINUED ON NEXT PAGE…..	04/15/03

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
INDEX	REVISION	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**	**Q**
REVISION	PAGE NO.	18	19															
INDEX	REVISION	**Q**	**Q**															

				ANALOG DEVICES INC.	
	ORIG				
	DSGN			TITLE:	
	ENGR			**MICROCIRCUIT, LINEAR, RH118, HIGH SPEED OPERATIONAL AMPLIFIER**	
	MFG				
	CM				
	QA			SIZE	CAGE CODE / DRAWING NUMBER / REV
	PROG				**64155** / **05-08-5025** / **R**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:	

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
	• PAGE 4: PARAGRAPH 3.4 , MOVED PARAGRAPH AND NOTES FROM PAGE 3. NOTE 2: CHANGED NOTES SHOWN ON PAGE 19 TO PAGE 20. PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.9, TABLE II CHANGED TO TABLE III. • PAGE 5: PARAGRAPH 3.11.1 WAS CHANGED FROM "…dosage rate of approximately 20 Rads per second" TO "…dosage rate of less than or equal to 10 Rads per second". PARAGRAPHS 4.1 THROUGH 4.4.2 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPHS 4.4.2.1 THROUGH 4.4.3 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. • PAGE 7: PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 8 THROUGH 18, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 19, TABLE IA WAS CHANGED TO TABLE II • PAGE 20, TABLE NOTES NOW REFLECTS TABLE I AND TABLE II BECAUSE OF CHANGE ON PAGE 19. • PAGE 21, TABLE II CHANGED TO TABLE III, TABLE III CHANGED TO TABLE IV.	04/15/03
J	• PAGE 10, CHANGED OUTLINE DRAWING PIN 1 NOTCH MOVED TO INSIDE LEAD LOCATION.	05/19/03
K	• PAGE 5, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/15/05
L	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 • PAGE 4 PARAGRAPH 3.10.3 ADDED OPTION 3 IS ALLOY 42 FOR FLATPACK. • CHANGED FIGURE 6 (W) PKG PIN 9 COMP3 TO 2 PIN 6 COMP2 TO 3, FIGURE 7 STATIC B/I NOTES 3 CHANGE B/I VOLTAGES V3= FROM (+ 1.0V TO + 1.1V) TO (+ 0.95V TO + 1.15V), FIGURE 8 DYNAMIC B/I ADDED 30pF, FIGURE 9 STATIC B/I NOTES 3 CHANGE B/I VOLTAGES V3= FROM (+ 1.0V TO + 1.1V) TO (+0.95V TO +1.15V), FIGURE 10 DYNAMIC B/I ADDED 30PF AND 10KΩ, FIGURE 11 STATIC B/I NOTES 2, 3 CHANGE Tj = FROM 191°C TO +165°C ADDED Tc = 139°C CHANGE Ta = FROM 125°C TO 100°C Tj = FROM 216°C TO +190°C AND Ta FROM 150°C TO 125°C, FIGURE 12 DYNAMIC BI NOTES:2, 3 CHANGED Tj = FROM 170°C TO +159°C ADDED Tc=135°C MIN. AT AMBIENT OF 100°C CHANGE Ta = 125°C TO Tj = +184°C MAX. AT AMBIENT OF 125°C, AND ADDED 30pF CHANGE 402Ω TO 301Ω PER. PRODUCT ENG.	01/07/08
M	• PAGE 6: PARAGRAPH 3.11.1 CHANGED VERBIAGE • PAGE 5: PARAGRAPH 3.10.3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT.	04/30/08
N	• PAGE 6, PARAGRAPH 4.4.2 CHANGED VERBIAGE. • PAGE 11, FIGURE 3 NOTE 2 ADDED TO LEAD THICKNESS.	06/12/08
P	• PAGE 17, STATIC BURN-IN CIRCUIT FIGURE. T_a CHANGED FROM +100°C TO +125°C; T_j CHANGED FROM +165°C TO +164°C; BURN-IN VOLTAGES, V1 CHANGED FROM "+20V TO +22V" TO "+18V TO +19.8V", V2 CHANGED FROM "-20V TO -22V" TO "-18V TO -19.8V".	6/14/13
Q **R**	CHANGED NOTE REQUIREMENTS IN FIGURE 7, 8, 9 & 10 **TO REMOVE SOURCE AND CHANGE LINEAR TO ANALOG**	06/18/15 **4/5/21**

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH118 High Precision High Speed Operational Amplifier, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH118H (TO5 Metal Can, 8 Leads)

3.2.2 Option 2 – RH118J8 (Ceramic Dip, 8 Leads)

3.2.3 Option 3 – RH118W (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage	±20V
Differential Input Current (See Note 1)	±10mA
Input Voltage (See Note 2)	±20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Sec)	+300°C

Note 1: The inputs are shunted with back-to-back zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage. (Notes also shown on page 20)

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 2.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and Table II.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in Table IV herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8

3.8.2 Option 2 (Ceramic Dip): Static Burn-In, Figure 9; Dynamic Burn-In, Figure 10

3.8.3 Option 3 (Glass Sealed Flatpack) : Static Burn-In, Figure 11; Dynamic Burn-In, Figure 12

3.9 Delta Limit Requirement: Delta limit parameters are specified in Table III herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical, dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar and options 2, 3 are Alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL- STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 13.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in **Table IV** herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in **Table IV** herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1

Group B, Subgroup 2c = 10%	Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)
Group B, Subgroup 3 = 10%	
Group B, Subgroup 4 = 5%	Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.5.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.5.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.5.3 Burn-In Variables Data and Deltas (if applicable)

4.5.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.5.5 Generic Group D data (4.4.3 herein)

4.5.6 SEM photographs (3.13 herein)

4.5.7 Wafer Lot Acceptance Report (3.13 herein)

4.5.8 X-Ray Negatives and Radiographic Report

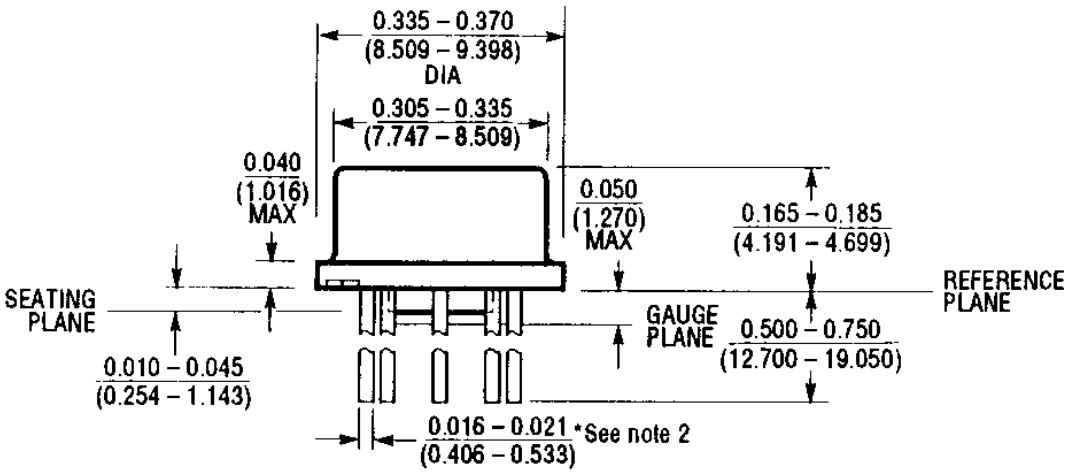
4.5.9 A copy of outside test laboratory radiation report if ordered

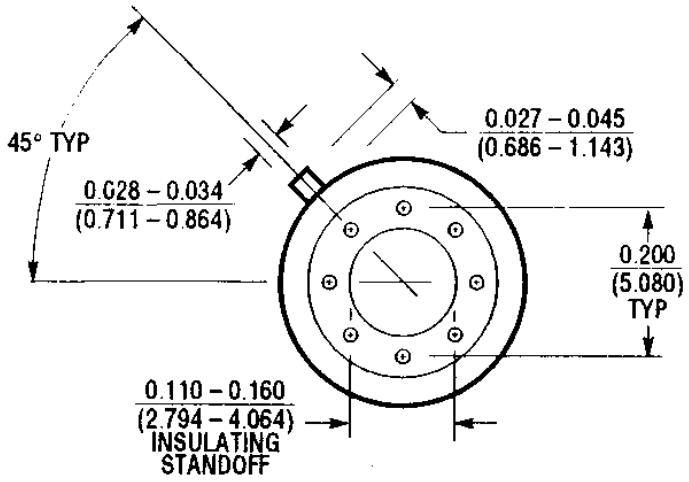
4.5.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.5.1 and 4.5.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as “No Charge Data”.

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1
(H) TO5 / 8 LEADS CASE OUTLINE



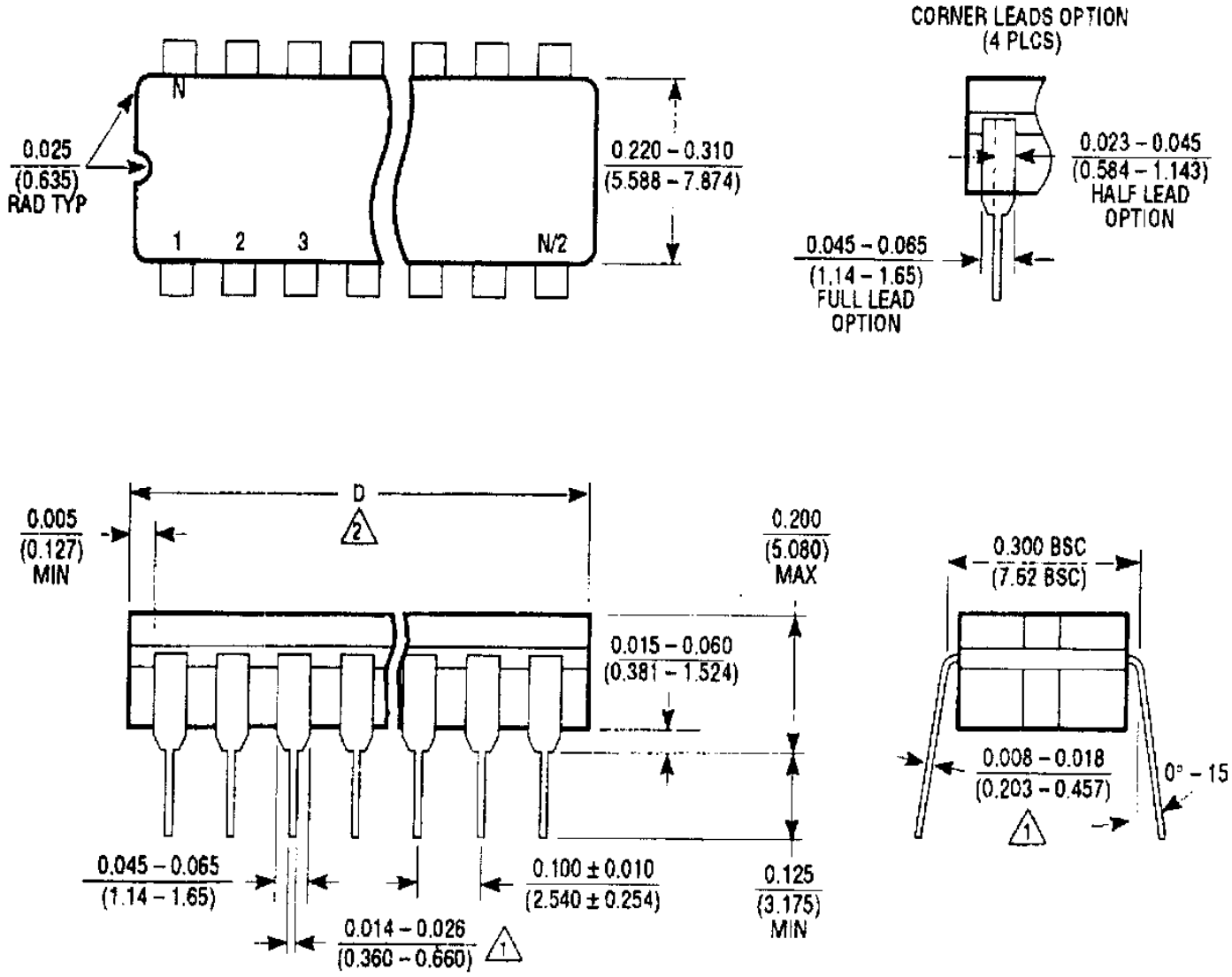


NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

θ_{ja} = +150°C/W
θ_{jc} = +40°C/W

FIGURE 1

DEVICE OPTION # 2
(J8) CERAMIC DIP / 8 LEADS CASE OUTLINE

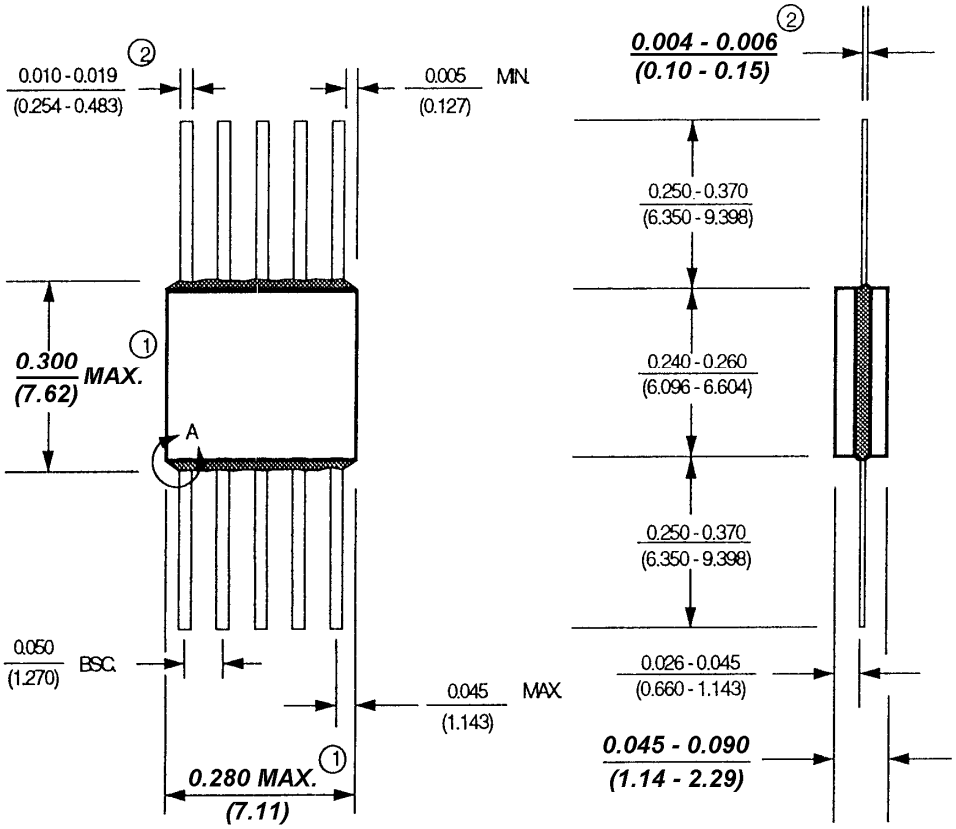


NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
2. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.
3. 8 LEAD, D MAX = 0.405 (10.287)

θ_{ja} = +110°C/W
θ_{jc} = +30°C/W

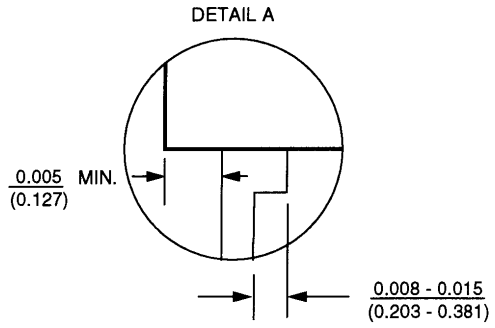
FIGURE 2

DEVICE OPTION # 3
(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).



θ_{ja} = +170°C/W
θ_{jc} = +40°C/W

FIGURE 3

TERMINAL CONNECTIONS

DEVICE OPTION #1, TO5, 8 LEAD METAL CAN

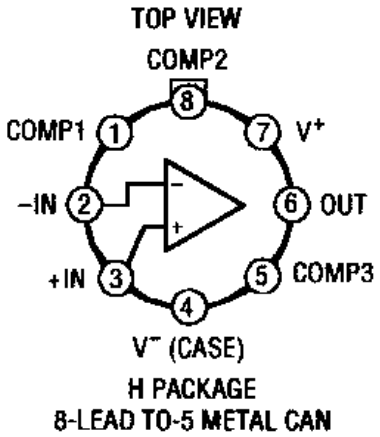


FIGURE 4

DEVICE OPTION #2, CERAMIC, 8 LEAD

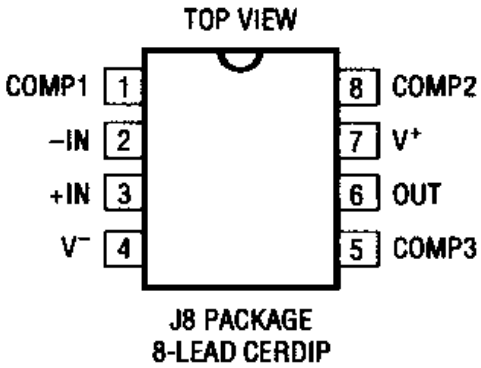


FIGURE 5

DEVICE OPTION #3, GLASS SEALED, 10 LEAD FLATPACK

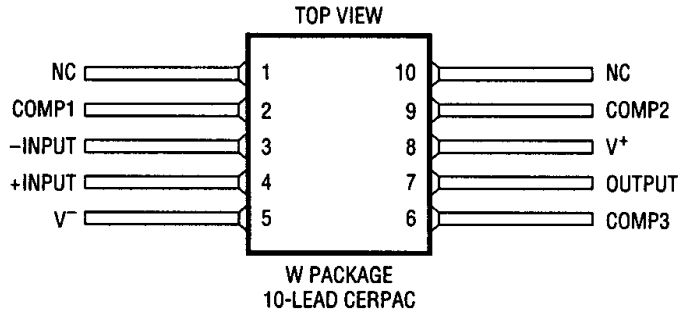
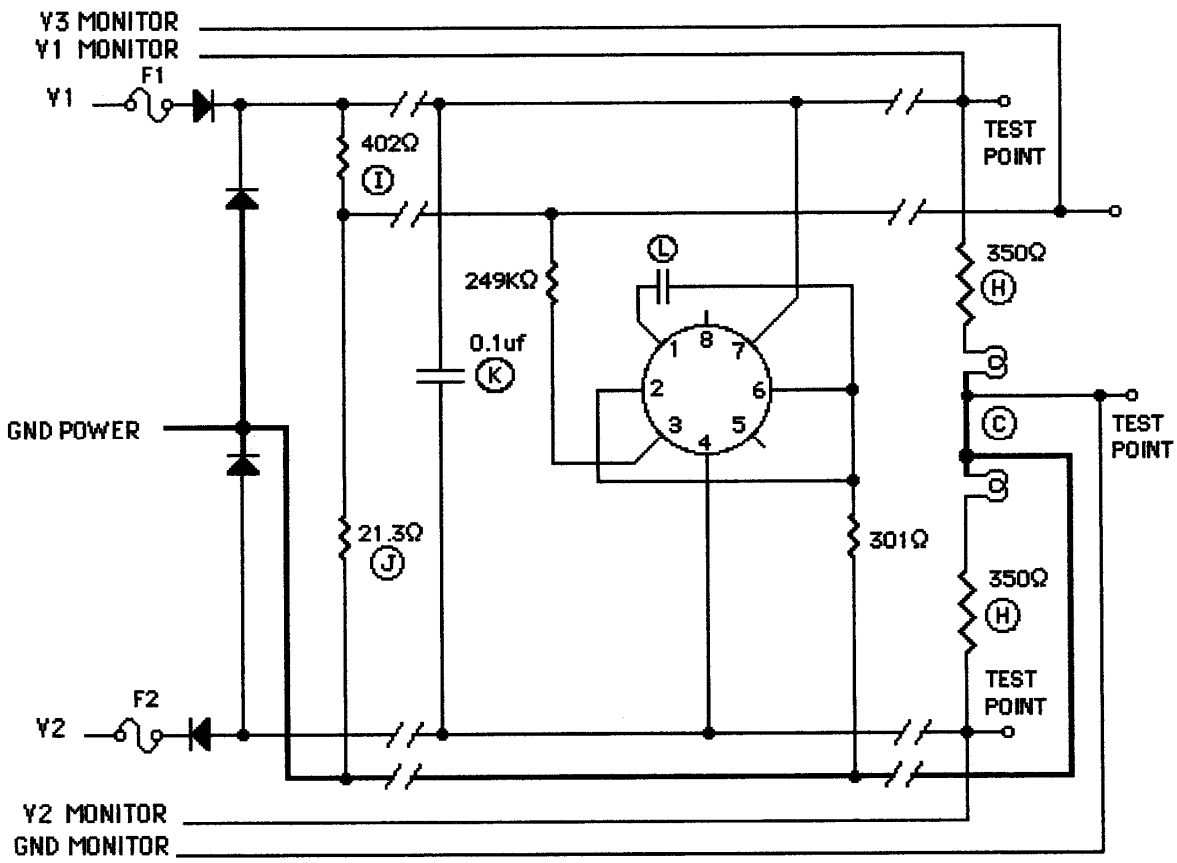
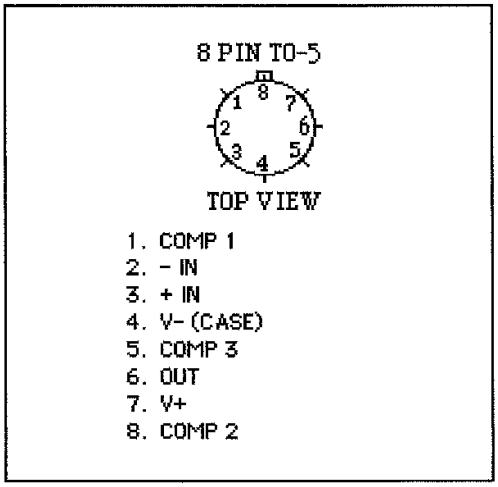


FIGURE 6

STATIC BURN-IN CIRCUIT
OPTION 1, T05 METAL CAN / 8 LEADS



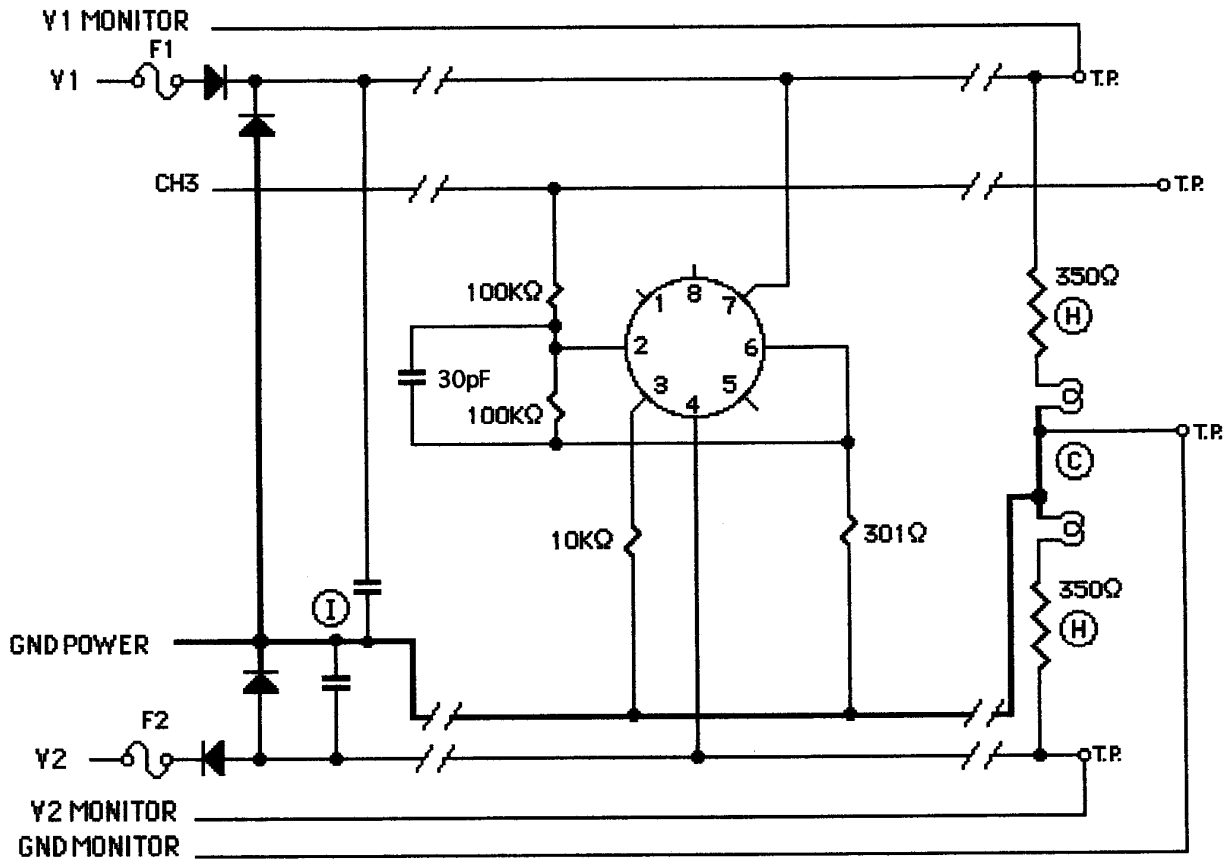
NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = + 163° C maximum.
3. Ta = +125 ° C .
4. Burn-in Voltages:V1 = +18V to +19.8V
   V2 = -18V to -19.8V
5. USE ALL OTHER INFORMATION ON # 04-06-0055



PACKAGE

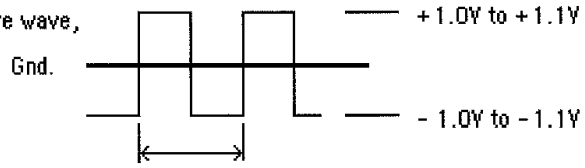
FIGURE 7

DYNAMIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN 8 LEADS

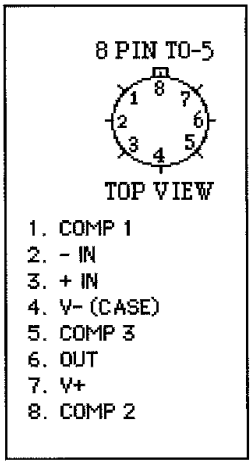


NOTES;

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = + 164 ° C maximum.
3. Ta = +125 ° C .
4. Burn-in Voltages: V1 = +18V to +19.8V
   V2 = -18V to -19.8V
5. CH. 3 = Square wave,



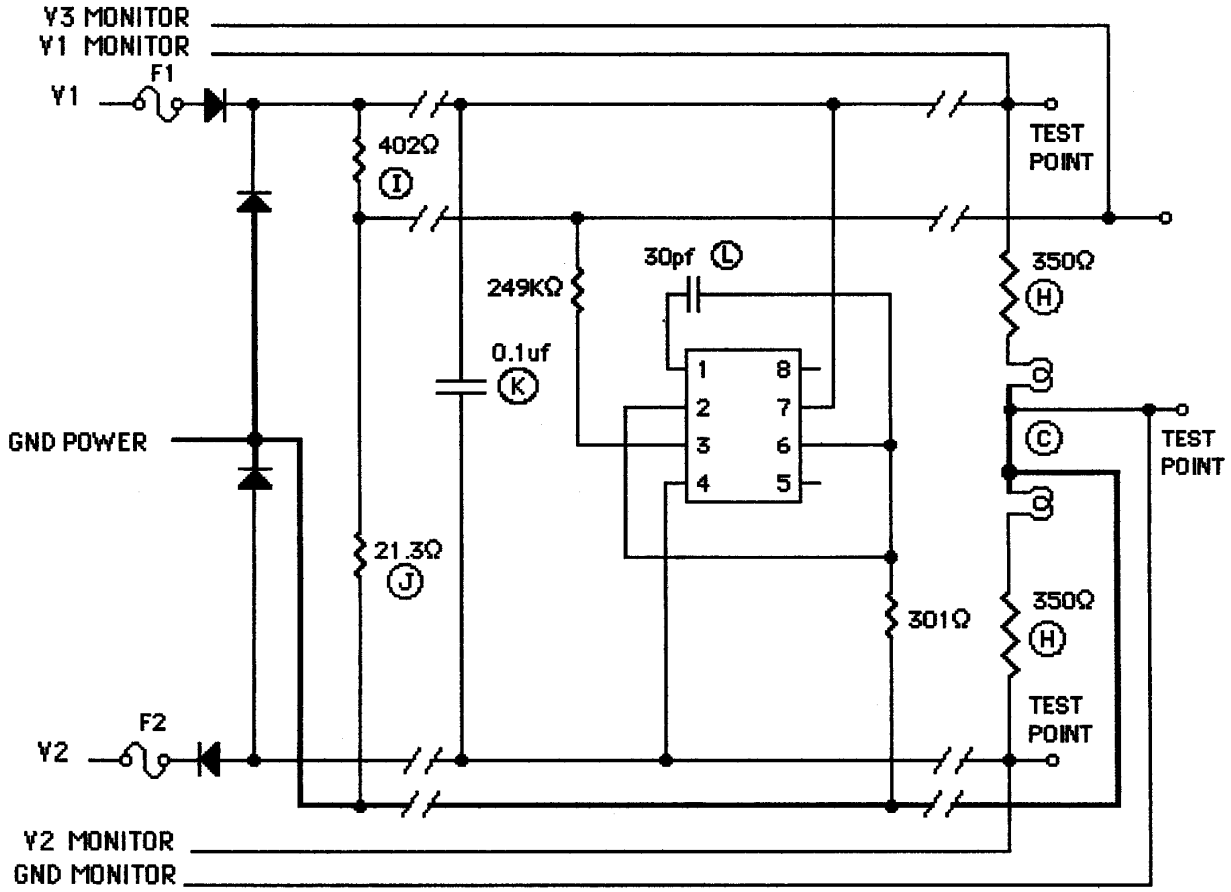
Frequency, 4.5hz(222ms) to 5.5hz(182ms)



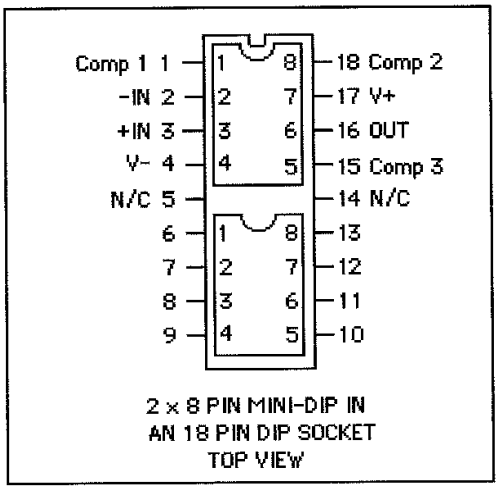
PACKAGE

FIGURE 8

STATIC BURN-IN CIRCUIT
OPTION #2, CERAMIC DIP / 8 LEADS



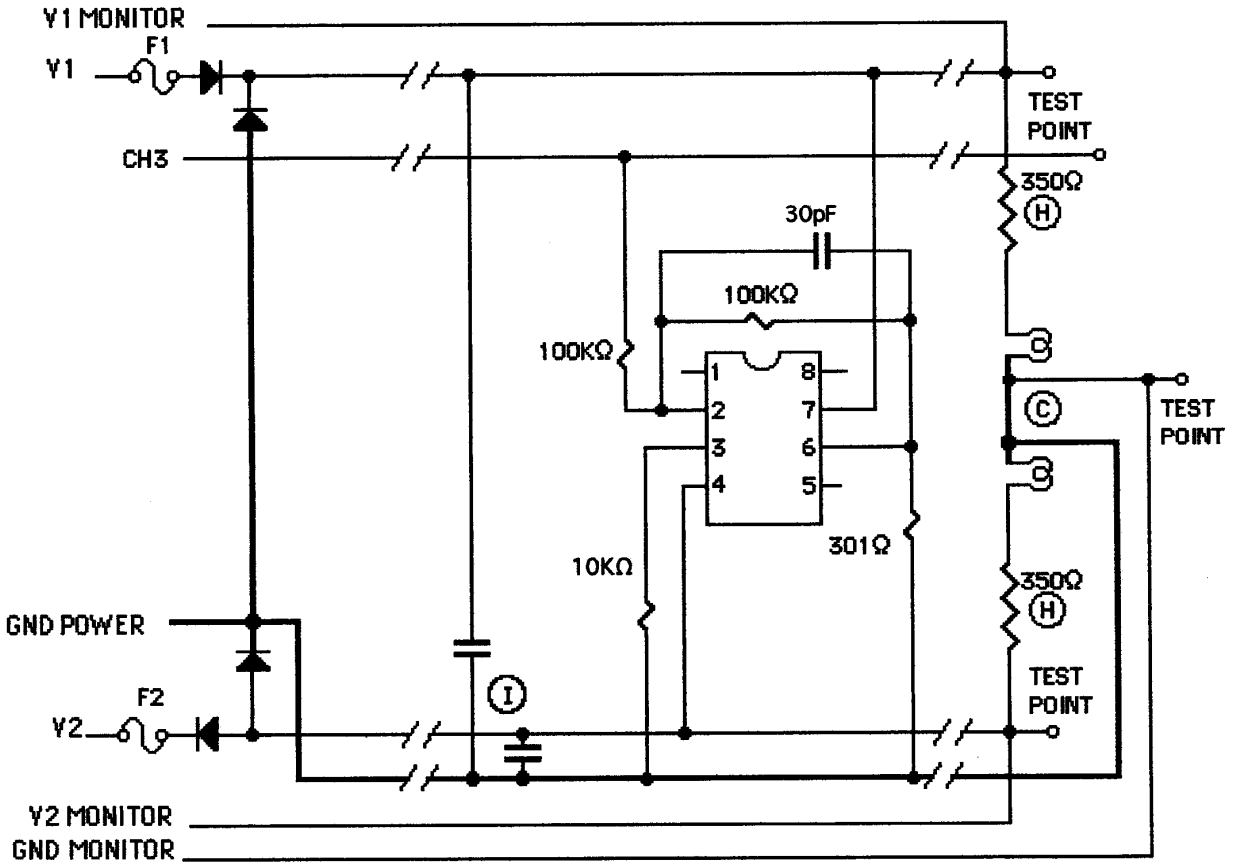
NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = + 163° C maximum.
3. Ta = +125 ° C .
4. Burn-in Voltages: V1 = +18V to +19.8V
   V2 = -18V to -19.8V



PACKAGE

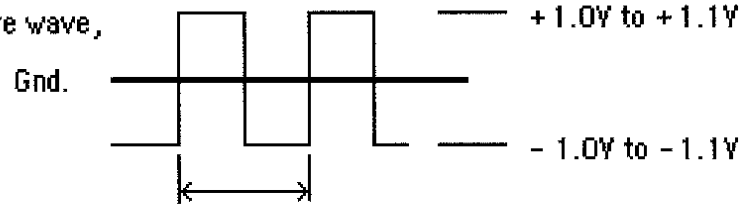
FIGURE 9

DYNAMIC BURN-IN CIRCUIT
OPTION 2, CERAMIC DIP / 8 LEADS

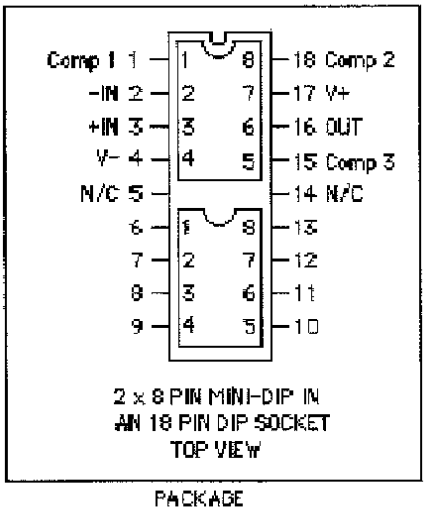


NOTES;

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = + 164 ° C maximum.
3. Ta = +125 ° C .
4. Burn-in Voltages:V1 = +18V to +19.8V
   V2 = -18V to -19.8V
5. CH. 3 = Square wave,



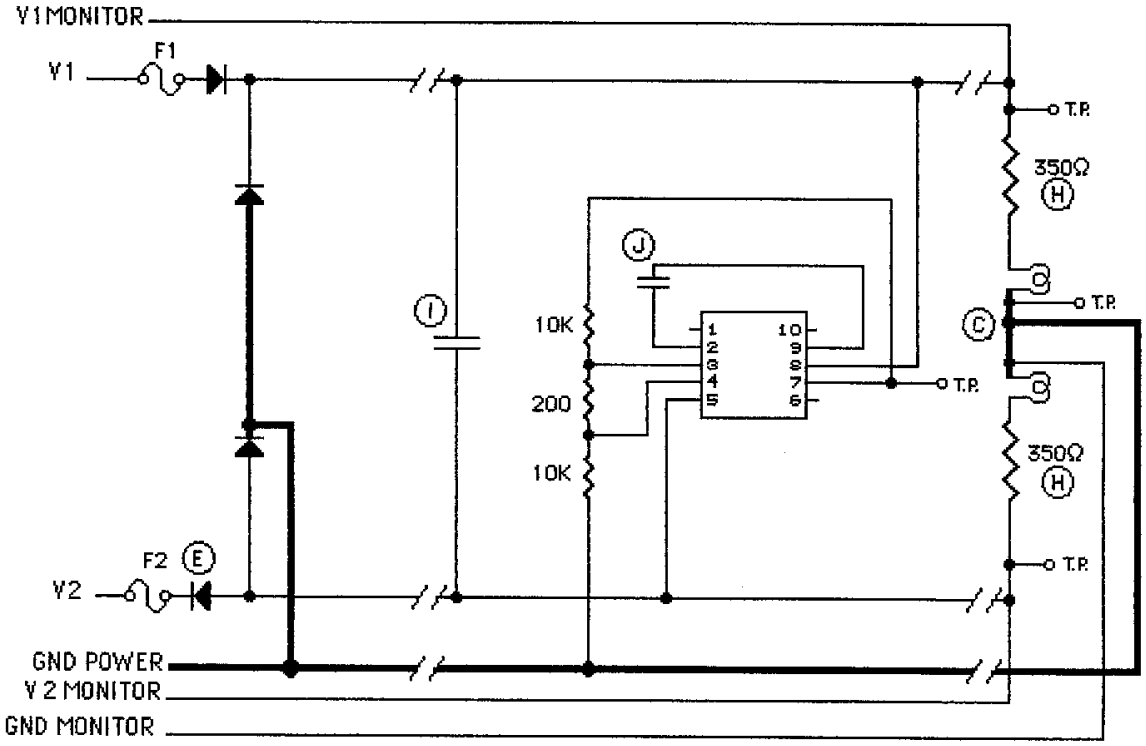
Frequency, 4.5hz(222ms) to 5.5hz(182ms)



PACKAGE

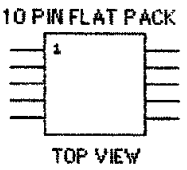
FIGURE 10

STATIC BURN-IN CIRCUIT
OPTION #3, GLASS SEALED FLATPACK, 10 LEADS



NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 164°C maximum.
3. Ta = 125°C.
4. Burn-in Voltages: V1 = +18V to +19.8V
   V2 = -18V to -19.8V

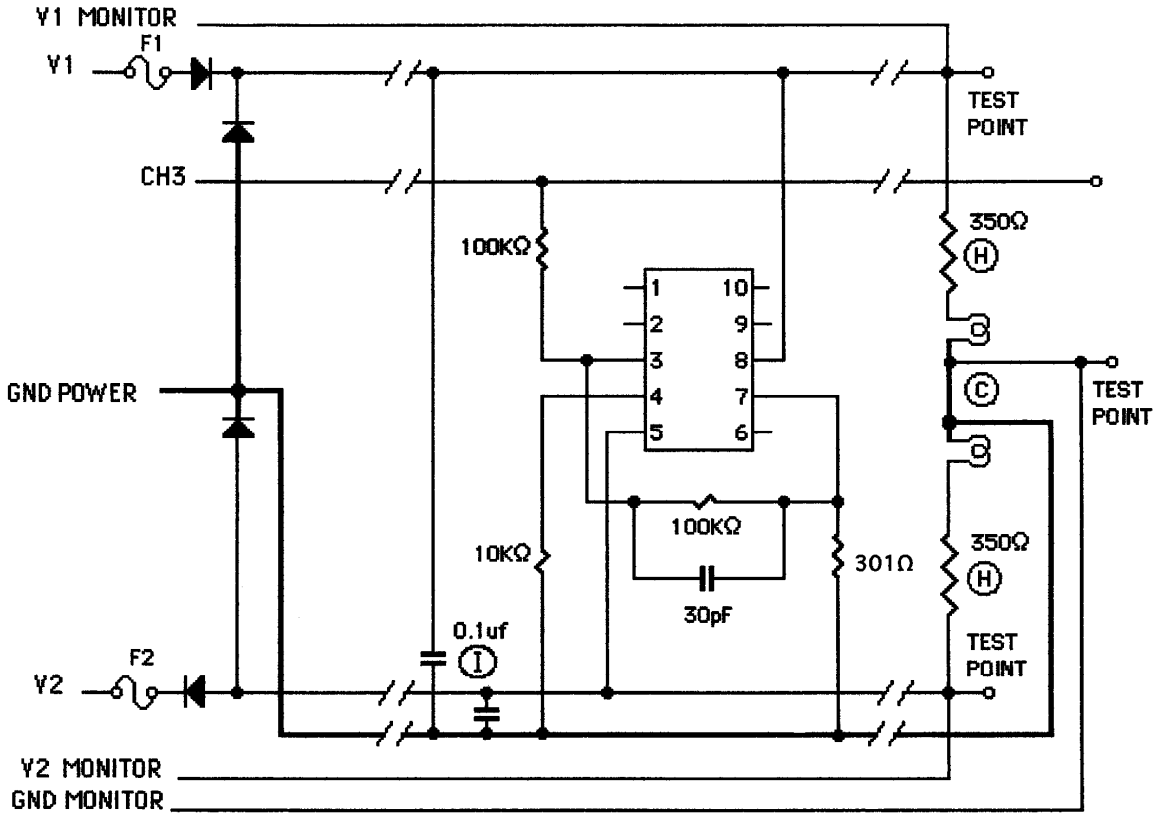
1. N/C
2. COMP A/BALANCE
3. - INPUT
4. + INPUT
5. V-
6. COMP B/BALANCE
7. OUTPUT
8. V+
9. COMP C
10. N/C



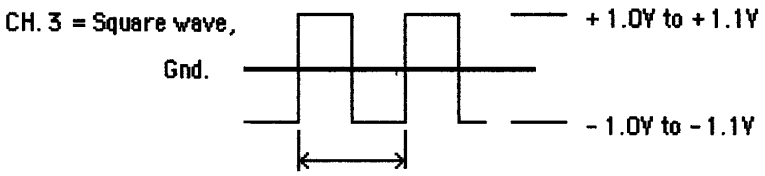
PACKAGE AND PINOUT

FIGURE 11

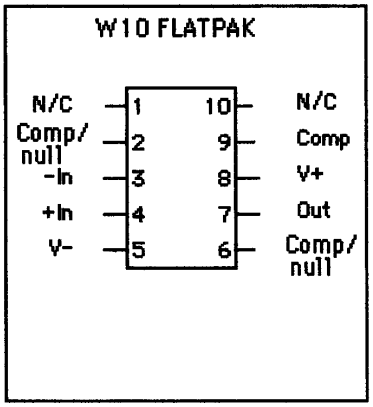
DYNAMIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED
FLATPACK / 10 LEADS



NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = +159 °C maximum., Tc = 135 °C minimum, at ambient of 100 °C.
3. Tj = +184 ° C maximum., at ambient of 125 °C.
4. Burn-in Voltages:V1 = +18V to +19.8V
   V3 = -18V to -19.8V
5. Device current maximum = 6mA.



Frequency, 4.5hz(222ms) to 5.5hz(182ms)



PACKAGE

FIGURE 12

TOTAL DOSE BIAS CIRCUIT

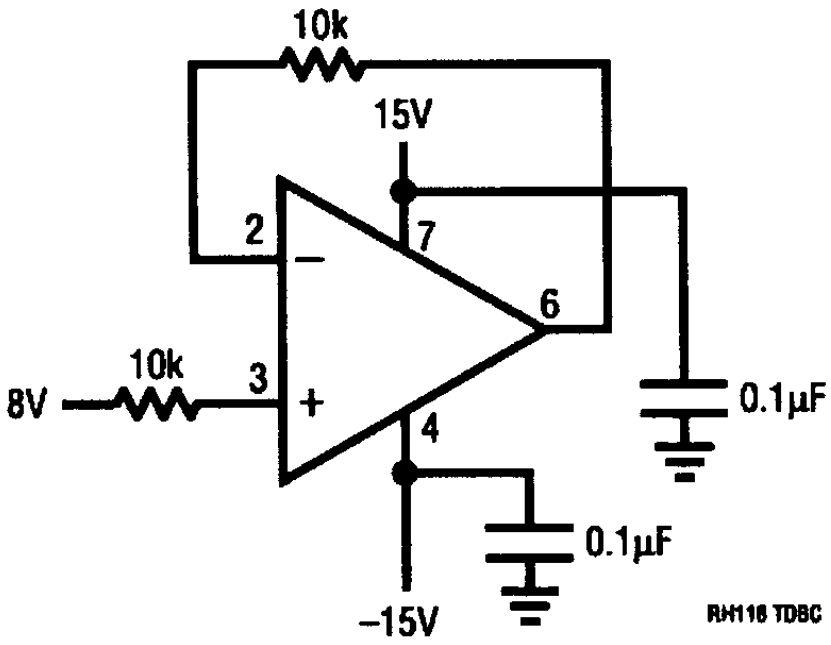


FIGURE 13

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) Note 3

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	TYP	MAX	SUB-GROUP	−55°C ≤ T_A ≤ 125°C MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage					4	1			6	2,3	mV
I_{OS}	Input Offset Current					50	1			100	2,3	nA
I_B	Input Bias Current					250	1			500	2,3	nA
R_{IN}	Input Resistance		4	1								MΩ
A_V	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L ≥ 2k		50			1	25			2,3	V/mV
SR	Slew Rate	V_S = ±15V, A_V = 1	5	50								V/µs
GBW	Gain Bandwidth Product	V_S = ±15V			15							MHz
	Output Voltage Swing	V_S = ±15V, R_L = 2k		±12			4	±12			5,6	V
	Input Voltage Range	V_S = ±20V		±16.5			1	±16.5			2,3	V
I_S	Supply Current					8	1					mA
		T_A = 125°C								7	2	mA
CMRR	Common Mode Rejection Ratio			80			1	80			2,3	dB
PSRR	Power Supply Rejection Ratio			70			1	70			2,3	dB

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) Note 6

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	MAX	20Krad(Si) MIN	MAX	50Krad(Si) MIN	MAX	100Krad(Si) MIN	MAX	200Krad(Si) MIN	MAX	UNITS
V_{OS}	Input Offset Voltage				4		4		4		4		10	mV
I_{OS}	Input Offset Current				50		50		50		50		100	nA
I_B	Input Bias Current				250		250		250		300		400	nA
R_{IN}	Input Resistance		4	1		1		1		0.5		0.5		MΩ
A_V	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L ≥ 2k		50		50		50		50		25		V/mV
SR	Slew Rate	V_S = ±15V, A_V = 1	5	50		50		50		50		50		V/µs
GBW	Gain Bandwidth Product	V_S = ±15V		15(Typ)		15(Typ)		15(Typ)		15(Typ)		15(Typ)		MHz
	Output Voltage Swing	V_S = ±15V, R_L = 2k		±12		±12		±12		±12		±12		V
	Input Voltage Range			±16.5		±16.5		±16.5		±15		±12		V
I_S	Supply Current				8		8		8		8		8	mA
CMRR	Common Mode Rejection Ratio			80		80		80		80		70		dB
PSRR	Power Supply Rejection Ratio			70		70		70		70		60		dB

Note 1: The inputs are shunted with back-to-back Zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for ±5V ≤ V_S ≤ ±20V. The power supplies must be bypassed with a 0.1µF or greater disc capacitor within four inches of the device.

Note 4: Guaranteed by design, characterization or correlation to other tested parameters.

Note 5: Slew rate is 100% tested at wafer probe testing. It is QA sample tested in finished package form.

Note 6: T_A = 25°C, V_S = ±20V, V_{CM} = 0V, unless otherwise specified. Supply bypassed per Note 3.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-4.0	4.0	-2.0	2.0	mV
$+I_{IB}$	1.0	250	-25	25	nA
$-I_{IB}$	1.0	250	-25	25	nA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5 6
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3, 4, 5, 6
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in that lot shall be used to determine the percent for the lot.