REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	Apr. 27, 2009
A	Pages 1 through 12, changed title from RH1185MK to RH1185AMK. Page 3, Re-formatted the Absolute Maximum Rating for the Thermal Resistance Junction to Case, TO-3 Control Area from 1DEGC/W to 1°C/W and the Power Transistor from 3 DEGC/W to 3ºC/W. Page 10, removed REF Pin Shutdown Current from Tables I and Table II Electrical Characteristics. PARAGRAPH 3.1. STATES "Positive Adjustable Regulator". Corrected Typo To State "Negative Adjustable Regulator".	May 6, 2011
B	**Pages 10 and 11, removed REF Pin Shutdown Current from Table I and Table II Electrical Characteristics.**	**June 21, 2011**

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12					
INDEX	REVISION	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**	**B**					
REVISION	PAGE NO.																	
INDEX	REVISION																	

	ORIG			**LINEAR TECHNOLOGY CORPORATION** **MILPITAS, CALIFORNIA**		
	DSGN			TITLE:		
	ENGR			**MICROCIRCUIT, LINEAR,** **RH1185AMK, Negative Regulator with Adjustable Current Limit**		
	MFG					
	CM					
	QA			SIZE	CAGE CODE	DRAWING NUMBER	REV
	PROG				**64155**	**05-08-5206**	**B**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:		

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1185AMK , 3A LOW DROPOUT NEGATIVE ADJUSTABLE REGULATOR, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 RH1185AMK (TO3 METAL CAN, 4 LEADS)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings (Note 1)

Input Voltage	35V
Input - Output Differential	30V
FB Voltage	7V
REF Voltage	7V
Output Voltage	30V
Output Reverse Voltage	2V
Operating Ambient Temperature Range	-55°C to 125°C
Operating Junction Temperature Range	
Control Section	-55°C to +150°C
Power Transistor Section	-55°C to +175°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Thermal Resistance Junction to Case	
TO-3 Control Area	1°C/W
Power Transistor	3°C/W

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 2.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and **Table II.**

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 (TO3, 4 Leads): Static Burn-in, Figure 3.

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 2.

3.10.3 Lead Material and Finish: The lead material and finish shall be Alloy 52 for device option 1 with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 4.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1

Group B, Subgroup 2c = 10%	Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)
Group B, Subgroup 3 = 10%	
Group B, Subgroup 4 = 5%	Group B, subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

4.6.9 A copy of outside test laboratory radiation report if ordered

4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

(K) TO3 / 4 LEADS CASE OUTLINE

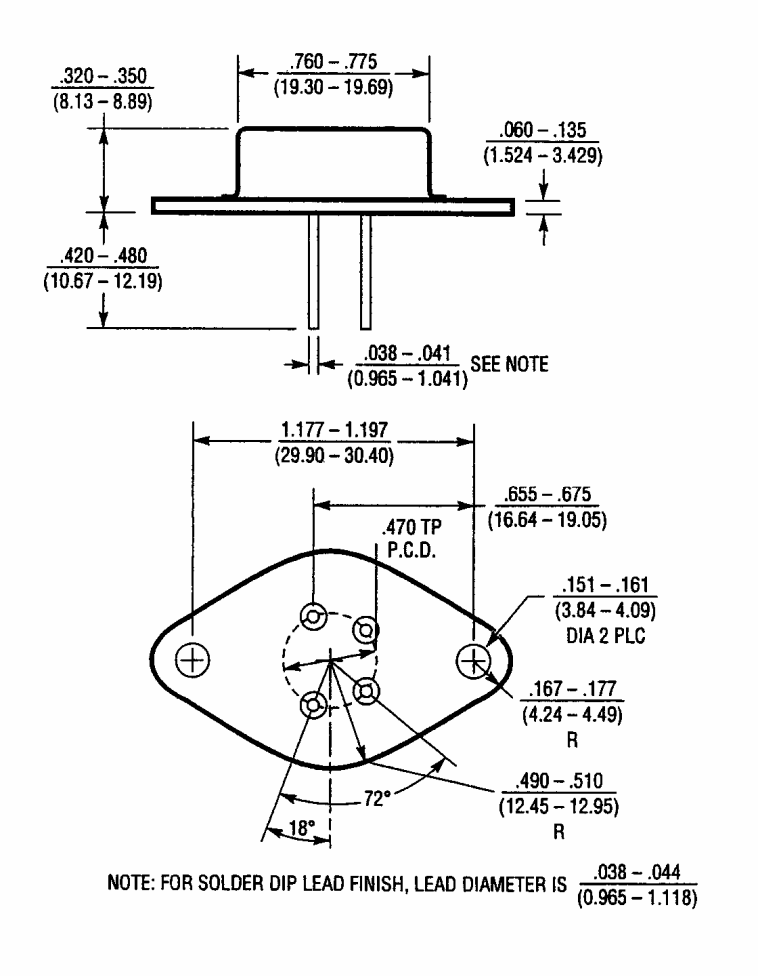


FIGURE 1

TERMINAL CONNECTIONS
TO3 / 4 LEAD METAL CAN

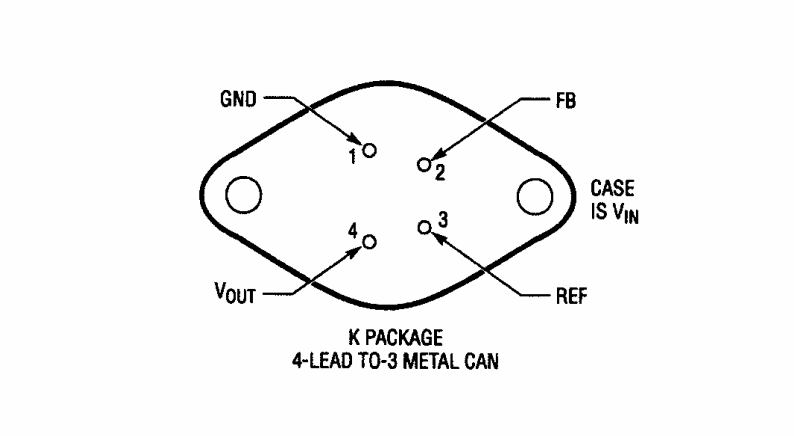
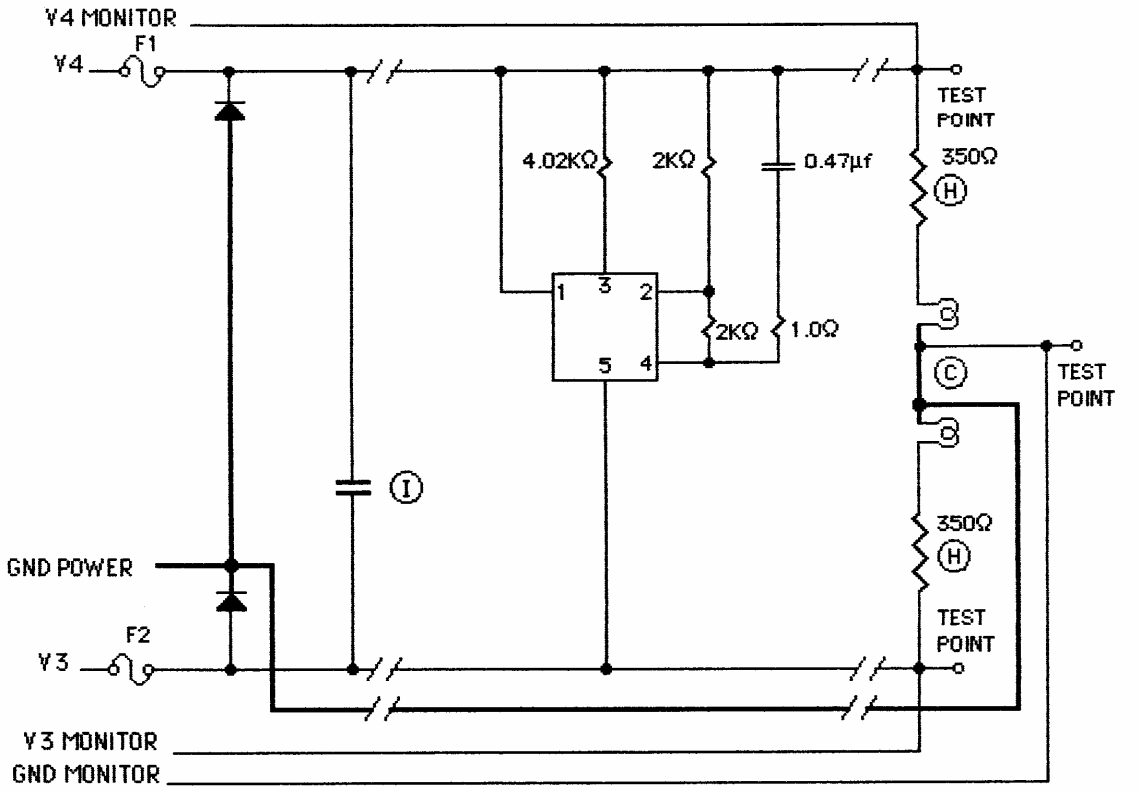


FIGURE 2

STATIC BURN-IN CIRCUIT
TO3 METAL CAN / 4 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 163°C maximum.
3. Ta = 150 °C.
4. Burn-in voltages: V4 = +15V to +16.5V
   V3 = -15V to -16.5V

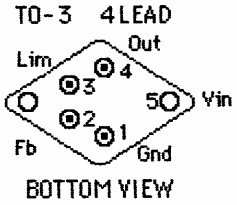


FIGURE 3

TOTAL DOSE BIAS CIRCUIT

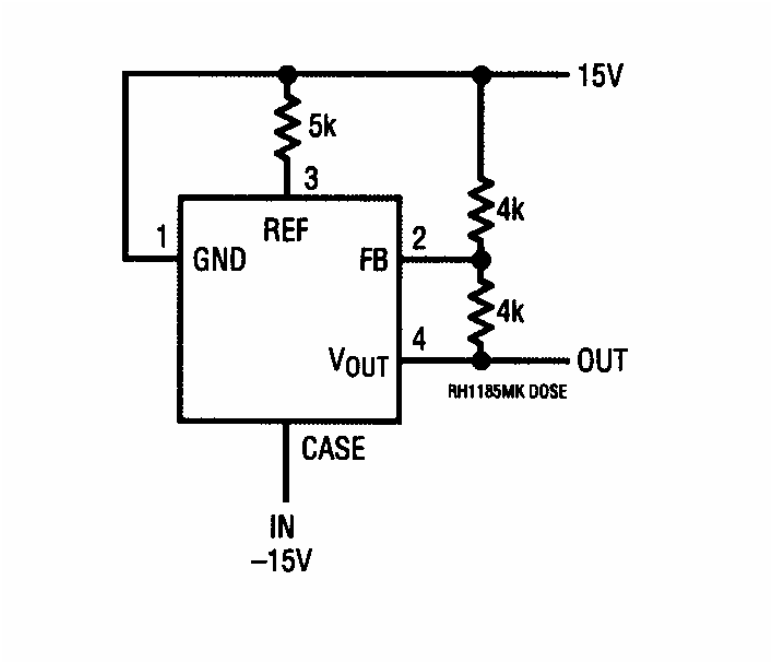


FIGURE 4

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION)

PARAMETER AND CONDITIONS	$T_A = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_A \le 125°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
Reference Voltage (At FB Pin)		2.37				2.37			V
Reference Voltage Tolerence (At FB Pin) (Note 2) $V_{IN} - V_{OUT} = 5V$, $V_{OUT} = V_{REF}$	–1.0	0.3	1.0	1					%
Reference Voltage Tolerance $V_{IN} - V_{OUT} = 1.2V$ to $V_{IN} = 30V$, $1mA \le I_{OUT} \le 3A$, $P_D \le 25W$ (Note 6), $V_{OUT} = 5V$, $T_{MIN} \le T_J \le T_{MAX}$ (Note 9)					–2.5		2.5	2, 3	%
Feedback Pin Bias Current, $V_{OUT} = V_{REF}$		0.7	2	1			2	2, 3	µA
Dropout Voltage (Note 3) $I_{OUT} = 0.5A$, $V_{OUT} = 5V$ $I_{OUT} = 3A$, $V_{OUT} = 5V$		0.2 0.67	0.37 1	1 1			0.55 1.4	2, 3 2, 3	V V
Load Regulation (Note 7) $I_{OUT} = 5mA$ to $3A$, $V_{IN} - V_{OUT} = 1.5V$ to $10V$, $V_{OUT} = 5V$		0.05	0.3	1			0.8	2, 3	%
Line Regulation (Note 7) $V_{IN} - V_{OUT} = 1V$ to $20V$, $V_{OUT} = 5V$		0.002	0.01	1			0.03	2, 3	%/V
Minimum Input Votlage (Note 4) $I_{OUT} = 1A$, $V_{OUT} = V_{REF}$ $I_{OUT} = 3A$, $V_{OUT} = V_{REF}$			3.9 4.4	1 1					V V
Internal Current Limit (See Graph for Guaranteed Curve) (Note 12) $1.5V \le V_{IN} - V_{OUT} \le 10V$ $V_{IN} - V_{OUT} = 15V$ $V_{IN} - V_{OUT} = 20V$ $V_{IN} - V_{OUT} = 30V$	 3.3 2 1 0.2	 3.6 3 1.7 0.4	 4.2 4.2 2.6 1	 1 1 1 1	 3.1 2 1 0.2	 4.4 4.3 3 1.1	 2, 3 2, 3 2, 3 2, 3	 A A A A
External Current Limit (Note 11) $R_{LIM} = 5k$, $V_{OUT} = 1V$ $R_{LIM} = 15k$, $V_{OUT} = 1V$	2.7 0.9	3 1	3.3 1.1	1 1	2.5 0.8		3.5 1.2	2, 3 2, 3	A A
Quiescent Supply Current (Note 5) $I_{OUT} = 5mA$, $V_{OUT} = V_{REF}$, $4V \le V_{IN} \le 25V$		2.5	3.5	1			3.5	2, 3	mA
Supply Current Change With Load $V_{IN} - V_{OUT} = V_{SAT}$ (Note 10) $V_{IN} - V_{OUT} \ge 2V$			25 15	1 1			40 25	2, 3 2, 3	mA mA
Thermal Regulation $V_{IN} - V_{OUT} = 10V$, $I_{OUT} = 5mA$ to $2A$							0.014		%/W
Reference Voltage Temperature Coefficient (Note 8)							0.01		%/°C

ALL NOTES ON NEXT PAGE.

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION)

T_A = 25°C unless otherwise noted.

PARAMETER AND CONDITONS	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
Reference Voltage Tolerance $V_{IN} - V_{OUT}$ = 5V, $V_{OUT} = V_{REF}$	–1.2	1.2	–1.2	1.2	–1.5	1.5	–1.5	1.5	–2	2	%
Reference Voltage Tolerance $V_{IN} - V_{OUT}$ = 1.2V to V_{IN} = 30V, 1mA ≤ I_{OUT} ≤ 3A, P_D ≤ 25W (Note 6), V_{OUT} = 5V, $T_{MIN} \le T_J \le T_{MAX}$ (Note 9)	–3	3	–3	3	–3.2	3.2	–3.5	3.5	–4	4	%
Feedback PIn Bias Current, $V_{OUT} = V_{REF}$		2		2		2.5		3		3	µA
Dropout Voltage (Note 3) I_{OUT} = 0.5A, V_{OUT} = 5V I_{OUT} = 3A, V_{OUT} = 5V		0.4 1		0.4 1		0.4 1		0.425 1.05		0.45 1.1	V V
Load Regulation (Note 7) I_{OUT} = 5mA to 3A $V_{IN} - V_{OUT}$ = 1.5V to 10V, V_{OUT} = 5V		0.3		0.4		0.5		0.8		1	%
Line Regulation, Absolute Value (Note 7) $V_{IN} - V_{OUT}$ = 1V to 20V, V_{OUT} = 5V		0.01		0.01		0.01		0.02		0.05	%/V
Minimum Input Voltage (Note 4) I_{OUT} = 1A, $V_{OUT} = V_{REF}$ I_{OUT} = 3A, $V_{OUT} = V_{REF}$		3.9 4.4		3.9 4.4		3.9 4.4		4 4.5		4 4.5	V V
Internal Current Limit (Note 12) 1.5V ≤ $V_{IN} - V_{OUT}$ ≤ 10V $V_{IN} - V_{OUT}$ = 15V $V_{IN} - V_{OUT}$ = 20V $V_{IN} - V_{OUT}$ = 30V	3.3 2 1 0.2	4.3 4.3 2.7 1	3.3 2 1 0.2	4.3 4.3 2.75 1.15	3.3 2 1 0.2	4.4 4.35 2.85 1.3	3.3 2 1 0.2	4.55 4.5 3.1 1.6	3.3 2 1 0.2	4.75 4.7 3.3 2	A A A A
External Current Limit (Note 11) R_{LIM} = 5k R_{LIM} = 15k	2.7 0.9	3.3 1.1	2.7 0.9	3.4 1.25	2.7 0.9	3.5 1.4	2.7 0.9	3.7 1.6	2.7 0.9	3.9 1.9	A A
Quiescent Supply Current I_{OUT} = 5mA, $V_{OUT} = V_{REF}$, 4V ≤ V_{IN} ≤ 25V		3.5		3.5		3.5		3.5		3.5	mA
Supply Current Change With Load $V_{IN} - V_{OUT} = V_{SAT}$ $V_{IN} - V_{OUT} \ge 2V$		25 15		27 16		30 18		35 21		45 27	mA/A mA/A

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Reference voltage is guaranteed both at nominal conditions (no load, 25°C) and at worst-case conditions of load, line, power and temperature.

Note 3: Dropout voltage is tested by reducing input voltage until the output drops 1% below its nominal value. Tests are done at 0.5A and 3A. The power transistor looks basically like a pure resistance in this range so that minimum differential at any intermediate current can be calculated by interpolation; $V_{DROPOUT} = 0.25V + 0.25\Omega \bullet I_{OUT}$. For load current other than 0.5A and 3.0A, see graph in LT1185 data sheet.

Note 4: "Minimum input voltage" is limited by base emitter voltage drive of the power transistor section, not saturation as measured in Note 3. For output voltages below 4V, "minimum input voltage" specification may limit dropout voltage before transistor saturation limitation.

Note 5: Supply current is measured on the ground pin, and does not include load current, R_{LIM}, or output divider current.

Note 6: The 25W power level is guaranteed for an input-output voltage of 8.3V to 17V. At lower voltages the 3A limit applies, and at higher voltages the internal power limiting may restrict regulator power below 25W. See graph of Internal Current Limit in LT1185 data sheet.

Note 7: Line and load regulation are measured on a pulse basis with a pulse width of ≈2ms, to minimize heating. DC regulation will be affected by thermal regulation and temperature coefficient of the reference. See the Applications Information section of LT1185 data sheet for details.

Note 8: Guaranteed by design and correlation to other tests, but not tested.

Note 9: T_{JMIN} = –55°C for the RH1185AMK. Power transistor area and control circuit area have different maximum junction temperatures. Control area limit is T_{JMAX} = 150°C for the RH1185AMK. Power area limit is 175°C for RH1185AMK.

Note 10: V_{SAT} is the maximum specified dropout voltage; $0.25V + 0.25\Omega \bullet I_{OUT}$.

Note 11: Current limit is programmed with a resistor from REF pin to GND pin. The value is 15k • A/I-limit.

Note 12: For $V_{IN} - V_{OUT}$ = 1.5V, V_{IN} = 5V and V_{OUT} = 3.5V. For all other current limit tests, V_{OUT} = 1.0V

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C

PARAMETER and CONDITIONS	ENDPOINT LIMIT		DELTA LIMITS		
	MIN	MAX	MIN	MAX	UNITS
Reference Voltage, V_{REF}					
Vin = 7.4V, Vout = V_{REF}	2.346	2.394	-0.040	+0.040	V

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1; SEE PDA TEST NOTE.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot. Linear Technology Corporation reserves the right to test to tighter limits than those given.