REVISION RECORD

REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/03/11
A	Pg 11, revised conditions for A_{VOL} IN TABLE I – PARAMETER CONDITIONS: from: V_S = ±5V; R_L = 100Ω; V_{OUT} = ±4.5V to: V_S = ±5V; R_L = 100Ω; V_{OUT} = ±2V	07/27/11
B	Page 2, amended section 3.3 Special Handling of Dice to more accurately describe our current procedures and requirements.	04/05/12
C	Page 13, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from "15%" to "10%".	07/02/13
D	Updated Die Sales table on pg 13.	05/20/15
E	**To remove SI and change Linear Technology to Analog Device**	**01/29/21**

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13			
INDEX	REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**			
REVISION	PAGE NO.																
INDEX	REVISION																

	ORIG		
	DSGN		
	ENGR		
	MFG		
	CM		
	QA		
	PROG		
APPLICATION	FUNCT	SIGNOFFS	DATE

ANALOG DEVICES INC.

TITLE:

MICROCIRCUIT, LINEAR, RH6200M DICE LOW NOISE, HIGH SPEED RAIL-TO-RAIL OP AMP

SIZE	CAGE CODE	DRAWING NUMBER	REV
	64155	**05-08-5250**	**E**

CONTRACT:

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH6200M DICE and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number: **RH6200M DICE,**

3.3 **Special Handling of Dice:** Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Analog Devices Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

ADI recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings: All notes are on page 12.

(Note 1)	
Total Supply Voltage (V^+ to V^-)	12.6V
Input Current (Note 2)	±40mA
Output Short-Circuit Duration (Note 3)	Indefinite
Pin Current While Exceeding Supplies (Note 4)	±30mA
Operating Junction Temperature Range (Note 5)	-55˚C to 125˚C
Storage Temperature Range	-65˚C to 150˚C
Lead Temperature (Soldering, 10 sec)	300˚C

3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.

3.7 Radiation Hardness Assurance (RHA):

3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.7.3 Total dose bias circuit is specified in **Figure 2**.

3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at Ta = +25°C to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.

3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ.**

3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.

4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.

5.0 SAMPLE ELEMENT EVALUATION: A sample from **each wafer supplying dice** shall be assembled and subjected to element evaluation per **Table III** herein.

5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.

5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in **Table I** and **Table II** herein.

5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.

5.4 Part Marking of Element Evaluation Sample Includes**:**

5.4.1 LTC Logo

5.4.2 LTC Part Number

5.4.3 Date Code

5.4.4 Serial Number

5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A

5.4.6 Diffusion Lot Number

5.4.7 Wafer Number

5.5 Burn-In Requirement: Burn-In circuit for Cerpac (W) package is specified in **Figure 3**.

5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with **Figure 4.**

5.7 Terminal Connections: The terminal connections shall be as specified in **Figure 5.**

5.8 Lead Material and Finish: The lead material and finish shall be alloy 42 with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with **Table III** herein.

6.3 Screening: Screening requirements shall be in accordance with **Table III** herein.

6.4 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

6.4.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.

6.4.2 100% attributes (completed element evaluation traveler).

6.4.3 Element Evaluation variables data, including Burn-In and Op Life

6.4.4 SEM photographs (3.10 herein)

6.4.5 Wafer Lot Acceptance Report (3.9 herein)

6.4.6 A copy of outside test laboratory radiation report if ordered

6.4.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6.4.1 and 6.4.7 will be delivered as a minimum, with each shipment.

7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

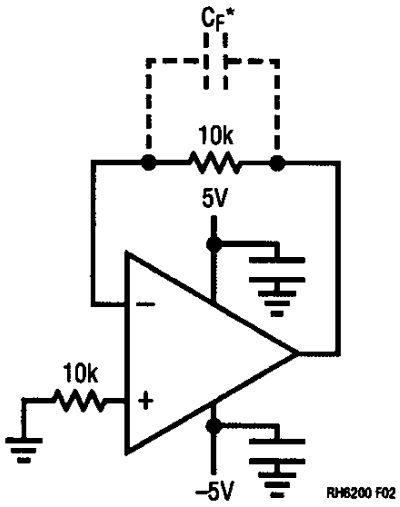
DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS

PAD FUNCTION

1. $\overline{\text{SHDN}}$
2. −IN
3. +IN
4. OUT
5. V^-
6. V^+

FIGURE 1

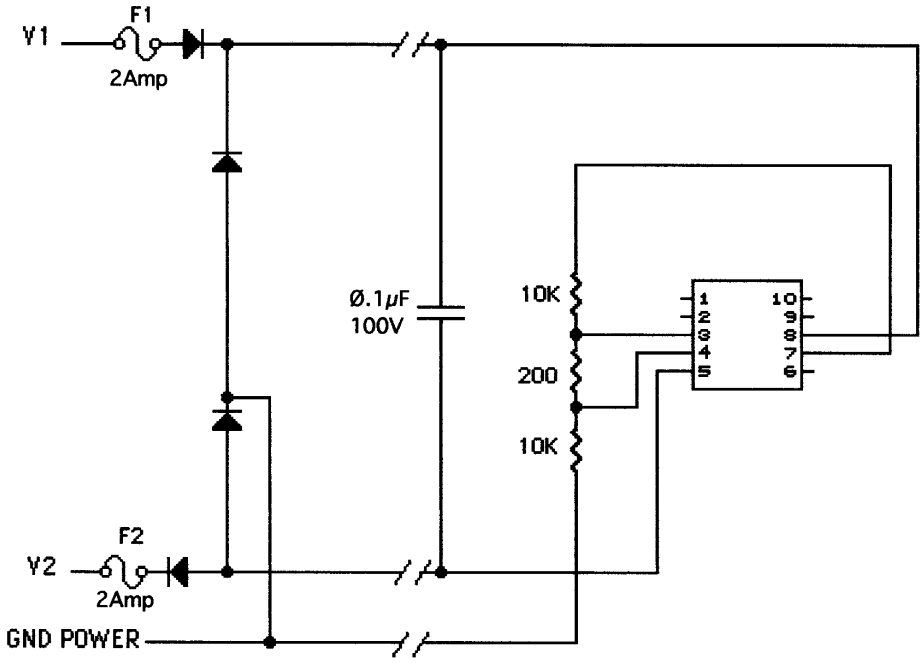
TOTAL DOSE BIAS CIRCUIT



*C_F IS COMPONENT OR PARASITIC CAPACITANCE ENSURING STABILITY

FIGURE 2

BURN-IN CIRCUIT



1. Unless otherwise specified, component tolerances shall be per military specification.
2. Ta = +90 ° C .
3. Tj = + 157° C maximum.
4. Tc = + 132° C minimum.
5. Diodes to be 1N5550.
6. Device current = 27mA.
7. Burn-in Voltages: V1 = +6.0V to +6.3V
   V2 = -6.0V to -6.3V

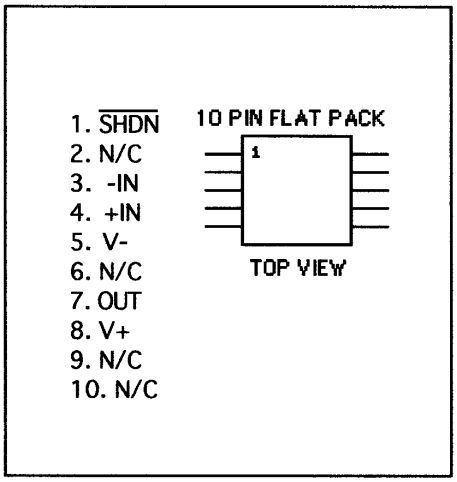
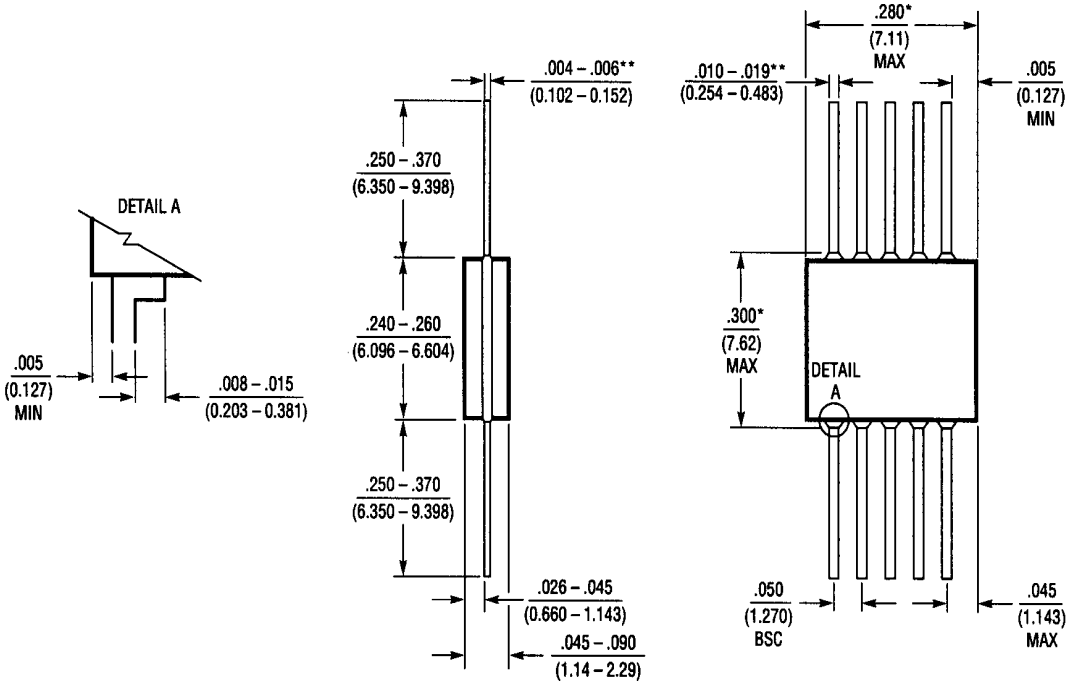


FIGURE 3

(W) CERPAC, 10 LEAD CASE OUTLINE



NOTES:
*THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN
**INCREASE DIMENSIONS BY 0.003 INCHES (0.076 mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED)

θja = +170°C / W
θjc = +40°C / W

FIGURE 4

(W) CERPAC, 10 LEAD TERMINAL CONNECTIONS

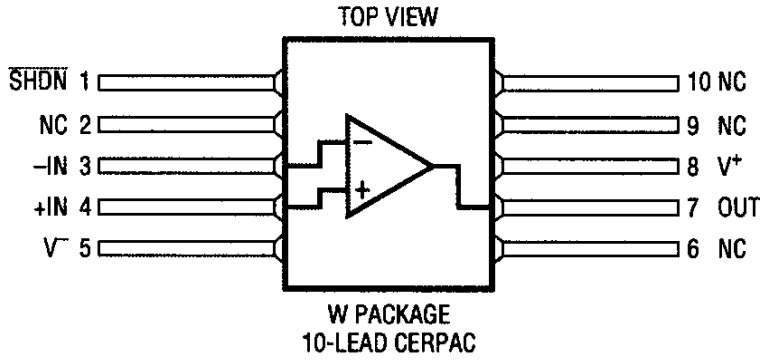


FIGURE 5

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation (Note 1)

DICE/DWF ELECTRICAL TEST LIMITS T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0V; V_{CM} = V^- to V^+		2	mV
		V_S = ±5V; V_{CM} = V^- to V^+		6	mV
I_B	Input Bias Current	V_S = 5V, 0V; V_{CM} = V^+		18	µA
		V_S = 5V, 0V; V_{CM} = V^-	–50		µA
		V_S = ±5V; V_{CM} = V^+		18	µA
		V_S = ±5V; V_{CM} = V^-	–50		µA
I_{OS}	Input Offset Current	V_S = 5V, 0V; V_{CM} = V^+		4	µA
		V_S = 5V, 0V; V_{CM} = V^-		5	µA
		V_S = ±5V; V_{CM} = V^+		7	µA
		V_S = ±5V; V_{CM} = V^-		12	µA
A_{VOL}	Large Signal Open-Loop Voltage Gain	V_S = 5V, 0V; R_L = 1k; V_{OUT} = 0.5V to 4.5V	70		V/mV
		V_S = 5V, 0V; R_L = 100Ω; V_{OUT} = 1V to 4V	11		V/mV
		V_S = ±5V; R_L = 1k; V_{OUT} = ±4.5V	115		V/mV
		V_S = ±5V; R_L = 100Ω; V_{OUT} = ±2V	15		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, 0V; V_{CM} = 0V to 5V	65		dB
		V_S = 5V, 0V; V_{CM} = 1.5V to 3.5V	85		dB
		V_S = ±5V; V_{CM} = ±5V	68		dB
		V_S = ±5V; V_{CM} = ±2V	75		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	60		dB
V_{OL}	Output Voltage Swing Low	V_S = 5V, 0V; I_L = 0		50	mV
		V_S = 5V, 0V; I_L = 5mA		100	mV
		V_S = 5V, 0V; I_L = 20mA		290	mV
		V_S = ±5V; I_L = 0		50	mV
		V_S = ±5V; I_L = 5mA		110	mV
		V_S = ±5V; I_L = 20mA		290	mV
V_{OH}	Output Voltage Swing High	V_S = 5V, 0V; I_L = 0		110	mV
		V_S = 5V, 0V; I_L = 5mA		190	mV
		V_S = 5V, 0V; I_L = 20mA		400	mV
		V_S = ±5V; I_L = 0		130	mV
		V_S = ±5V; I_L = 5mA		210	mV
		V_S = ±5V; I_L = 20mA		420	mV
I_{SC}	Short-Circuit Current	V_S = 5V, 0V or V_S = ±5V	±60		mA
I_S	Supply Current	V_S = 5V, 0V		20	mA
		V_S = ±5V		23	mA
$I_{S(SHDN)}$	Shutdown Supply Current	V_S = 5V, 0V		1.8	mA
		V_S = ±5V		2.1	mA
I_{SHDN}	Shutdown Pin Current	V_S = 5V, 0V or V_S = ±5V; V_{SHDN} = 0.3V	–280		µA
GBW	Gain Bandwidth Product	V_S = ±5V; at f = 1MHz	110		MHz

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much "softer" than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

NOTES ON NEXT PAGE

TABLE II ELECTRICAL CHARACTERISTICS – Post-Irradiation

T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0V; V_{CM} = V^- to V^+		2.2		2.4		2.6		2.8		3	mV
		V_S = ±5V; V_{CM} = V^- to V^+		6.5		7		7.5		8		8.5	mV
I_B	Input Bias Current	V_S = 5V, 0V, V_{CM} = V^+		20		22		24		26		28	µA
		V_S = 5V, 0V, V_{CM} = V^-	–55		–60		–65		–70		–75		µA
		V_S = ±5V, V_{CM} = V^+		20		22		24		26		28	µA
		V_S = ±5V, V_{CM} = V^-	–55		–60		–65		–70		–75		µA
I_{OS}	Input Offset Current	V_S = 5V, 0V; V_{CM} = V^+		5		6		7		8		9	µA
		V_S = 5V, 0V; V_{CM} = V^-		6		7		8		9		10	µA
		V_S = ±5V; V_{CM} = V^+		8		9		10		11		12	µA
		V_S = ±5V; V_{CM} = V^-		13		14		15		16		17	µA
A_{VOL}	Large Signal Open Loop Voltage Gain	V_S = 5V, 0V; R_L = 1k; V_{OUT} = 0.5V to 4.5V	65		60		55		50		45		V/mV
		V_S = 5V, 0V; R_L = 100Ω; V_{OUT} = 1V to 4V	10		9		8		7		6		V/mV
		V_S = ±5V; R_L = 1k; V_{OUT} = ±4.5V	110		100		90		80		70		V/mV
		V_S = ±5V; R_L = 100Ω; V_{OUT} = ±2V	13.5		12		10.5		9		7.5		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, 0V; V_{CM} = 0V to 5V	64		63		62		61		60		dB
		V_S = 5V, 0V; V_{CM} = 1.5V to 3.5V	84		83		82		81		80		dB
		V_S = ±5V; V_{CM} = ±5V	67		66		65		64		63		dB
		V_S = ±5V; V_{CM} = ±2V	74		73		72		71		70		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	59		58		57		56		55		dB
V_{OL}	Output Voltage Swing Low	V_S = 5V, 0V; I_L = 0		52		54		56		58		60	mV
		V_S = 5V, 0V; I_L = 5mA		104		108		112		116		120	mV
		V_S = 5V, 0V; I_L = 20mA		296		302		308		314		320	mV
		V_S = ±5V; I_L = 0		52		54		56		58		60	mV
		V_S = ±5V; I_L = 5mA		114		118		122		126		130	mV
		V_S = ±5V; I_L = 20mA		296		302		308		314		320	mV
V_{OH}	Output Voltage Swing High	V_S = 5V, 0V; I_L = 0		114		118		122		126		130	mV
		V_S = 5V, 0V; I_L = 5mA		198		206		214		222		230	mV
		V_S = 5V, 0V; I_L = 20mA		415		430		445		460		475	mV
		V_S = ±5V; I_L = 0		134		138		142		146		150	mV
		V_S = ±5V; I_L = 5mA		218		226		234		242		250	mV
		V_S = ±5V; I_L = 20mA		430		455		470		485		500	mV
I_{SC}	Short-Circuit Current	V_S = 5V, 0V or V_S = ±5V		58		56		54		52		50	mA
I_S	Supply Current	V_S = 5V, 0V		20.4		20.8		21.2		21.6		22	mA
		V_S = ±5V		23.4		23.8		24.2		24.6		25	mA
$I_{S(SHDN)}$	Shutdown Supply Current	V_S = 5V, 0V		1.84		1.88		1.92		1.96		2	mA
		V_S = ±5V		2.14		2.18		2.22		2.26		2.3	mA
I_{SHDN}	Shutdown Pin Current	V_S = 5V, 0V or V_S = ±5V; V_{SHDN} = 0.3V		–284		–288		–292		–296		–300	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current must be limited to less than 40mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: There are reverse-biased ESD diodes from all inputs and outputs to the respective supply pins. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient in nature and limited to less than 30mA, no damage to the device will occur.

Note 5: The RH6200 is tested under pulse load conditions such that $T_J \approx T_A$. The thermal resistance of the W 10-lead CERPAC package (without heat sink) is estimated at 170°C/W. For a given application, multiply the RMS power dissipation of the RH6200 times the package thermal resistance (including any heat sinking if present) to calculate the temperature difference between the ambient temperature and the junction temperature. The RH6200 has a thermal shutdown feature that protects the part from excessive junction temperature. The amplifier will shut down to an inactive, low current condition when the junction temperature exceeds approximately 160°C. The amplifier will remain shut down until the die cools off to below approximately 150°C, at which point the amplifier will return to normal operation.

Note 6: This parameter is not production tested. Typical bench evaluation performance listed for information only.

TABLE III RH ELEMENT EVALUATION TABLE QUALIFICATION OF DICE SALES

LINEAR TECHNOLOGY

RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS K/S	CLASS V	CLASS H/B	OPERATION	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY (ACCEPT NUMBER)
1	X	X		SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25°C)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
	X	X		BOND PULL MONITOR	2011		
5	X	X		STABILIZATION BAKE	1008	C	ASSEMBLED PARTS ONLY
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
	X	X		GROSS LEAK	1014	C	
6	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			45(0)
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X	X		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs.	1015	+ 125°c MINIMUM 240 HOURS	
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25°C			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X			TOTAL IRRADIATION DOSE	1019	A	
	X	X		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	X	X		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005	+ 125°c MINIMUM 1000 HOURS	
	X	X		POST OP-LIFE ELECT. (R & R @ 25°C, +125°C OR +150°C, -55°C			
7	X	X	X	WIRE BOND EVALUATION	2011		15(0) OR 25(1) - # of wires

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Surgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.